PIN ASSIGNMENT

(FPT-8P-M02)

## PIN DESCRIPTION

| Pin name | Pin no. | I/O | Description |
| :---: | :---: | :---: | :--- |
| XOUT | 1 | O | Resonator connection pin |
| OE | 2 | I/O | Clock output enable pin <br> L : output disable, H : output enable <br> Serial input/output pin (only program mode) |
| PEX | 3 | I | Programmable enable setting pin <br> L : program mode, $\mathrm{H}:$ normal operation |
| VSS | 4 | - | GND pin |
| OUT | 5 | O | Modulation clock output pin |
| VDD | 6 | - | Power supply voltage pin |
| NC | 7 | - | Non-connection pin (do not connect anything) |
| XIN | 8 | I | Resonator connection pin/clock input pin |

## I/O CIRCUIT TYPE

| Pin name | Circuit type | Remarks |
| :---: | :---: | :---: |
| PEX |  | - CMOS hysteresis input <br> - With pull-up resistor ( $50 \mathrm{k} \Omega$ ) |
| OE |  | With pull-up resistor ( $50 \mathrm{k} \Omega$ ) <br> - CMOS hysteresis input (Input) <br> In serial output mode <br> - CMOS output <br> - lol $=3 \mathrm{~mA}$ |
| OUT |  | - CMOS output <br> - lol $=3 \mathrm{~mA} / 7 \mathrm{~mA}$ selectable (Selectable by Output driver setting bit) <br> - Hi-Z or "L" output at OE = "L" (Selectable by OUT pin setting bit) |

Note : About XIN and XOUT pins, please refer to the chapter of " CRYSTAL OSCILLATION CIRCUIT".

## MB88R157

## HANDLING DEVICES

## - Preventing Latch-up

A latch-up can occur if, on this device, (a) a voltage higher than power supply voltage or a voltage lower than GND is applied to an input or output pin or (b) a voltage higher than the rating is applied between power supply and GND. The latch-up, if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use this device, be very careful not to exceed the maximum rating.

- Handling unused pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, using a pull-up or pulldown resistor.

- To use external clock input

To use an external clock signal, input the clock signal to the XIN pin with the XOUT pin connected to nothing.

## - Power supply pins

Please design connecting the power supply pin of this device by as low impedance as possible from the current supply source.
We recommend connecting electrolytic capacitor (about $10 \mu \mathrm{~F}$ ) and the ceramic capacitor (about $0.01 \mu \mathrm{~F}$ ) in parallel between power supply and GND near the device, as a bypass capacitor.

## - Oscillation circuit

Noise near the XIN pin and XOUT pin may cause the device to malfunction. Design printed circuit boards so that electric wiring of XIN pin or XOUT pin and the resonator do not intersect other wiring.
Design the printed circuit board that surrounds the XIN pin and XOUT pin with ground in order to stabilize operation.

## MB88R157

MEMORY MAP

| Address | Function | Remarks |
| :---: | :---: | :--- |
| bit0-bit11 | M divider setting (12-bit) | Selectable in the range of 1 to 4096 |
| bit12-bit22 | N divider setting (11-bit) | Selectable in the range of 1 to 2048 |
| bit23-bit29 | K divider setting (7-bit) | Selectable in the range of 1 to 128 |
| bit30-bit32 | L divider setting (3-bit) | Modulation frequency setting <br> (the value is due to the input frequency) |
| bit33-bit36 | Charge Pump setting (4-bit) | Charge pump current setting due to VCO oscillation frequency |
| bit37-bit41 | VCO Gain setting (5-bit) | VCO gain setting due to VCO oscillation frequency |
| bit42-bit44 | Modulation rate setting (3-bit) | No modulation, $\pm 0.25 \%, \pm 0.50 \%, \pm 0.75 \%, \pm 1.00 \%, \pm 1.25 \%$, <br> $\pm 1.50 \%, \pm 1.75 \%$ are selectable |
| bit45 | OUT pin setting (1bit) | Selectable OUT pin situation at OE pin $=\mathrm{L}$ <br> $0:$ L output $1:$ Hi-Z output |
| bit46 | Output drive setting (1bit) | OUT pin driving ability setting <br> $0:$ Ability small $1:$ Ability large |
| bit47 | Source clock dividing mode (1bit) | Source clock selectable to K divider <br> $0:$ VCO output $1:$ Source clock |
| bit48 | PLL mode setting (1bit) | $0:$ Normal mode $1:$ PLL mode |
| bit49-bit55 | XIN oscillation stabilization <br> capacitance setting (7-bit) | Capacitance is selectable from 5 pF to 10 pF by 0.039 pF Step |
| bit56-bit62 | XOUT oscillation stabilization <br> capacitance setting (7-bit) | Capacitance is selectable from 5 pF to 10 pF by 0.039 pF Step |
| bit63 | Reserve |  |

## OPERATION SETTING

## - Frequency setting

Output frequency can be set by writing the internal memory to each divider parameter in the PLL block.
Internal oscillation frequency and output frequency can be calculated following expressions :
Internal oscillation frequency (fvco*) $=$ Input frequency $($ fin $) \times(\mathrm{M}+1) /(\mathrm{N}+1)$

* : Please set the fvco range from 20 MHz to 134 MHz .

Output frequency (fout*) $=$ Input frequency $($ fin $) \times(\mathrm{M}+1) /((\mathrm{N}+1) \times \mathrm{K})$
*: Please set the fout range from 1 MHz to 134 MHz .
(Setting example)
fin $=27 \mathrm{MHz}$, fout $=60 \mathrm{MHz}$
M divider parameter : 1999 ( = 7СFн) , N divider parameter : 899 ( $=383 \mathrm{H}$ ) , K divider parameter : 1 ( $=01 \mathrm{H}$ ) $27 \times(1999+1) /((899+1) \times 1)=60[\mathrm{MHz}](f v c o=27 \times(1999+1) /(899+1)=60[M H z])$
Note: Recommended value of each divider parameter is different at PLL mode and normal mode. Please refer and confirm the recommended value by our support tool. Contact the sales representatives for details on the support tools.

- Modulation frequency setting

Modulation frequency can be set by writing the internal memory to $L$ divider parameter.
The average of modulation frequency can be calculated following expressions :

$$
\frac{\text { Input frequency }}{266 \times(\mathrm{L}+1)} \quad(\mathrm{L}=1,2,3,4,5,6,7)
$$

Note: Please refer and confirm the recommended value by our support tool. Contact the sales representatives for details on the support tools.

- Modulation rate setting

Modulation rate can be selectable from no modulation, $\pm 0.25 \%, \pm 0.50 \%, \pm 0.75 \%, \pm 1.00 \%, \pm 1.25 \%, \pm 1.50 \%$, $\pm 1.75 \%$.

| bit44 | bit43 | bit42 | Modulation rate setting |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | No modulation |
| 0 | 0 | 1 | $\pm 0.25 \%$ |
| 0 | 1 | 0 | $\pm 0.50 \%$ |
| 0 | 1 | 1 | $\pm 0.75 \%$ |
| 1 | 0 | 0 | $\pm 1.00 \%$ |
| 1 | 0 | 1 | $\pm 1.25 \%$ |
| 1 | 1 | 0 | $\pm 1.50 \%$ |
| 1 | 1 | 1 | $\pm 1.75 \%$ |

## MB88R157

## - Charge Pump setting, VCO gain setting

Note: Please refer and confirm the recommended value by our support tool. Contact the sales representatives for details on the support tools.

## - OUT pin setting

OUT pin situation can be selected at OE pin "L" input.

| bit45 | OUT pin situation |
| :---: | :--- |
| 0 | "L" output |
| 1 | "Hi-Z" output |

Note : Internal oscillation circuit has been operating when OE pin is input " L ".

- Output drive ability setting

Output drive ability of OUT pin can be selected.

| bit46 | OUT pin drive ability |
| :---: | :--- |
| 0 | Small (loL $=3 \mathrm{~mA})$ |
| 1 | Large (loL $=7 \mathrm{~mA})$ |

## - Source clock dividing setting

Source clock to K divider can be selected.
When "input frequency" is selected, source clock or its divided clock can be output. But modulation setting is not enable.

| bit47 | Source clock to K divider |
| :---: | :--- |
| 0 | VCO output clock |
| 1 | Input clock (Source clock) |

Note: When "input frequency " is selected, internal oscillation circuit has been operating. About M and N divider parameter setting, please refer and confirm the recommended value by our support tool. Contact the sales representatives for details on the support tools.

## - PLL mode setting

It can be selected normal mode and PLL mode by bit48 setting in the memory map. PLL mode is good jitter specification at non modulation. When the mode is selected, it becomes non modulation setting, the resistance and capacitance value of the loop filter is changed, so oscillation specification is change.

| bit48 | Operation mode |
| :---: | :--- |
| 0 | SSCG mode |
| 1 | PLL mode |

Note: When PLL mode is selected, recommended value of $M, N, K$ divider is changed. Please refer and confirm the recommended value by our support tool. Contact the sales representatives for details on the support tools.

## MB88R157

## MEMORY ACCESS

Read/write to the built-in non-volatile memory is enabled through the serial communication with the OE pin functioned as the I/O pin.
Set for the communication protocol. Also, set the transfer speed as $1 / 512$ of the source clock.

- Asynchronous transfer mode of UART
- LSB fast
- NRZ format
- Bit length: 8 bits
- No parity
- Stop bit: 1 bit


## - Transfer sequence



OUT


1. Set the PEX pin to "L" more than 30 ms after this device is turned on, input a command from the OE pin set MB88R157 into memory access mode.(When a command is input by serial communication, data of "FDh" is sent.)
Note: When memory access is available, source clock can be output from the OUT pin.
Fix the PEX pin to "H", or fix the OE pin to "H" or "L" until command input.
2. At writing, " 00 H " is sent serially, and at reading, " 40 H " is sent.

Note: This device needs to stop outputting to the OE pin of the transferred device within $15 \mu \mathrm{~s}$ after transferring " 40 H " serially at the reading state and place it to a receivable state.
3. At writing : Send 8-byte data blocks from the lower address of the memory map in turn with more than $100 \mu \mathrm{~s}$ between each data block.
At read : This device outputs 8 -byte data blocks from the lower address of the memory map in turn.
4. Repeat the operations of 2 . and 3 . for re-writing and re-reading.

To operate the device using the written data, turn on the power again.
However, the oscillation stabilization capacitance is set simultaneously with writing to memory. When the oscillation stabilization capacitance and the crystal oscillation frequency are adjusted, change the oscillation stabilization capacitance value so that the clock output from the OUT pin is set to the desired frequency.

## MB88R157

- Interconnection example

* 1 : Set the UO pin to Hi-z to read from memory, as the UO pin serves for serial I/O.

UO : UART serial data output pin
UI : UART serial data input pin
UCK : UART serial synchronous clock I/O pin
*2 : Because the transfer rate is set to $1 / 512$ of source oscillation in MB88R157, the clock generator is used as shown in above figure, so that the transfer speed is set to $1 / 512$ of source clock in MB88R157. However, the clock generator is not needed if the transfer speed can be maintained from an internal clock of the baud rate generator of the UART.

## MB88R157

ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating |  | Unit |
| :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max |  |
| Power supply voltage* | VDD | -0.5 | + 4.0 | V |
| Input voltage* | $\mathrm{V}_{1}$ | Vss -0.5 | $\mathrm{V}_{\mathrm{DD}}+0.5$ | V |
| Output voltage* | Vo | Vss -0.5 | $V_{\text {do }}+0.5$ | V |
| Storage temperature | Tst | - 55 | + 125 | ${ }^{\circ} \mathrm{C}$ |
| Operation junction temperature | TJ | -40 | + 125 | ${ }^{\circ} \mathrm{C}$ |
| Output current | Io | - 14 | + 14 | mA |
| Overshoot | Viover | - | VDD +1.0 (tover $\leq 50 \mathrm{~ns}$ ) | V |
| Undershoot | Viunder | Vss - 1.0 (tunder $\leq 50 \mathrm{~ns}$ ) | - | V |

*: This parameter is based on $\mathrm{V}_{\mathrm{ss}}=0.0 \mathrm{~V}$
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Overshoot/Undershoot


## RECOMMENDED OPERATING CONDITONS

| $(\mathrm{V}$ ss $=0.0 \mathrm{~V}$ ) |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Parameter | Symbol | Pin name | Conditions | Value |  |  | Unit |
|  |  |  |  | Min | Typ | Max |  |
| Power supply voltage | V ${ }_{\text {d }}$ | VDD | - | 3.0 | 3.3 | 3.6 | V |
| "H" level input voltage | $\mathrm{V}_{\mathrm{H}}$ | $\begin{gathered} \text { OE, PEX, } \\ \text { XIN } \end{gathered}$ | Input slew rate for XIN pin only $3 \mathrm{~V} / \mathrm{ns}$ | VDD $\times 0.80$ | - | $V_{\text {DD }}+0.3$ | V |
| "L" level input voltage | VIL |  |  | Vss | - | $V_{D D} \times 0.20$ | V |
| Input clock duty cycle | tocı | XIN | 10 MHz to 50 MHz | 40 | 50 | 60 | \% |
| Operating temperature | Ta | - | Write to the internal non-volatile memory <br> Operating test after the re-flow | +20 | - | + 50 | ${ }^{\circ} \mathrm{C}$ |
|  |  |  | Other than those above | -20 | - | + 85 | ${ }^{\circ} \mathrm{C}$ |

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

Input clock duty cycle (tocı $=\mathrm{t}_{\mathrm{o}} / \mathrm{ta}$ )

XIN


## MB88R157

## ELECTRICAL CHARACTERISTICS

- DC Characteristics

$$
\left(\mathrm{T}_{\mathrm{a}}=-20^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C}, \mathrm{~V}_{\mathrm{DD}}=3.3 \mathrm{~V} \pm 0.3 \mathrm{~V}, \mathrm{~V}_{\mathrm{SS}}=0.0 \mathrm{~V}\right)
$$

| Parameter | Symbol | Pin name | Conditions | Value |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Typ | Max |  |
| Power supply current | Icc | VDD | 24 MHz input (Crystal), 24 MHz internal oscillation, 24 MHz output no load capacitance | - | 5.5 | 7.0 | mA |
|  | Icc2 |  | 50 MHz input clock, 134 MHz internal oscillation, 134 MHz output 15 pF load capacitance | - | - | 26 | mA |
| Output voltage | Vон | OUT | "H" level output <br> Driving voltage (low) $\mathrm{l} \mathbf{\mathrm { oH }}=-3 \mathrm{~mA}$, <br> Driving voltage (high) Іон $=-7 \mathrm{~mA}$ | $\begin{gathered} \mathrm{VDD}_{\mathrm{DD}} \\ 0.5 \end{gathered}$ | - | VDD | V |
|  | VoL |  | "L" level output Driving voltage (low) loL $=3 \mathrm{~mA}$, Driving voltage (high) loL $=7 \mathrm{~mA}$ | Vss | - | 0.4 | V |
| Pull-up resistance | Rpu | OE, PEX | - | 25 | 50 | 200 | k $\Omega$ |
| Load capacitance | Cin | $\begin{aligned} & \text { XIN, OE, } \\ & \text { PEX } \end{aligned}$ | $\begin{aligned} & \mathrm{T}_{\mathrm{a}}=+25^{\circ} \mathrm{C}, \\ & \mathrm{~V}_{\mathrm{DD}}=\mathrm{V}_{1}=0.0 \mathrm{~V}, \\ & \mathrm{f}=1 \mathrm{MHz} \end{aligned}$ | - | - | 16 | pF |

- AC characteristics (1)

$$
\left(\mathrm{T}_{\mathrm{a}}=-20^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C}, \mathrm{VDD}=3.3 \mathrm{~V} \pm 0.3 \mathrm{~V}, \mathrm{~V} \text { Ss }=0.0 \mathrm{~V}\right)
$$

| Parameter | Symbol | Pin name | Conditions |  | Value |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  | Min | Typ | Max |  |
| Crystal oscillation frequency | $\mathrm{f}_{\mathrm{x}}$ | $\begin{gathered} \text { XIN, } \\ \text { XOUT } \end{gathered}$ | Fundamental oscillation |  | 10 | - | 40 | MHz |
| Input frequency | fin | XIN | - |  | 10 | - | 40 | MHz |
| Internal oscillation frequency | fvco | - | - |  | 20 | - | 134 | MHz |
| Output frequency | fout | OUT | Operation in PLL mode and at non modulation |  | 1 | - | 134 | MHz |
|  |  |  | Operation at modulation |  | 16 | - | 134 |  |
| Output slewing rate | SR |  | 0.4 V to 2.4 V load capacitan Driving ability at 1 MHz to 60 put Driving ability at 60 MHz to output | ce 15 pF small: MHz outlarge: 134 MHz | 0.3 | - | - | V/ns |
| Output impedance | Zo |  | Driving ability | small | - | 75 | - | $\Omega$ |
|  |  |  | Driving ability | large | - | 38 | - |  |
| Output clock duty cycle | tocc |  | VCO clock ou | tput | 45 | - | 55 | \% |
|  | tocr |  | At reference clock output |  | tocl-10* | - | toci+10* |  |
| Modulation frequency (number of clocks par one modulation) | $\begin{aligned} & \text { fмод } \\ & \text { (пмоо) } \end{aligned}$ |  | - |  | $\left\lvert\, \begin{gathered} \mathrm{fin} /(224 \times \\ (\mathrm{L}+1)) \\ (224 \times(\mathrm{L}+1)) \end{gathered}\right.$ | $\begin{gathered} \text { fin/ (266× } \\ (\mathrm{L}+1)) \\ (266 \times(\mathrm{L}+1)) \end{gathered}$ | $\left\|\begin{array}{c} \operatorname{fin} /(308 \times \\ (L+1)) \\ (308 \times(L+1)) \end{array}\right\|$ | $\begin{gathered} \mathrm{kHz} \\ \text { (clks) } \end{gathered}$ |
| Power supply time | tr | VDD | 0.2 V to 3.0 V |  | 0.05 | - | 20 | ms |
| Lock-up time | tLk | OUT | - |  | - | 270/fin +5 | 270/fin+10 | ms |
| Cycle-cycle jitter | tuc |  | No load capacitance, $\mathrm{T}_{\mathrm{a}}=+25^{\circ} \mathrm{C}$ $V_{D D}=3.3 \mathrm{~V}$ | $\begin{aligned} & \text { fout } \geq \\ & 2 \mathrm{MHz} \end{aligned}$ | - | - | 100 | $\begin{aligned} & \text { ps- } \\ & \text { rms } \end{aligned}$ |
|  |  |  |  | fout< <br> 2 MHz | - | - | 150 |  |
| Output stop time from OE exit. | tod |  | $\mathrm{ta}_{\text {a }}=1 /$ fout |  | - | - | $2 \times \mathrm{ta}_{\text {a }}$ | ns |
| Output start time after OE entry | toe |  | $\mathrm{ta}_{\text {a }}=1 /$ fout |  | - | - | $2 \times \mathrm{ta}$ | ns |

*: The duty cycle value (tocr) of the source clock output depends on the duty cycle of input clock tocl. Either case of $A$ or $B$ will be guaranteed.
A. Resonator
: Oscillating with the resonator connected with XIN, XOUT
B. External clock input : The input level is Full - swing (Vss - VDD).

## DEFINITION of MODULATION FREQUENCY and NUMBER of INPUT CLOCKS PER MODULATION



This product contains the modulation period to realize the efficient EMI reduction.
The modulation period $\mathrm{F}_{\text {mod }}$ depends on the input frequency and changes between $\mathrm{Fmod}_{\text {( }}$ (Min) and Fmod (Max). Furthermore, the typical value of the electrical characteristics is equivalent to the average value of the modulation period Fмод.

## TURNING ON POWER SUPPLY AND LOCK-UP TIME



## OUTPUT CLOCK DUTY CYCLE ( $\mathbf{t o c c}=\mathbf{t}_{\mathrm{b}} / \mathrm{t}_{\mathrm{a}}$ )



## INPUT FREQUENCY ( $\mathrm{fin}_{\mathrm{in}}=\mathbf{1} / \mathrm{t}_{\mathrm{in}}$ )



## OUTPUT SLEW RATE (SR)



Note: $\mathrm{SR}=(2.4-0.4) / \mathrm{tr}_{\mathrm{r}}, \mathrm{SR}=(2.4-0.4) / \mathrm{t}_{\mathrm{t}}$

CYCLE-CYCLE JITTER ( $\left.\mathbf{t}_{\mathrm{sc}}=\left|\mathrm{t}_{\mathrm{n}}-\mathbf{t}_{\mathrm{n}+1}\right|\right)$


## MB88R157

## OUTPUT TIMING AT OE CHANGE

- Output stop time from OE exit

- Output start time after OE entry



## MB88R157

- AC characteristics (2) (Serial interface timing)

| Parameter | Symbol | Pin name | Conditions | Value |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Typ | Max |  |
| Cycle time of transfer and receiver | tscyc | OE | - | $\begin{gathered} (\operatorname{tin} \times 512) \\ \times 0.93 \end{gathered}$ | tin $\times 512$ | $\begin{gathered} (\operatorname{tin} \times 512) \\ \times 1.025 \end{gathered}$ | $\mu \mathrm{S}$ |
| Read operation Read command receive $\rightarrow$ OE in read data output | troo |  | - | 15 | - | - | $\mu \mathrm{S}$ |
| Read operation <br> Final read data output $\rightarrow$ OE pin input mode exchanged | totı |  | - | - | - | 65 | $\mu \mathrm{s}$ |

## - Command / write data transfer



- Read operation



## INTERCONNECTION CIRCUIT EXAMPLE



C1 : Capacitor of $10 \mu \mathrm{~F}$ or higher
C2 : Capacitor of about $0.01 \mu \mathrm{~F}$ (connect a capacitor of good high frequency property (ex. laminated ceramic capacitor) to close to this device)
R1 : Impedance matching resistor for board pattern

## CRYSTAL OSCILLATION CIRCUIT

The figure below shows the connection example about general resonator. The oscillation circuit has the built-in feedback resistor ( $500 \mathrm{k} \Omega$ ) and oscillation stabilization capacitance (C1 and C2).
C1 and C2 value can be changeable by setting bit49 to bit55 and bit56 to bit62 in memory. It is necessary to set suitable parameter for each resonator.
To use an external clock signal (without using the resonator), input the clock signal to the XIN pin with the XOUT pin connected to nothing.


> | Fundamental resonator |
| :--- | :--- |

## MB88R157

## ORDERING INFORMATION

| Part number | Package |
| :--- | :---: |
| MB88R157PNF-G-JNE1 | 8-pin plastic SOP <br> (FPT-8P-M02) |
| MB88R157PNF-G-JN-ERE1 |  |

## MB88R157

## PACKAGE DIMENSION

| 8-pin plastic SOP | Lead pitch | 1.27 mm |
| :---: | :---: | :---: |
| Package width $\times$ <br> package length | $3.9 \times 5.05 \mathrm{~mm}$ |  |
|  | Geallwing shape | Plastic mold |
|  | Wounting height | 1.75 mm MAX |
|  |  | 0.06 g |

8-pin plastic SOP
(FPT-8P-M02)

$\square$

Note 1) *1: These dimensions include resin protrusion.
Note 2) *2 : These dimensions do not include resin protrusion. Note 3) Pins width and pins thickness include plating thickness. Note 4) Pins width do not include tie bar cutting remainder.
$\rightarrow \int \frac{0.22_{-0.07}^{+0.03}}{\left(.009_{-.003}^{.001}\right)}$


Dimensions in mm (inches) Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL. http://edevice.fujitsu.com/package/en-search/

MEMO

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