72 Mb (2M x 36 & 4M x 18)
QUADP (Burst of 4) Synchronous SRAMs

May 2009

Features

- 2M x 36 or 4M x 18.
- On-chip delay-locked loop (DLL) for wide data valid window.
- Separate read and write ports with concurrent read and write operations.
- Synchronous pipeline read with late write operation.
- Double data rate (DDR) interface for read and write input ports.
- Fixed 4-bit burst for read and write operations.
- Clock stop support.
- Two input clocks (K and $\overline{K}$) for address and control registering at rising edges only.
- Two echo clocks (CQ and $\overline{CQ}$) that are delivered simultaneously with data.
- +1.8V core power supply and 1.5, 1.8V V_{DDQ}, used with 0.75, 0.9V V_{REF}.
- HSTL input and output levels.
- Registered addresses, write and read controls, byte writes, data in, and data outputs.
- Full data coherency.
- Boundary scan using limited set of JTAG 1149.1 functions.
- Byte write capability.
- Fine ball grid array (FBGA) package
  - 15mm x 17mm body size
  - 1mm pitch
  - 165-ball (11 x 15) array
- Programmable impedance output drivers via 5x user-supplied precision resistor.

Description

The 72Mb IS61QDPB42M36 and IS61QDPB44M18 are synchronous, high-performance CMOS static random access memory (SRAM) devices. These SRAMs have separate I/Os, eliminating the need for high-speed bus turnaround. The rising edge of K clock initiates the read/write operation, and all internal operations are self-timed. Refer to the *Timing Reference Diagram for Truth Table* on page 8 for a description of the basic operations of these QUADP (Burst of 4) SRAMs.

Read and write addresses are registered on alternating rising edges of the K clock. Reads and writes are performed in double data rate. The following are registered internally on the rising edge of the K clock:

- Read/write address
- Read enable
- Write enable
- Byte writes for burst addresses 1 and 3
- Data-in for burst addresses 1 and 3

The following are registered on the rising edge of the $\overline{K}$ clock:

- Byte writes for burst addresses 2 and 4
- Data-in for burst addresses 2 and 4

Byte writes can change with the corresponding data-in to enable or disable writes on a per-byte basis. An internal write buffer enables the data-ins to be registered one cycle after the write address. The first data-in burst is clocked one cycle later than the write command signal, and the second burst is timed to the following rising edge of the $\overline{K}$ clock. Two full clock cycles are required to complete a write operation.

The device is operated with a single +1.8V power supply and is compatible with HSTL I/O interfaces.

x36 FBGA Pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/SA*	SA	$\overline{W}$	$\overline{BW_2}$	$\overline{K}$	$\overline{BW_1}$	$\overline{R}$	SA	NC/SA*	CQ
B	Q27	Q18	D18	SA	$\overline{BW_3}$	K	$\overline{BW_0}$	SA	D17	Q17	Q8
C	D27	Q28	D19	V_{SS}	SA	NC	SA	V_{SS}	D16	Q7	D8
D	D28	D20	Q19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q16	D15	D7
E	Q29	D29	Q20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	Q15	D6	Q6
F	Q30	Q21	D21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D14	Q14	Q5
G	D30	D22	Q22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q13	D13	D5
H	$\overline{Doff}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	D31	Q31	D23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D12	Q4	D4
K	Q32	D32	Q23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q12	D3	Q3
L	Q33	Q24	D24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	D11	Q11	Q2
M	D33	Q34	D25	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D10	Q1	D2
N	D34	D26	Q25	V_{SS}	SA	SA	SA	V_{SS}	Q10	D9	D1
P	Q35	D35	Q26	SA	SA	NC	SA	SA	Q9	D0	Q0
R	TDO	TCK	SA	SA	SA	NC	SA	SA	SA	TMS	TDI

Note: *The following pins are reserved for higher densities: 10A for 144Mb, and 2A for 288Mb. QVLD pin (6P) is not supported.

x18 FBGA Pinout (Top View)

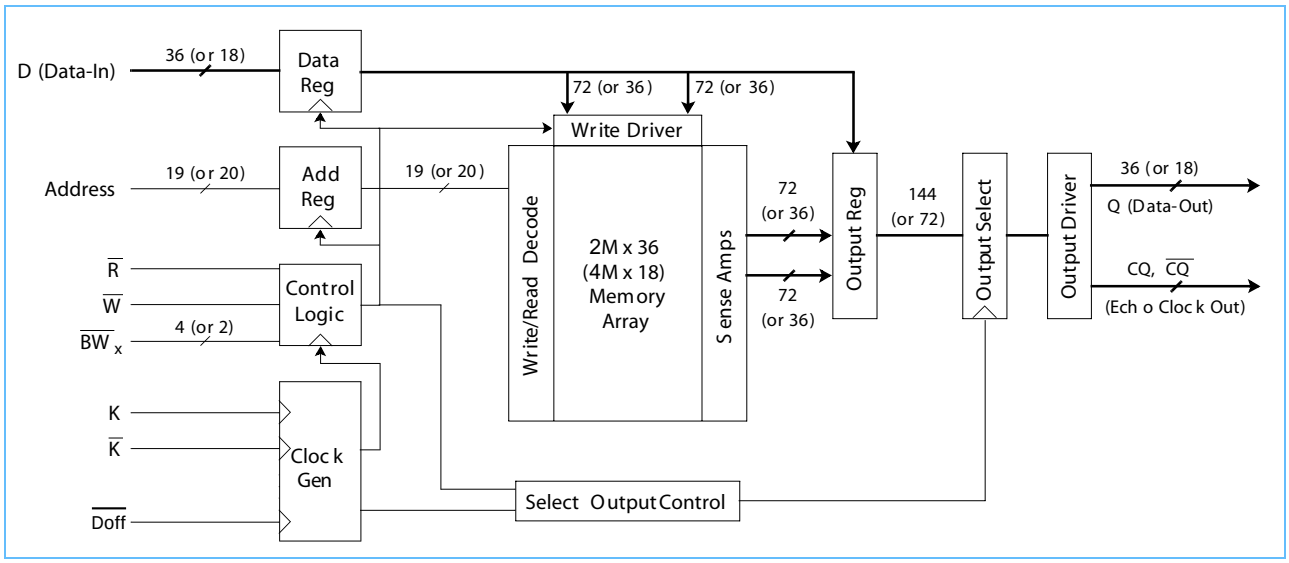
	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/SA*	SA	$\overline{W}$	$\overline{BW_1}$	$\overline{K}$	NC	$\overline{R}$	SA	SA	CQ
B	NC	Q9	D9	SA	NC	K	$\overline{BW_0}$	SA	NC	NC	Q8
C	NC	NC	D10	V_{SS}	SA	NC	SA	V_{SS}	NC	Q7	D8
D	NC	D11	Q10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D7
E	NC	NC	Q11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	D5
H	$\overline{Doff}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	D14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q2
M	NC	NC	D16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q1	D2
N	NC	D17	Q16	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	D1
P	NC	NC	Q17	SA	SA	NC	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	NC	SA	SA	SA	TMS	TDI

Note: *The following pins are reserved for higher densities: 2A for 144Mb. QVLD pin (6P) is not supported.

Pin Description

Symbol	Pin Number	Description
K, $\overline{K}$.	6B, 6A	Input clock.
CQ, $\overline{CQ}$	11A, 1A	Output echo clock.
$\overline{Doff}$	1H	DLL disable when low.
SA	3A, 9A, 4B, 8B, 5C, 7C, 5N, 6N, 7N, 4P, 5P, 7P, 8P, 3R, 4R, 5R, 7R, 8R, 9R	2M x 36 address inputs.
SA	3A, 9A, 10A, 4B, 8B, 5C, 7C, 5N, 6N, 7N, 4P, 5P, 7P, 8P, 3R, 4R, 5R, 7R, 8R, 9R	4M x 18 address inputs.
D0–D8 D9–D17 D18–D26 D27–D35	10P, 11N, 11M, 10K, 11J, 11G, 10E, 11D, 11C 10N, 9M, 9L, 9J, 10G, 9F, 10D, 9C, 9B 3B, 3C, 2D, 3F, 2G, 3J, 3L, 3M, 2N 1C, 1D, 2E, 1G, 1J, 2K, 1M, 1N, 2P	2M x 36 data inputs.
Q0–Q8 Q9–Q17 Q18–Q26 Q27–Q35	11P, 10M, 11L, 11K, 10J, 11F, 11E, 10C, 11B 9P, 9N, 10L, 9K, 9G, 10F, 9E, 9D, 10B 2B, 3D, 3E, 2F, 3G, 3K, 2L, 3N, 3P 1B, 2C, 1E, 1F, 2J, 1K, 1L, 2M, 1P	2M x 36 data outputs.
D0–D8 D9–D17	10P, 11N, 11M, 10K, 11J, 11G, 10E, 11D, 11C 3B, 3C, 2D, 3F, 2G, 3J, 3L, 3M, 2N	4M x 18 data inputs.
Q0–Q8 Q9–Q17	11P, 10M, 11L, 11K, 10J, 11F, 11E, 10C, 11B 2B, 3D, 3E, 2F, 3G, 3K, 2L, 3N, 3P	4M x 18 data outputs.
$\overline{W}$	4A	Write control, active low.
$\overline{R}$	8A	Read control, active low.
$\overline{BW}_0$, $\overline{BW}_1$, $\overline{BW}_2$, $\overline{BW}_3$	7B, 7A, 5A,5B	2M x 36 byte write control, active low.
$\overline{BW}_0$, $\overline{BW}_1$	7B, 5A	4M x 18 byte write control, active low.
V_{REF}	2H, 10H	Input reference level.
V_{DD}	5F, 7F, 5G, 7G, 5H, 7H, 5J, 7J, 5K, 7K	Power supply.
V_{DDQ}	4E,8E,4F,8F,4G,8G,3H,4H,8H,9H,4J,8J,4K,8K,4L,8L	Output power supply.
V_{SS}	4C, 8C, 4D, 5D, 6D, 7D, 8D, 5E, 6E, 7E, 6F, 6G, 6H, 6J, 6K, 5L, 6L, 7L, 4M, 5M, 6M, 7M, 8M, 4N, 8N	Ground.
ZQ	11H	Output driver impedance control.
TMS, TDI, TCK	10R, 11R, 2R	IEEE 1149.1 test inputs (1.8V LVTTL levels).
TDO	1R	IEEE 1149.1 test output (1.8V LVTTL level).
NC for x36	2A, 10A, 6C, 6P, 6R	
NC for x18	2A, 7A, 1B, 5B, 9B, 10B, 1C, 2C, 6C, 9C, 1D, 9D, 10D, 1E, 2E, 9E, 1F, 9F, 10F, 1G, 9G, 10G, 1J, 2J, 9J, 1K, 2K, 9K, 1L, 9L, 10L, 1M, 2M, 9M, 1N, 9N, 10N, 1P, 2P, 6P, 9P, 6R	

Block Diagram



SRAM Features

Read Operations

The SRAM operates continuously in a burst-of-four mode. Read cycles are started by registering $\overline{R}$ in active low state at the rising edge of the K clock. $\overline{R}$ can be activated every other cycle because two full cycles are required to complete the burst of four in DDR mode. A set of free-running echo clocks, CQ and $\overline{CQ}$, are produced internally with timings identical to the data-outs. The echo clocks can be used as data capture clocks by the receiver device.

The data corresponding to the first address is clocked 2.5 cycles later by the rising edge of the $\overline{K}$ clock. The data corresponding to the second burst is clocked 3 cycles later by the following rising edge of the K clock. The third data-out is clocked by the subsequent rising edge of the $\overline{K}$ clock, and the fourth data-out is clocked by the subsequent rising edge of the K clock.

A NOP operation ($\overline{R}$ is high) does not terminate the previous read.

Write Operations

Write operations can also be initiated at every other rising edge of the K clock whenever $\overline{W}$ is low. The write address is provided simultaneously. Again, the write always occurs in bursts of four.

The write data is provided in a ‘late write’ mode; that is, the data-in corresponding to the first address of the burst, is presented 1 cycle later or at the rising edge of the following K clock. The data-in corresponding to the second write burst address follows next, registered by the rising edge of $\overline{K}$. The third data-in is clocked by the subsequent rising edge of the K clock, and the fourth data-in is clocked by the subsequent rising edge of the $\overline{K}$ clock.

The data-in provided for writing is initially kept in write buffers. The information in these buffers is written into the array on the third write cycle. A read cycle to the last two write addresses produces data from the write buffers. The SRAM maintains data coherency.

During a write, the byte writes independently control which byte of any of the four burst addresses is written (see *X18/X36 Write Truth Tables* on pages 10 - 11 and *Timing Reference Diagram for Truth Table* on page 8).

Whenever a write is disabled ($\overline{W}$ is high at the rising edge of K), data is not written into the memory.

RQ Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and V_{SS} to enable the SRAM to adjust its output driver impedance. The value of RQ must be 5x the value of the intended line impedance driven by the SRAM. For example, an RQ of 250Ω results in a driver impedance of 50Ω. The allowable range of RQ to guarantee impedance matching is between 175Ω and 350Ω, with the tolerance described in *Programmable Impedance Output Driver DC Electrical Characteristics* on page 16. The RQ resistor should be placed less than two inches away from the ZQ ball on the SRAM module. The capacitance of the loaded ZQ trace must be less than 3 pF.

The ZQ pin can also be directly connected to V_{DDQ} to obtain a minimum impedance setting. ZQ must never be connected to V_{SS}.

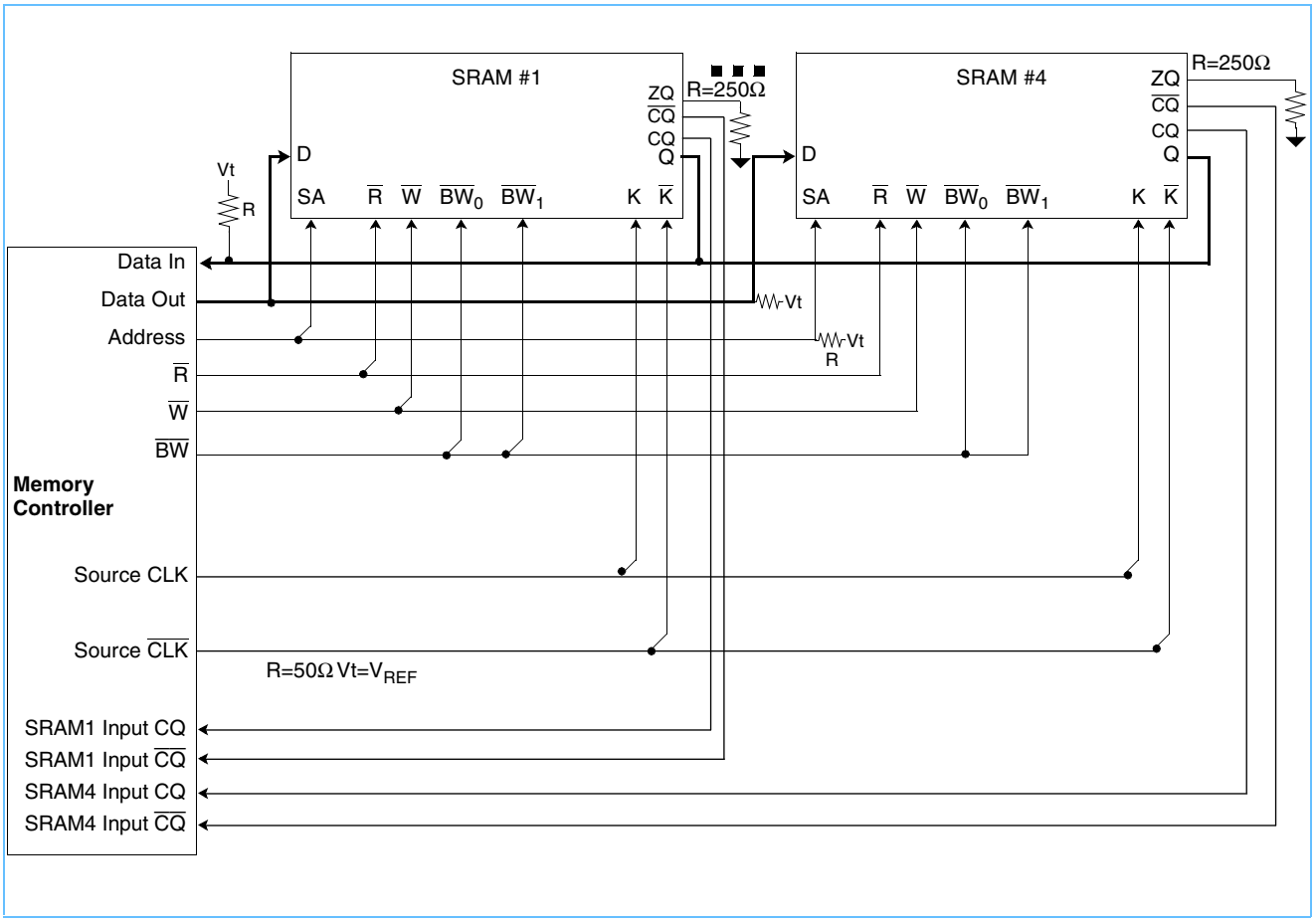
Programmable Impedance and Power-Up Requirements

Periodic readjustment of the output driver impedance is necessary as the impedance is greatly affected by drifts in supply voltage and temperature. At power-up, the driver impedance is in the middle of allowable impedances values. The final impedance value is achieved within 2048 clock cycles.

Depth Expansion

Separate input and output ports enable easy depth expansion, as each port can be selected and deselected independently. Read and write operations can occur simultaneously without affecting each other. Also, all pending read and write transactions are always completed prior to deselecting the corresponding port.

Application Example



Power-Up and Power-Down Sequences

The following sequence is used for power-up:

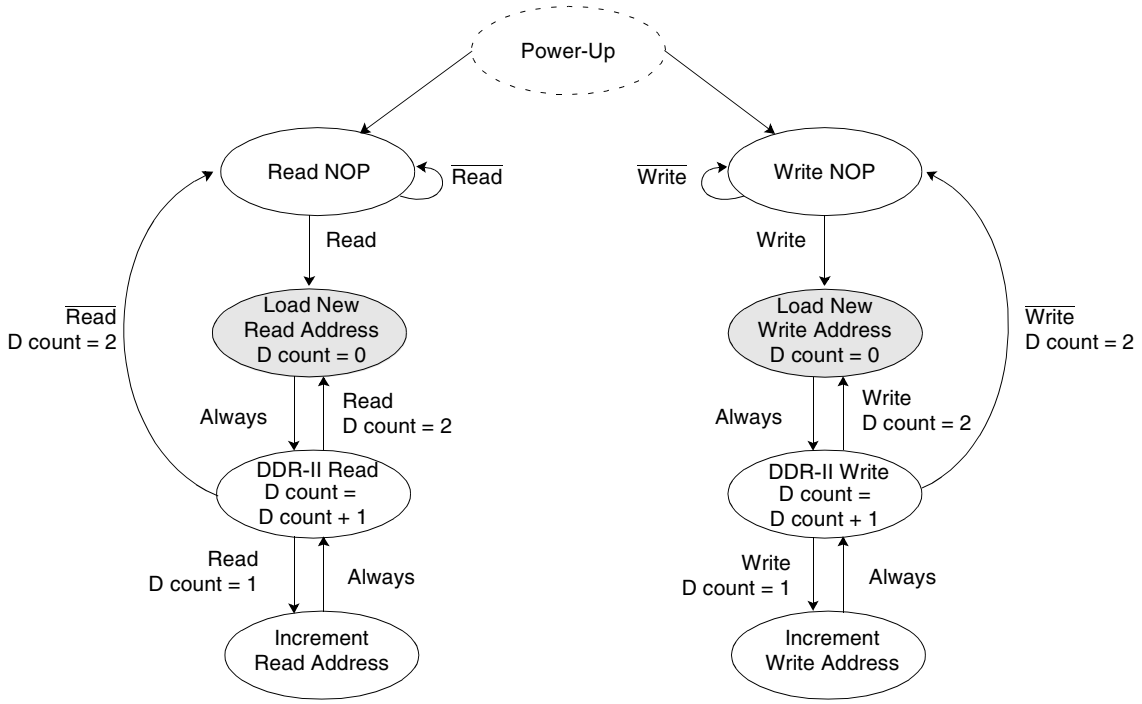
1. The power supply inputs must be applied in the following order while keeping $\overline{\text{Doff}}$ in LOW logic state:

    1) VDD
    2) VDDQ
    3) VREF

2. Start applying stable clock inputs (K, $\overline{\text{K}}$, C, and $\overline{\text{C}}$).
3. After clock signals have stabilized, change $\overline{\text{Doff}}$ to HIGH logic state.
4. Once the $\overline{\text{Doff}}$ is switched to HIGH logic state, wait an additional 1024 clock cycles to lock the DLL.

NOTES:
1. The power-down sequence must be done in reverse of the power-up sequence.
2. VDDQ can be allowed to exceed VDD by no more than 0.6V.
3. VREF can be applied concurrently with VDDQ.

State Diagram

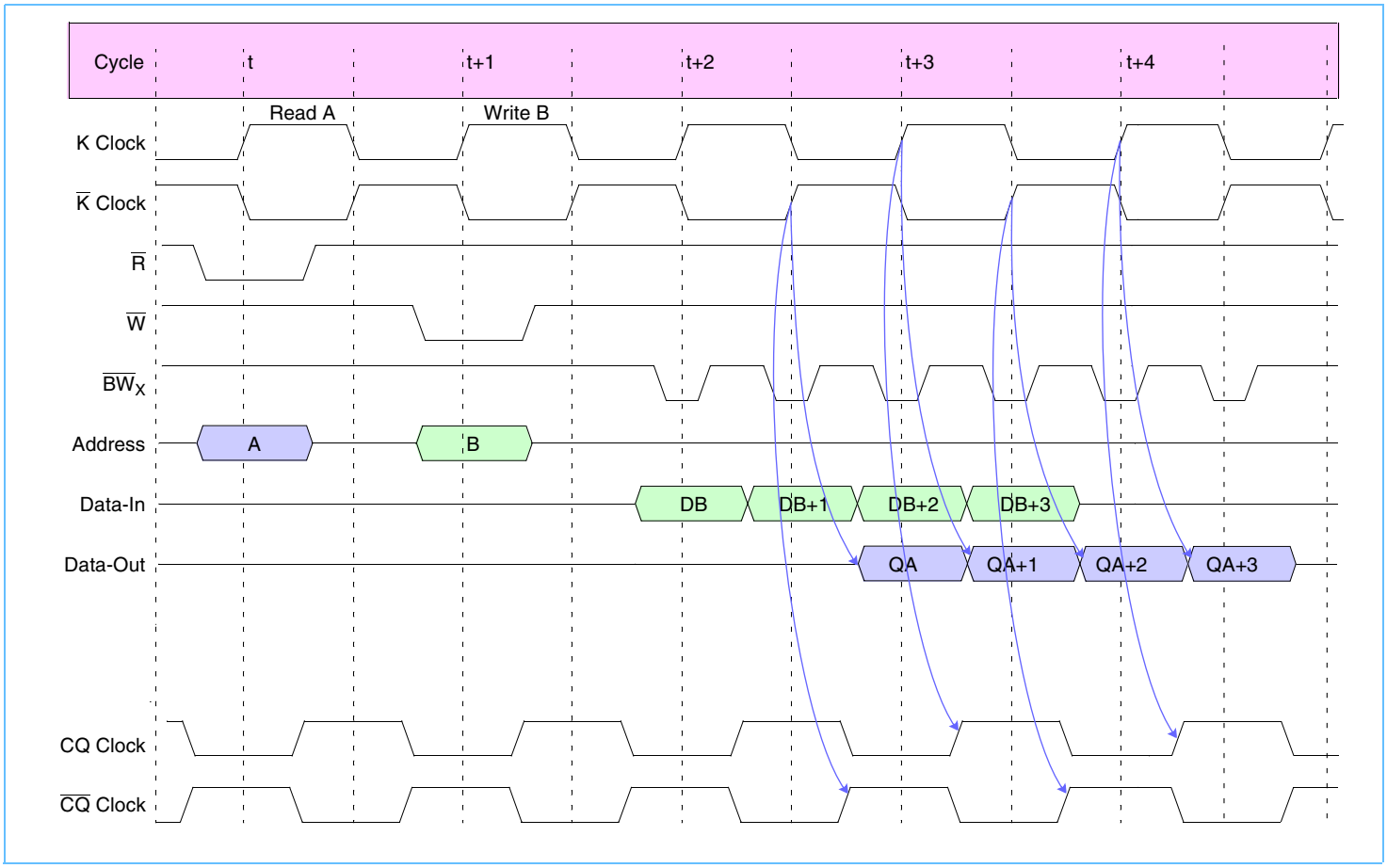


Notes: 1. Internal burst counter is fixed as four-bit linear; that is, when first address is A0+0, next internal burst addresses are A0+1, A0+2, and A0+3

2. *Read* refers to read active status with $\overline{R}$ = low. *Read* refers to read inactive status with $\overline{R}$ = high.
3. *Write* refers to write active status with $\overline{W}$ = low. *Write* refers to write inactive status with $\overline{W}$ = high.
4. The read and write state machines can be active simultaneously.
5. State machine control timing sequence is controlled by K.

The *Timing Reference Diagram for Truth Table* on page 8 is helpful in understanding the clock and write truth tables, as it shows the cycle relationship between clocks, address, data in, data out, and controls. All read and write commands are issued at the beginning of cycle “t”.

Timing Reference Diagram for Truth Table



Clock Truth Table (Use the following table with the *Timing Reference Diagram for Truth Table*.)

Mode	Clock	Controls		Data In				Data Out			
	K	$\overline{R}$	$\overline{W}$	D_B	D_{B+1}	D_{B+2}	D_{B+3}	Q_A	Q_{A+1}	Q_{A+2}	Q_{A+3}
Stop Clock	Stop	X	X	Previous State	Previous State	Previous State	Previous State	Previous State	Previous State	Previous State	Previous State
No Operation (NOP)	L→H	H	H	X	X	X	X	High-Z	High-Z	High-Z	High-Z
Read B	L →H	L	X	X	X	X	X	Dout at $\overline{K}$ (t + 2.5)	Dout at K (t + 3.0)	Dout at $\overline{K}$ (t + 3.5)	Dout at K (t + 4.0)
Write A	L →H	X	L	Din at K (t + 1)	Din at $\overline{K}$ (t + 1.5)	Din at K (t + 2)	Din at $\overline{K}$ (t + 2.5)	X	X	X	X

Notes:

1. Internal burst counter is always fixed as four-bit.
2. X = “don’t care”; H = logic “1”; L = logic “0”.
3. A read operation is started when control signal $\overline{R}$ is active low
4. A write operation is started when control signal $\overline{W}$ is active low. Before entering into stop clock, all pending read and write commands must be completed.
5. Consecutive read or write operations can be started only at every other K clock rising edge. If two read or write operations are issued in consecutive K clock rising edges, the second one will be ignored.
6. If both $\overline{R}$ and $\overline{W}$ are active low after a NOP operation, the write operation will be ignored.
7. For timing definitions, refer to the *AC Characteristics* on page 17. Signals must have AC specifications at timings indicated in parenthesis with respect to switching clocks K and $\overline{K}$.

X36 Write Truth Table Use the following table with the *Timing Reference Diagram for Truth Table* on page 8.

Operation	K(t+1)	$\overline{K}$(t+1.5)	K(t+2)	$\overline{K}$(t+2.5)	$\overline{BW}_0$	$\overline{BW}_1$	$\overline{BW}_2$	$\overline{BW}_3$	D_B	D_{B+1}	D_{B+2}	D_{B+3}
Write Byte 0	L→H				L	H	H	H	D0-8 (t+1)			
Write Byte 1	L→H				H	L	H	H	D9-17 (t+1)			
Write Byte 2	L→H				H	H	L	H	D18-26 (t+1)			
Write Byte 3	L→H				H	H	H	L	D27-35 (t+1)			
Write All Bytes	L→H				L	L	L	L	D0-35 (t+1)			
Abort Write	L→H				H	H	H	H	Don't care			
Write Byte 0		L→H			L	H	H	H		D0-8 (t+1.5)		
Write Byte 1		L→H			H	L	H	H		D9-17 (t+1.5)		
Write Byte 2		L→H			H	H	L	H		D18-26 (t+1.5)		
Write Byte 3		L→H			H	H	H	L		D27-35 (t+1.5)		
Write All Bytes		L→H			L	L	L	L		D0-35 (t+1.5)		
Abort Write		L→H			H	H	H	H		Don't care		
Write Byte 0			L→H		L	H	H	H			D0-8 (t+2)	
Write Byte 1			L→H		H	L	H	H			D9-17 (t+2)	
Write Byte 2			L→H		H	H	L	H			D18-26 (t+2)	
Write Byte 3			L→H		H	H	H	L			D27-35 (t+2)	
Write All Bytes			L→H		L	L	L	L			D0-35 (t+2)	
Abort Write			L→H		H	H	H	H			Don't care	
Write Byte 0				L→H	L	H	H	H				D0-8 (t+2.5)
Write Byte 1				L→H	H	L	H	H				D9-17 (t+2.5)
Write Byte 2				L→H	H	H	L	H				D18-26 (t+2.5)
Write Byte 3				L→H	H	H	H	L				D27-35 (t+2.5)
Write All Bytes				L→H	L	L	L	L				D0-35 (t+2.5)
Abort Write				L→H	H	H	H	H				Don't care

Notes;

1. For all cases, $\overline{W}$ needs to be active low during the rising edge of K occurring at time t.
2. For timing definitions refer to the *AC Characteristics* on page 17. Signals must have AC specifications with respect to switching clocks $\overline{K}$ and K.

X18 Write Truth Table Use the following table with the *Timing Reference Diagram for Truth Table* on page 8.

Operation	K(t+1)	$\overline{K}$(t+1.5)	K(t+2)	$\overline{K}$(t+2.5)	$\overline{BW}_0$	$\overline{BW}_1$	D_B	D_{B+1}	D_{B+2}	D_{B+3}
Write Byte 0	L→H				L	H	D0-8 (t+1)			
Write Byte 1	L→H				H	L	D9-17 (t+1)			
Write All Bytes	L→H				L	L	D0-17 (t+1)			
Abort Write	L→H				H	H	Don't care			
Write Byte 0		L→H			L	H		D0-8 (t+1.5)		
Write Byte 1		L→H			H	L		D9-17 (t+1.5)		
Write All Bytes		L→H			L	L		D0-17 (t+1.5)		
Abort Write		L→H			H	H		Don't care		
Write Byte 0			L→H		L	H			D0-8 (t+2)	
Write Byte 1			L→H		H	L			D9-17 (t+2)	
Write All Bytes			L→H		L	L			D0-17 (t+2)	
Abort Write			L→H		H	H			Don't care	
Write Byte 0				L→H	L	H				D0-8 (t+2.5)
Write Byte 1				L→H	H	L				D9-17 (t+2.5)
Write All Bytes				L→H	L	L				D0-17 (t+2.5)
Abort Write				L→H	H	H				Don't care

Notes;

1. For all cases. $\overline{W}$ needs to be active low during the rising edge of K occurring at time t.
2. For timing definitions refer to the *AC Characteristics* on page 17. Signals must have AC specifications with respect to switching clocks $\overline{K}$ and K.

Absolute Maximum Ratings

Item	Symbol	Rating	Units
Power supply voltage	V_{DD}	-0.5 to 2.9V	V
Output power supply voltage	V_{DDQ}	-0.5 to 2.9V	V
Input voltage	V_{IN}	-0.5 to VDD+0.3V	V
Data out voltage	V_{DOUT}	-0.5 to 2.6	V
Operating temperature	T_A	0 to 70	°C
Junction temperature	T_J	110	°C
Storage temperature	T_{STG}	-55 to +125	°C

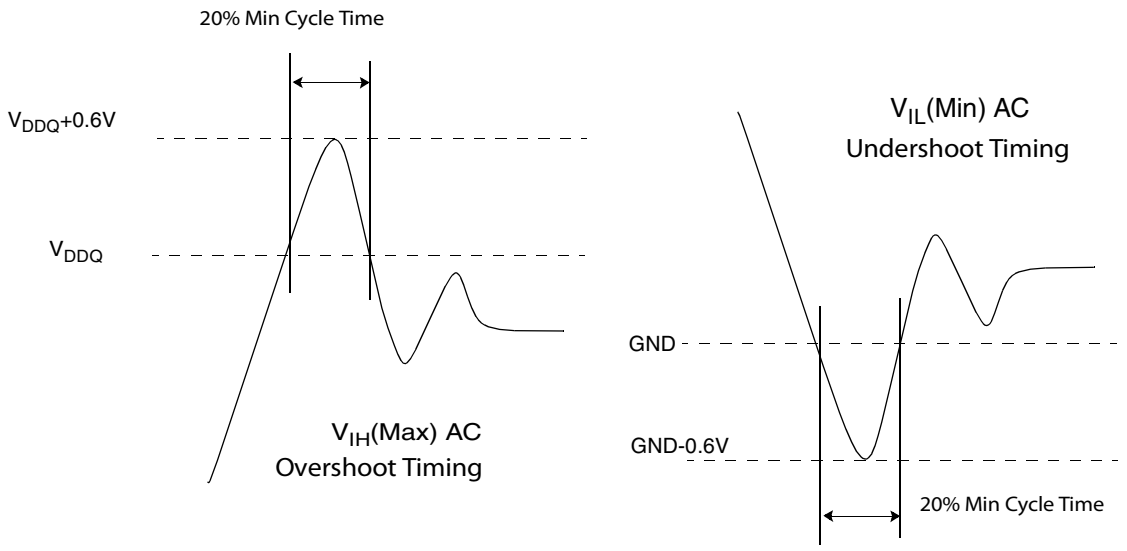
Note: Stresses greater than those listed in this table can cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this datasheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to +70° C)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Supply voltage	V_{DD}	1.8 - 5%		1.8 + 5%	V	1
Output driver supply voltage	V_{DDQ}	1.4		1.9	V	1
Input high voltage	V_{IH}	V_{REF} +0.1		V_{DDQ} + 0.2	V	1, 2
Input low voltage	V_{IL}	-0.2		V_{REF} - 0.1	V	1, 3
Input reference voltage	V_{REF}	0.68		0.95	V	1, 5
Clocks signal voltage	$V_{IN - CLK}$	-0.2		V_{DDQ} + 0.2	V	1, 4

1. All voltages are referenced to V_{SS}. All V_{DD}, V_{DDQ}, and V_{SS} pins must be connected.
2. V_{IH}(Max) AC = See *0vershoot and Undershoot Timings*.
3. V_{IL}(Min) AC = See *0vershoot and Undershoot Timings*.
4. V_{IN-CLK} specifies the maximum allowable DC excursions of each clock (K and $\overline{K}$).
5. Peak-to-peak AC component superimposed on V_{REF} may not exceed 5% of V_{REF}.

0vershoot and Undershoot Timings



PBGA Thermal Characteristics

Item	Symbol	Rating	Units
Thermal resistance junction to ambient (airflow = 1m/s)	RΘJA	18.6	°C/W
Thermal resistance junction to case	RΘJC	4.3	°C/W
Thermal resistance junction to pins	RΘJB	1.77	°C/W

Capacitance (T_A = 0 to + 70 C, V_{DD} = 1.8V -5%, +5%, f = 1MHz)

Parameter	Symbol	Test Condition	Maximum	Units
Input capacitance	C_{IN}	V_{IN} = 0V	4	pF
Data-in capacitance (D0–D35)	C_{DIN}	V_{DIN} = 0V	4	pF
Data-out capacitance (Q0–Q35)	C_{OUT}	V_{OUT} = 0V	4	pF
Clocks Capacitance (K, $\overline{K}$)	C_{CLK}	V_{CLK} = 0V	4	pF

DC Electrical Characteristics (T_A = 0 to + 70 C, V_{DD} = 1.8V -5%, +5%)

Parameter	Symbol	Minimum	Maximum	Units	Notes
x36 average power supply operating current (I_{OUT} = 0, V_{IN} = V_{IH} or V_{IL})	I_{DD25} I_{DD27} I_{DD30} I_{DD33}	—	1050 950 850 750	mA	1
x18 average power supply operating current (I_{OUT} = 0, V_{IN} = V_{IH} or V_{IL})	I_{DD25} I_{DD27} I_{DD30} I_{DD33}	—	1000 900 800 700	mA	1
Power supply standby current ($\overline{R}$ = V_{IH}, $\overline{W}$ = V_{IH}. All other inputs = V_{IH} or V_{IH}, I_{IH} = 0)	I_{SB}	—	400	mA	1
Input leakage current, any input (except JTAG) (V_{IN} = V_{SS} or V_{DD})	I_{LI}	-2	+2	µA	
Output leakage current (V_{OUT} = V_{SS} or V_{DDQ}, Q in High-Z)	I_{LO}	-2	+2	µA	
Output “high” level voltage (I_{OH} = -6mA)	V_{OH}	V_{DDQ} -.4	V_{DDQ}	V	2, 3
Output “low” level voltage (I_{OL} = +6mA)	V_{OL}	V_{SS}	V_{SS}+.4	V	2, 3
JTAG leakage current (V_{IN} = V_{SS} or V_{DD})	I_{LIJTAG}	-100	+100	A	4

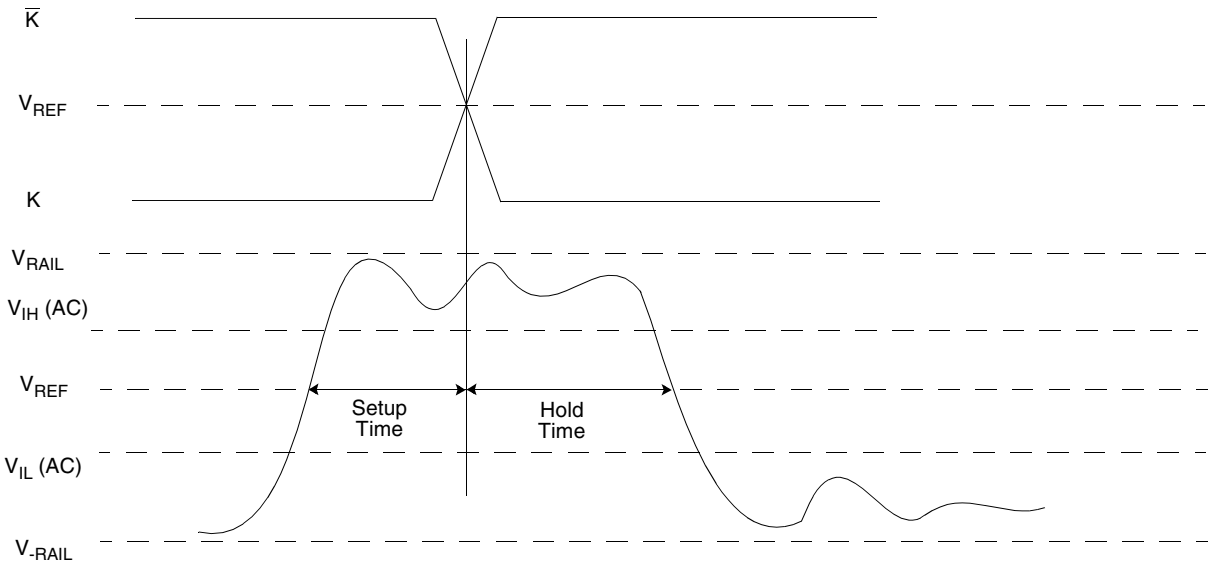
1. I_{OUT} = chip output current.
2. Minimum impedance output driver.
3. JEDEC Standard JESD8-6 Class 1 compatible.
4. For JTAG inputs only.

Typical AC Input Characteristics

Item	Symbol	Minimum	Maximum	Notes
AC input logic high	V_{IH} (ac)	V_{REF} + 0.2		1, 2, 3, 4
AC input logic low	V_{IL} (ac)		V_{REF} - 0.2	1, 2, 3, 4
Clock input logic high (K, $\overline{K}$, C, $\overline{C}$)	V_{IH-CLK} (ac)	V_{REF} + 0.2		1, 2, 3
Clock input logic low (K, $\overline{K}$, C, $\overline{C}$)	V_{IL-CLK} (ac)		V_{REF} - 0.2	1, 2, 3

1. The peak-to-peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF}.
2. Performance is a function of V_{IH} and V_{IL} levels to clock inputs.
3. See the *AC Input Definition* diagram.
4. See the *AC Input Definition* diagram. The signals should swing monotonically with no steps rail-to-rail with input signals never ringing back past VIH (AC) and VIL (AC) during the input setup and input hold window. VIH (AC) and VIL (AC) are used for timing purposes only.

AC Input Definition



Programmable Impedance Output Driver DC Electrical Characteristics

(T_A = 0 to +70° C, V_{DD} = 1.8V -5%, +5%, V_{DDQ} = 1.5, 1.8V)

Parameter	Symbol	Minimum	Maximum	Units	Notes
Output “high” level voltage	V_{OH}	V_{DDQ} / 2	V_{DDQ}	V	1, 3
Output “low” level voltage	V_{OL}	V_{SS}	V_{DDQ} / 2	V	2, 3

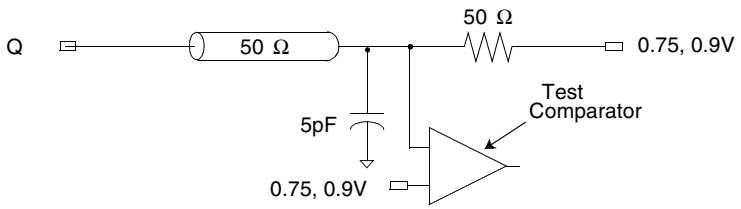
1. $I_{OH} = \left(\frac{VDDQ}{2}\right) / \left(\frac{RQ}{5}\right) \pm 15\%$ @ $V_{OH} = V_{DDQ} / 2$ For: $175\Omega \leq RQ \leq 350\Omega$
2. $I_{OL} = \left(\frac{VDDQ}{2}\right) / \left(\frac{RQ}{5}\right) \pm 15\%$ @ $V_{OL} = V_{DDQ} / 2$ For: $175\Omega \leq RQ \leq 350\Omega$
3. Parameter tested with RQ = 250Ω and V_{DDQ} = 1.5V.

AC Test Conditions (T_A = 0 to +70° C, V_{DD} = 1.8V -5%, +5%, V_{DDQ} = 1.5, 1.8V)

Parameter	Symbol	Conditions	Units	Notes
Output driver supply voltage	V_{DDQ}	1.5, 1.8	V	
Input high level	V_{IH}	V_{REF}+0.5	V	
Input Low Level	V_{IL}	V_{REF}-0.5	V	
Input reference voltage	V_{REF}	0.75, 0.9	V	
Input rise time	T_R	0.35	ns	
Input fall time	T_F	0.35	ns	
Output timing reference level		V_{REF}	V	
Clocks reference level		V_{REF}	V	
Output load conditions				1, 2

1. See *AC Test Loading*.
2. Parameter tested with RQ = 250Ω and V_{DDQ} = 1.5V.

AC Test Loading



AC CHARACTERISTICS (VDD = 1.8V 0.1V, TA=0 C to +70 C)

PARAMETER		25 (400 MHz)		27 (375 MHz)		30 (333 MHz)		33 (300 MHz)		unit	notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock											
Clock Cycle Time (K, $\overline{K}$)	tKHKH	2.50	7.5	2.66	7.5	3.00	7.5	3.30	7.5	ns	
Clock Phase Jitter (K, $\overline{K}$)	tKC var		0.20		0.20		0.20		0.20	ns	4
Clock High Time (K, $\overline{K}$)	tKHKL	0.40		0.40		0.40		0.40		cycles	
Clock Low Time (K, $\overline{K}$)	tKLKH	0.40		0.40		0.40		0.40		ns	
Clock to $\overline{Clock}$ (K, $\overline{K}$)	tKH$\overline{K}$H	1.06		1.13		1.28		1.40		ns	
DLL Lock Time (K, $\overline{K}$)	tKC lock	2048		2048		2048		2048		cycles	5
Doff Low period to DLL reset	tDoffLowToReset	5		5		5		5		ns	
Output Times											
K, $\overline{K}$ High to Output Valid	tCHQV		0.45		0.45		0.45		0.45	ns	
K, $\overline{K}$ High to Output Hold	tCHQX	-0.45		-0.45		-0.45		-0.45		ns	
K, $\overline{K}$ High to Echo Clock Valid	tCHCQV		0.45		0.45		0.45		0.45	ns	
K, $\overline{K}$ High to Echo Clock Hold	tCHCQX	-0.45		-0.45		-0.45		-0.45		ns	
CQ, $\overline{CQ}$ High to Output Valid	tCQHQV		0.20		0.20		0.20		0.20	ns	6
CQ, $\overline{CQ}$ High to Output Hold	tCQHQX	-0.20		-0.20		-0.20		-0.20		ns	6
K, High to Output High-Z	tCHQZ		0.45		0.45		0.45		0.45	ns	
K, High to Output Low-Z	tCHQX1	-0.45		-0.45		-0.45		-0.45		ns	
Setup Times											
Address valid to K rising edge	tAVKH	0.40		0.40		0.40		0.40		ns	
Control inputs valid to K rising edge	tIVKH	0.40		0.40		0.40		0.40		ns	2
Data-in valid to K, K rising edge	tDVKH	0.28		0.28		0.28		0.28		ns	
Hold Times										ns	
K rising edge to address hold	tKHAX	0.40		0.40		0.40		0.40		ns	
K rising edge to control inputs hold	tKHIX	0.40		0.40		0.40		0.40		ns	
K, $\overline{K}$ rising edge to data-in hold	tKHDX	0.28		0.28		0.28		0.28		ns	

Notes:

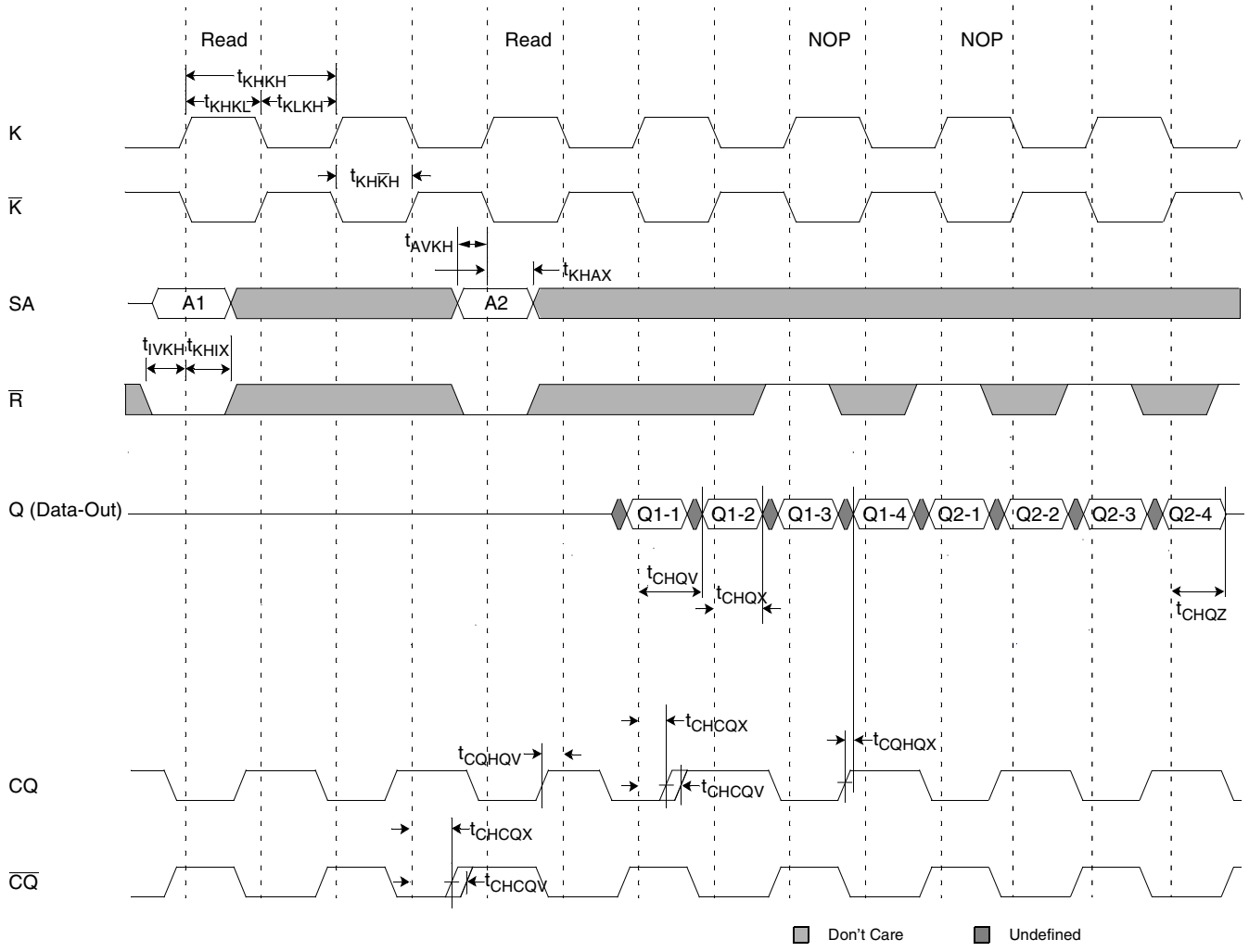
1. All address inputs must meet the specified setup and hold times for all latching clock edges.
2. Control singles are R, W,BW0,BW1 and (BW2, BW3, also for x36)
3. To avoid bus contention, at a given voltage and temperature tCHQX1 is bigger than tCHQZ.

The specs as shown do not imply bus contention because tCHQX1 is a MIN parameter that is worst case at totally different test conditions (0 C, 1.9V) than tCHQZ, which is a MAX parameter (worst case at 70 C, 1.7V)

It is not possible for two SRAMs on the same board to be at such different voltage and temperature.

4. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
5. Vdd slew rate must be less than 0.1V DC per 50ns for DLL lock retention. DLL lock time begins once Vdd and input clock are stable.
6. Echo clock is very tightly controlled to data valid/data hold. By design, there is a ns variation from echo clock to data. The data sheet parameters reflect tester guard bands and test setup variations

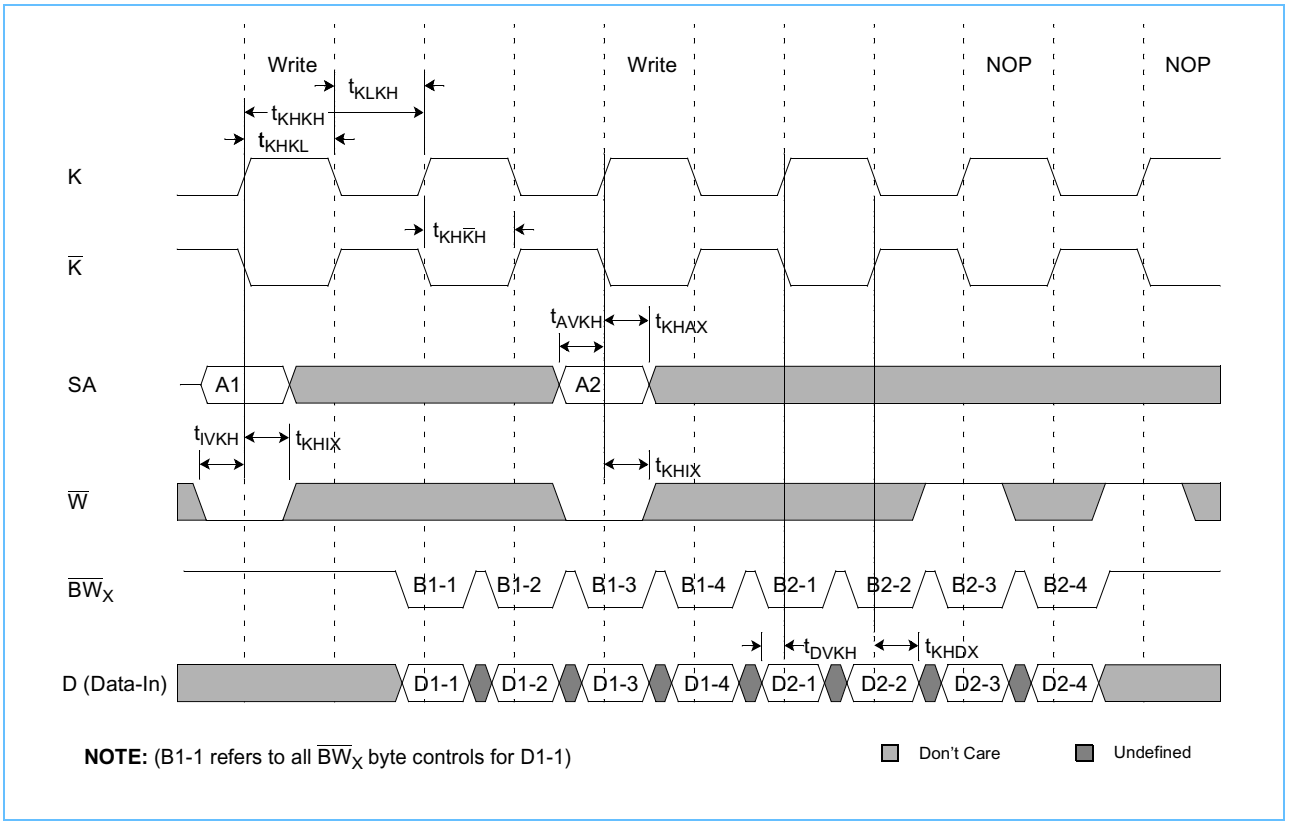
Read and Deselect Cycles Timing Diagram



Note: 1. Q1-1 refers to the output from address A1+0, Q1-2, Q1-3, Q1-4 refers to the output from address A1+1, A1+2, A1+3, which is the nex internal burst addresses following A1+0.

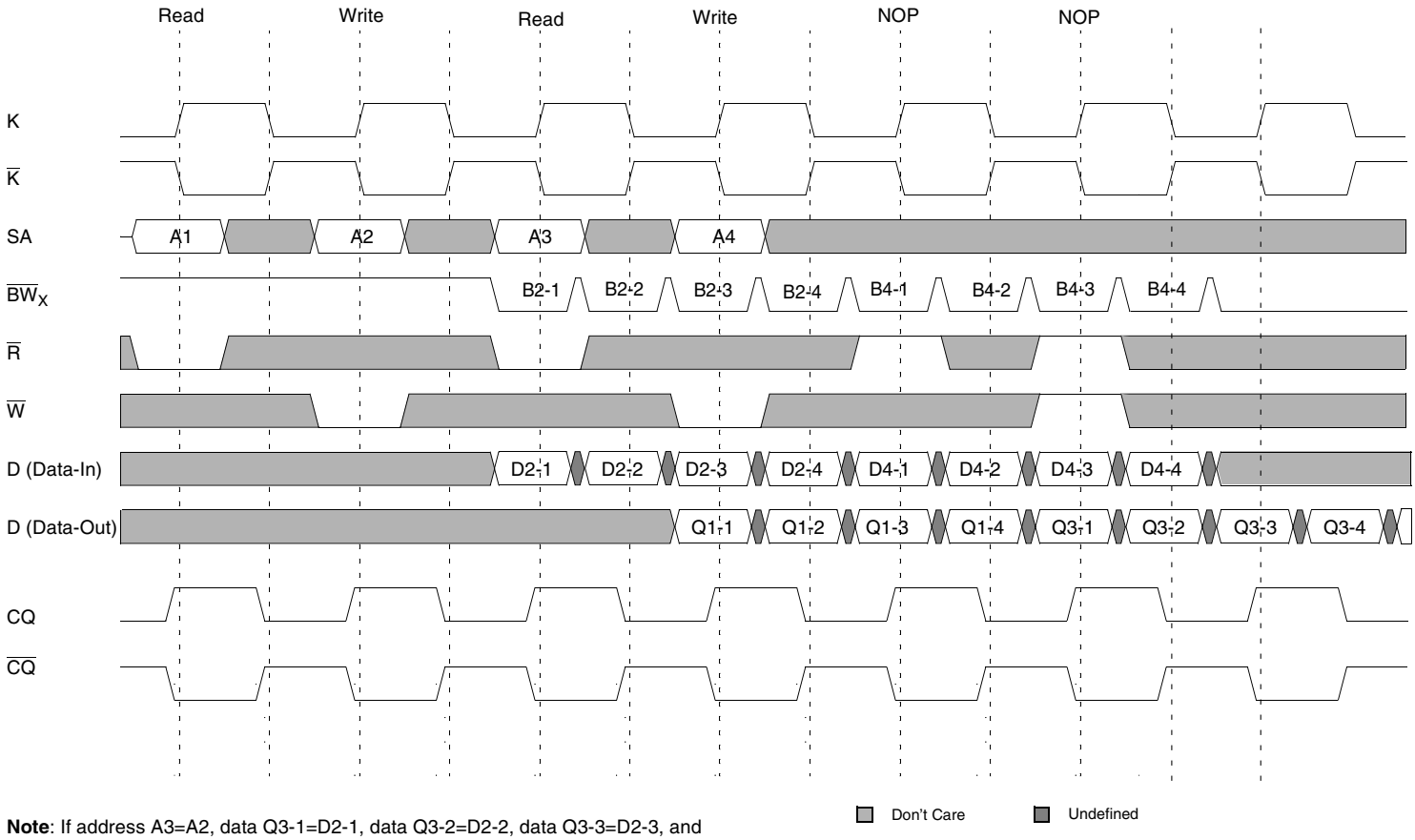
2. Outputs are disabled one cycle after a NOP.

Write and NOP Timing Diagram



NOTE: (B1-1 refers to all $\overline{BW}_X$ byte controls for D1-1)

Read, Write, and NOP Timing Diagram



Note: If address A3=A2, data Q3-1=D2-1, data Q3-2=D2-2, data Q3-3=D2-3, and data Q3-4=D2-4, then write data is forwarded immediately as read results.

IEEE 1149.1 TAP and Boundary Scan

The SRAM provides a limited set of JTAG functions to test the interconnection between SRAM I/Os and printed circuit board traces or other components. There is no multiplexer in the path from I/O pins to the RAM core.

In conformance with IEEE Standard 1149.1, the SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

The TAP controller has a standard 16-state machine that resets internally on power-up. Therefore, a TRST signal is not required.

Signal List

- TCK: test clock
- TMS: test mode select
- TDI: test data-in
- TDO: test data-out

JTAG DC Operating Characteristics (T_A = 0 to +70° C)

Operates with JEDEC Standard 8-5 (1.8V) logic signal levels

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
JTAG input high voltage	V_{IH1}	1.3	—	V_{DD}+0.3	V	1
JTAG input low voltage	V_{IL1}	-0.3	—	0.5	V	1
JTAG output high level	V_{OH1}	V_{DD}-0.4	—	V_{DD}	V	1, 2
JTAG output low level	V_{OL1}	V_{SS}	—	0.4	V	1, 3

1. All JTAG inputs and outputs are LVTTL-compatible.
2. I_{OH1} = -2mA
3. I_{OL1} = +2mA

JTAG AC Test Conditions (T_A = 0 to +70° C, V_{DD} = 1.8V -5%, +5%)

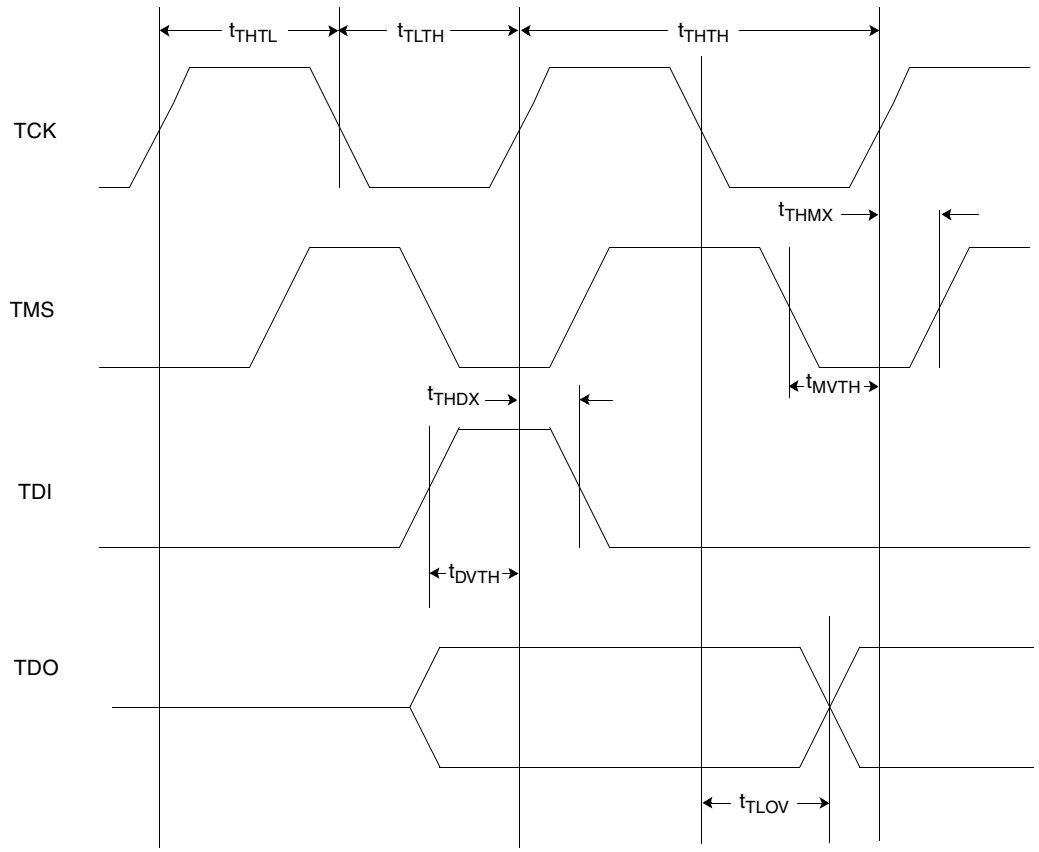
Parameter	Symbol	Conditions	Units
Input pulse high level	V_{IH1}	1.3	V
Input pulse low level	V_{IL1}	0.5	V
Input rise time	T_{R1}	1.0	ns
Input fall time	T_{F1}	1.0	ns
Input and output timing reference level		0.9	V

JTAG AC Characteristics (T_A = 0 to +70° C, V_{DD} = 1.8V -5%, +5%)

Parameter	Symbol	Minimum	Maximum	Units	Notes
TCK cycle time	t_{THTH}	20	—	ns	
TCK high pulse width	t_{THTL}	7	—	ns	
TCk low pulse width	t_{TLTH}	7	—	ns	
TMS setup	t_{MVTH}	4	—	ns	
TMS hold	t_{THMX}	4	—	ns	
TDI setup	t_{DVTH}	4	—	ns	
TDI hold	t_{THDX}	4	—	ns	
TCK low to valid data	t_{TLOV}	—	7	ns	1

1. See *AC Test Loading* on page 16.

JTAG Timing Diagram



Scan Register Definition

Register Name	Bit Size x18 or x36
Instruction	3
Bypass	1
ID	32
Boundary Scan	109

ID Register Definition

Part	Field Bit Number and Description			
	Revision Number (31:29)	Part Configuration (28:12)	JEDEC Code (11:1)	Start Bit (0)
4M x 18	000	00def0wx0t0q0b0s0	000 101 001 00	1
2M x 36	000	00def0wx0t0q0b0s0	000 101 001 00	1

Part Configuration Definition:
def = 011 for 72Mb
wx = 11 for x36, 10 for x18
t = 1 for DLL, 0 for non-DLL
q = 1 for QUADB4, 0 for DDR-II
b = 1 for burst of 4, 0 for burst of 2
s = 1 for separate I/0, 0 for common I/O

Instruction Set

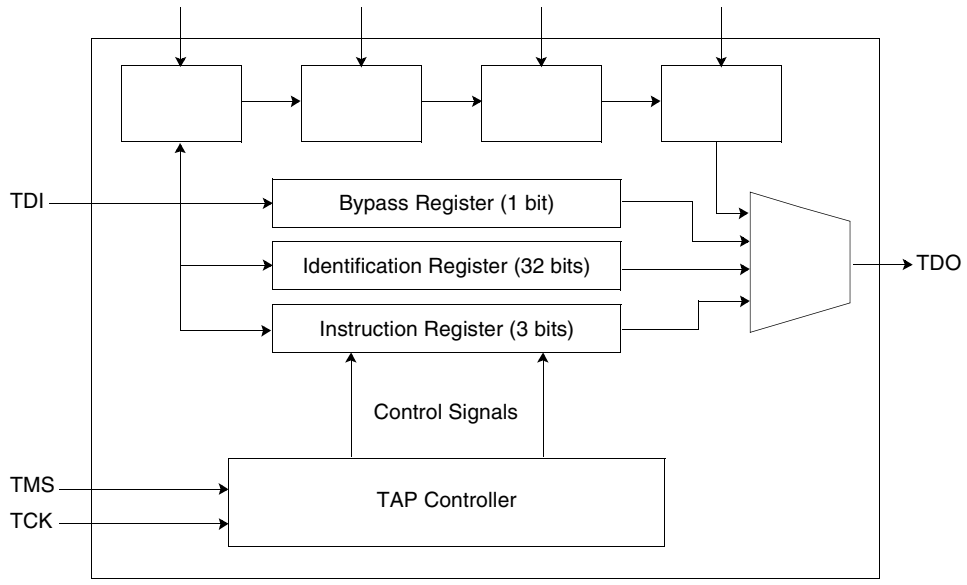
Code	Instruction	TDO Output	Notes
000	EXTEST	Boundary Scan Register	2,6
001	IDCODE	32-bit Identification Register	
010	SAMPLE-Z	Boundary Scan Register	1, 2
011	PRIVATE	Do not use	5
100	SAMPLE	Boundary Scan Register	4
101	PRIVATE	Do not use	5
110	PRIVATE	Do not use	5
111	BYPASS	Bypass Register	3

1. Places Qs in high-Z in order to sample all input data, regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. BYPASS register is initiated to V_{SS} when BYPASS instruction is invoked. The BYPASS register also holds the last serially loaded TDI when exiting the shift-DR state.
4. SAMPLE instruction does not place DQs in high-Z.
5. This instruction is reserved. Invoking this instruction will cause improper SRAM functionality.
6. This EXTEST is not IEEE 1149.1-compliant. By default, it places Q in high-Z. If the internal register on the scan chain is set high, Q will be updated with information loaded via a previous SAMPLE instruction. The actual transfer occurs during the update IR state after EXTEST is loaded. The value of the internal register can be changed during SAMPLE and EXTEST only.

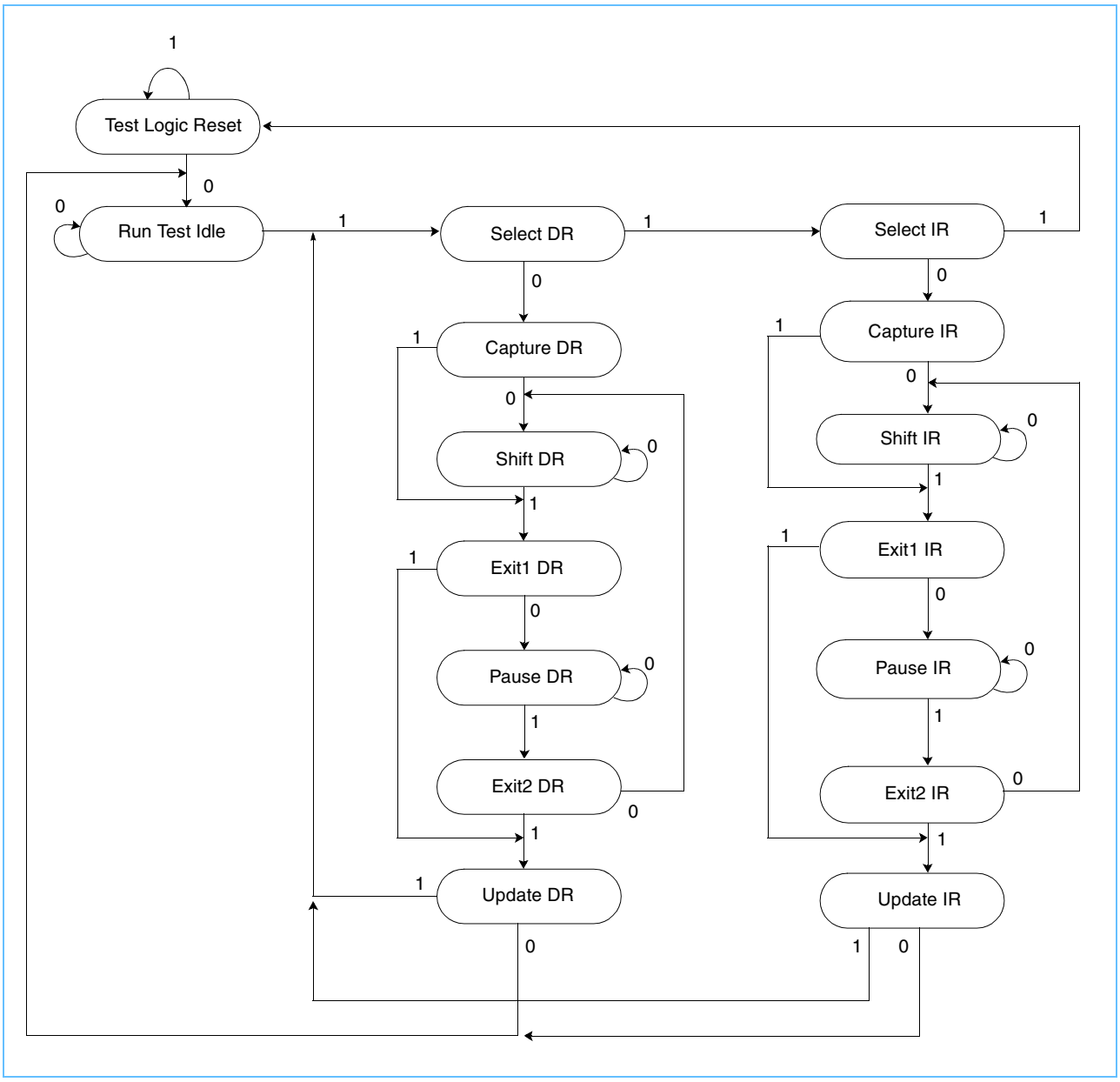
List of IEEE 1149.1 Standard Violations

- 7.2.1.b, e
- 7.7.1.a-f
- 10.1.1.b, e
- 10.7.1.a-d
- 6.1.1.d

JTAG Block Diagram



TAP Controller State Machine



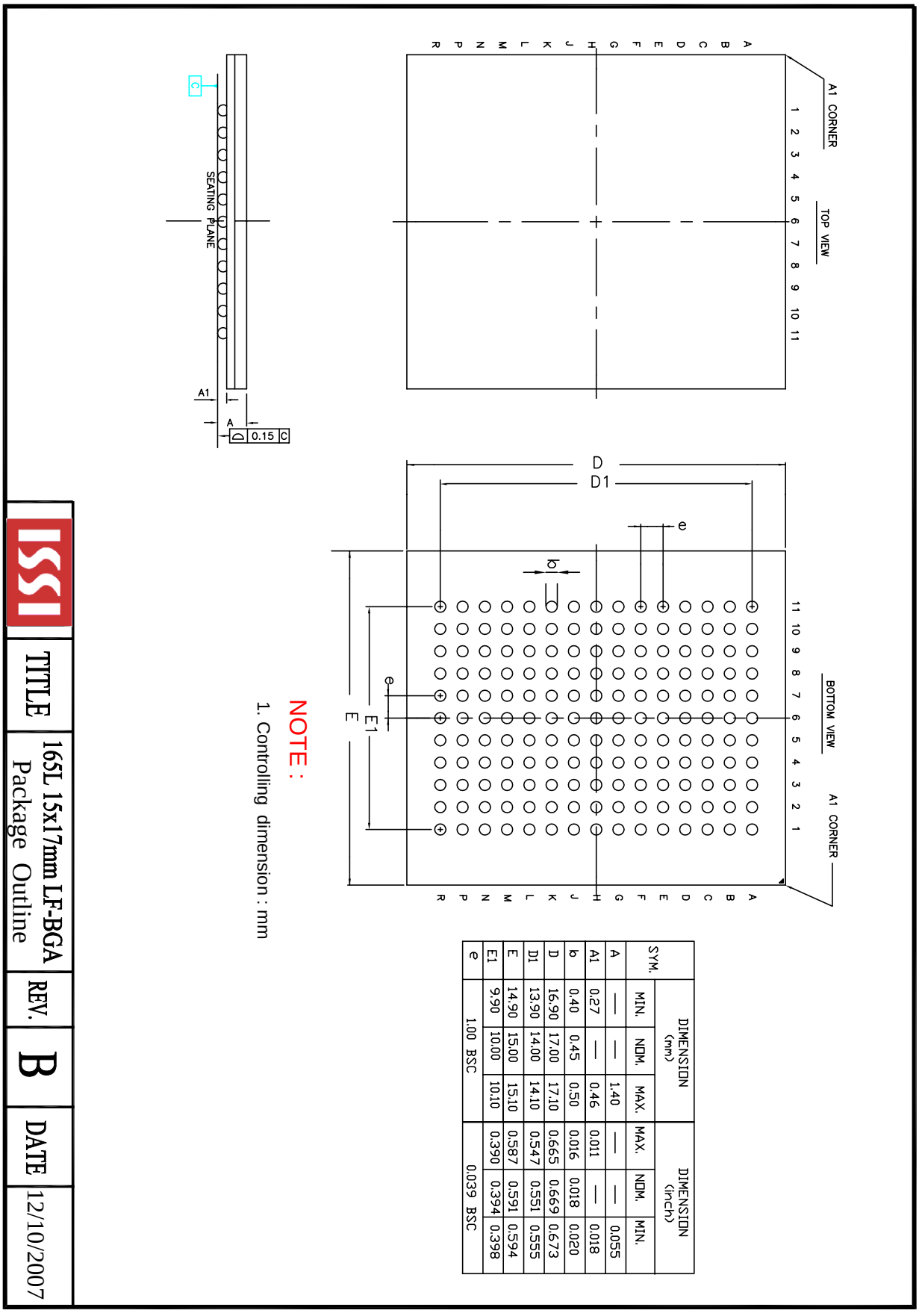
Boundary Scan Exit Order The same length is used for x18 and x36 I/O configuration.

Order	Pin ID
1	6R
2	6P
3	6N
4	7P
5	7N
6	7R
7	8R
8	8P
9	9R
10	11P
11	10P
12	10N
13	9P
14	10M
15	11N
16	9M
17	9N
18	11L
19	11M
20	9L
21	10L
22	11K
23	10K
24	9J
25	9K
26	10J
27	11J
28	11H
29	10G
30	9G
31	11F
32	11G
33	9F
34	10F
35	11E
36	10E

Order	Pin ID
37	10D
37	9E
39	10C
40	11D
41	9C
42	9D
43	11B
44	11C
45	9B
46	10B
47	11A
48	10A
49	9A
50	8B
51	7C
52	6C
53	8A
54	7A
55	7B
56	6B
57	6A
58	5B
59	5A
60	4A
61	5C
62	4B
63	3A
64	2A
65	1A
66	2B
67	3B
68	1C
69	1B
70	3D
71	3C
72	1D

Order	Pin ID
73	2C
74	3E
75	2D
76	2E
77	1E
78	2F
79	3F
80	1G
81	1F
82	3G
83	2G
84	1H
85	1J
86	2J
87	3K
88	3J
89	2K
90	1K
91	2L
92	3L
93	1M
94	1L
95	3N
96	3M
97	1N
98	2M
99	3P
100	2N
101	2P
102	1P
103	3R
104	4R
105	4P
106	5P
107	5N
108	5R
109	Internal

Note:
1) NC pins as defined on *FBGA pinouts* on page 2 are read as “don’t cares”.
2) State of Internal pin (#109) is loaded via JTAG



SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MAX.	NOM.	MIN.
A	—	—	1.40	—	—	0.055
A1	0.27	—	0.46	0.011	—	0.018
b	0.40	0.45	0.50	0.016	0.018	0.020
D	16.90	17.00	17.10	0.665	0.669	0.673
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	14.90	15.00	15.10	0.587	0.591	0.594
E1	9.90	10.00	10.10	0.390	0.394	0.398
e	1.00 BSC			0.039 BSC		

TITLE	165L 15x17mm LF-BGA Package Outline
REV.	B
DATE	12/10/2007

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed	Order Part No.	Organization	Package
400 MHz	IS61QDPB42M36-400M3	2Mx36	165 BGA
	IS61QDPB42M36-400M3L	2Mx36	165 BGA, Lead-free
	IS61QDPB44M18-400M3	4Mx18	165 BGA
	IS61QDPB44M18-400M3L	4Mx18	165 BGA, Lead-free
375 MHz	IS61QDPB42M36-375M3	2Mx36	165 BGA
	IS61QDPB42M36-375M3L	2Mx36	165 BGA, Lead-free
	IS61QDPB44M18-375M3	4Mx18	165 BGA
	IS61QDPB44M18-375M3L	4Mx18	165 BGA, Lead-free
333 MHz	IS61QDPB42M36-333M3	2Mx36	165 BGA
	IS61QDPB42M36-333M3L	2Mx36	165 BGA, Lead-free
	IS61QDPB44M18-333M3	4Mx18	165 BGA
	IS61QDPB44M18-333M3L	4Mx18	165 BGA, Lead-free
300 MHz	IS61QDPB42M36-300M3	2Mx36	165 BGA
	IS61QDPB42M36-300M3L	2Mx36	165 BGA, Lead-free
	IS61QDPB44M18-300M3	4Mx18	165 BGA
	IS61QDPB44M18-300M3L	4Mx18	165 BGA, Lead-free