

Silicon PNP Power Transistors

2SB595

DESCRIPTION

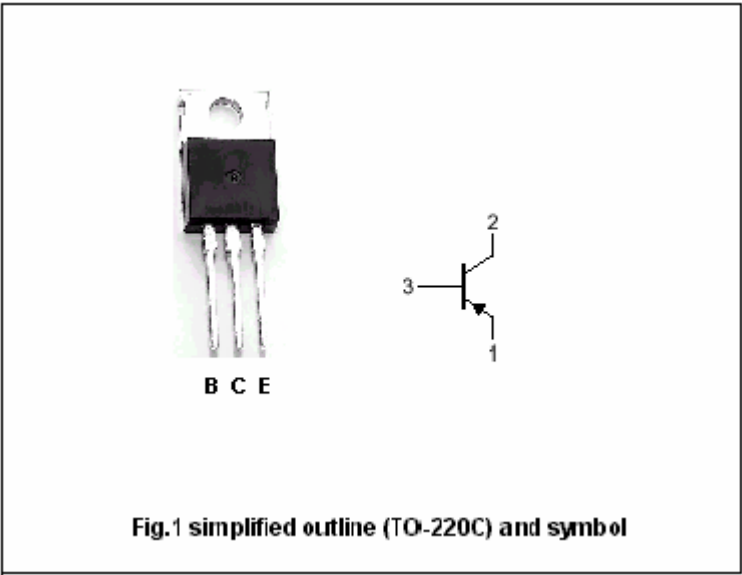
- With TO-220C package
- Complement to type 2SD525
- High breakdown voltage : $V_{CEO}=-100V$
- Low collector saturation voltage
: $V_{CE(sat)}=-2.0V(Max)$

APPLICATIONS

- Power amplifier applications
- Recommend for 30W high fidelity audio frequency amplifier output stage

PINNING

PIN	DESCRIPTION
1	Emitter
2	Collector;connected to mounting base
3	Base



Absolute maximum ratings($T_c=25\text{ }^{\circ}C$)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	-100	V
V_{CEO}	Collector-emitter voltage	Open base	-100	V
V_{EBO}	Emitter-base voltage	Open collector	-5	V
I_C	Collector current		-5	A
I_E	Emitter current		-5	A
I_B	Base current		-4	A
P_C	Collector power dissipation	$T_c=25$	40	W
T_j	Junction temperature		150	
T_{stg}	Storage temperature		-55~150	

CHARACTERISTICS

T_j=25 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =-50mA; I _B =0	-100			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =-10mA; I _C =0	-5			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =-4A; I _B =-0.4 A			-2.0	V
V _{BE}	Base-emitter on voltage	I _C =-4A ; V _{CE} =-5V			-1.5	V
I _{CBO}	Collector cut-off current	V _{CB} =-100V; I _E =0			-100	μ A
I _{EBO}	Emitter cut-off current	V _{EB} =-5V; I _C =0			-1	mA
h _{FE-1}	DC current gain	I _C =-1A ; V _{CE} =-5V	40		240	
h _{FE-2}	DC current gain	I _C =-4A ; V _{CE} =-5V	20			
f _T	Transition frequency	I _C =-1A ; V _{CE} =-5V		5		MHz
C _{OB}	Output capacitance	I _E =0; V _{CB} =-10V; f=1MHz		270		pF

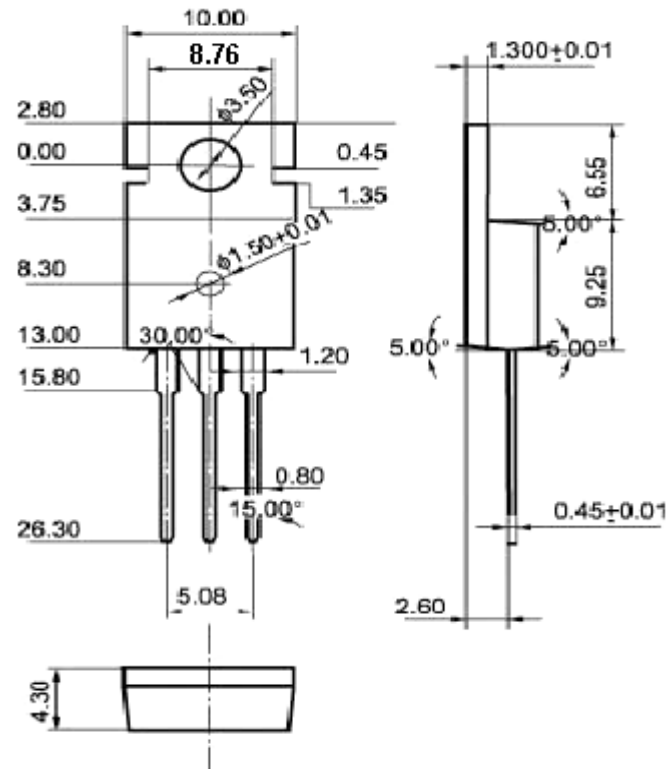
◆ h_{FE-1} classifications

R	O	Y
40-80	70-140	120-240

Silicon PNP Power Transistors

2SB595

PACKAGE OUTLINE

Fig.2 Outline dimensions (unindicated tolerance: ± 0.10 mm)

Silicon PNP Power Transistors

2SB595

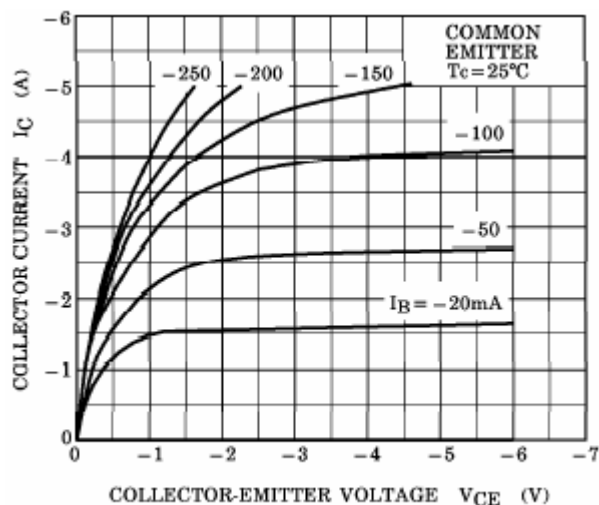


Fig.3 Static Characteristic

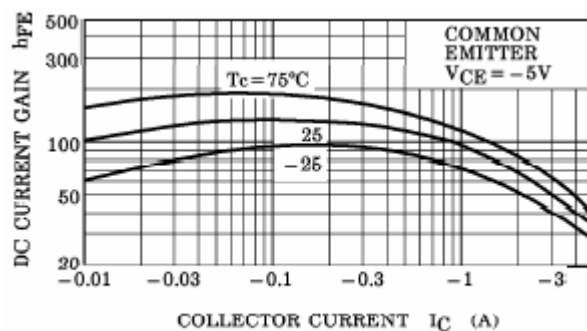


Fig.4 DC current Gain

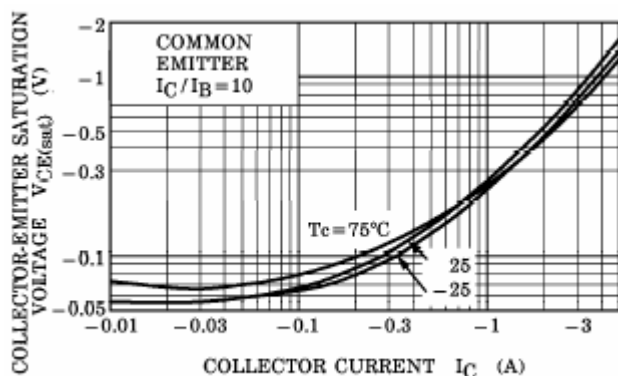


Fig.5 Collector-Emmitter Saturation Voltage

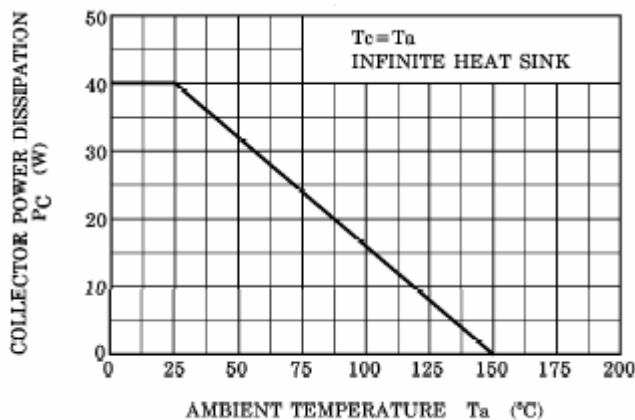


Fig.6 Power Derating

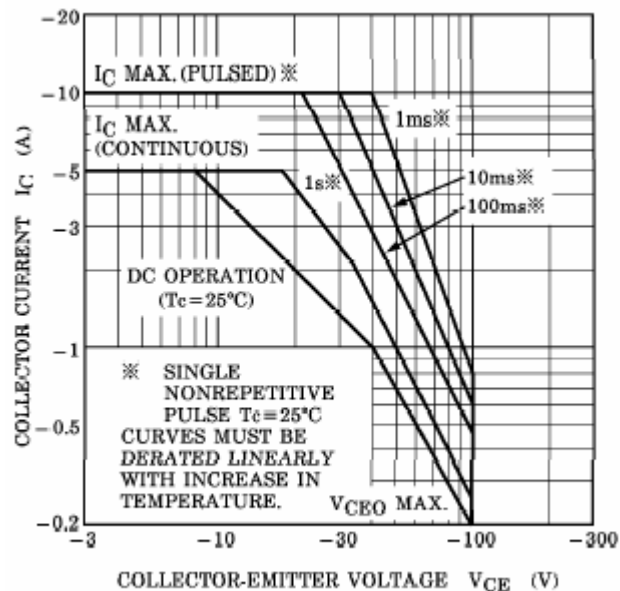


Fig.7 Safe Operating Area