

74ABT821

10-bit D-type flip-flop; positive-edge trigger; 3-state

Rev. 03 — 25 February 2010

Product data sheet

1. General description

The 74ABT821 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT821 bus interface register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of buses carrying parity.

The 74ABT821 is a buffered 10-bit wide version of the 74ABT374A.

The 74ABT821 is a 10-bit, edge-triggered register coupled to ten 3-state output buffers. The device is controlled by the clock (CP) and output enable (\overline{OE}) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition is transferred to the corresponding output Q of the flip-flop.

The 3-state output buffers are designed to drive heavily loaded 3-state buses, MOS memories, or MOS microprocessors.

The active LOW output enable (\overline{OE}) controls all ten 3-state buffers independent of the register operation. When \overline{OE} is LOW, the data in the register appears at the outputs. When \overline{OE} is HIGH, the outputs are in high-impedance OFF-state, which means they will neither drive nor load the bus.

2. Features and benefits

- High-speed parallel registers with positive-edge triggered D-type flip-flops
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Output capability: +64 mA and -32 mA
- Power-on 3-state
- Power-on reset
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V

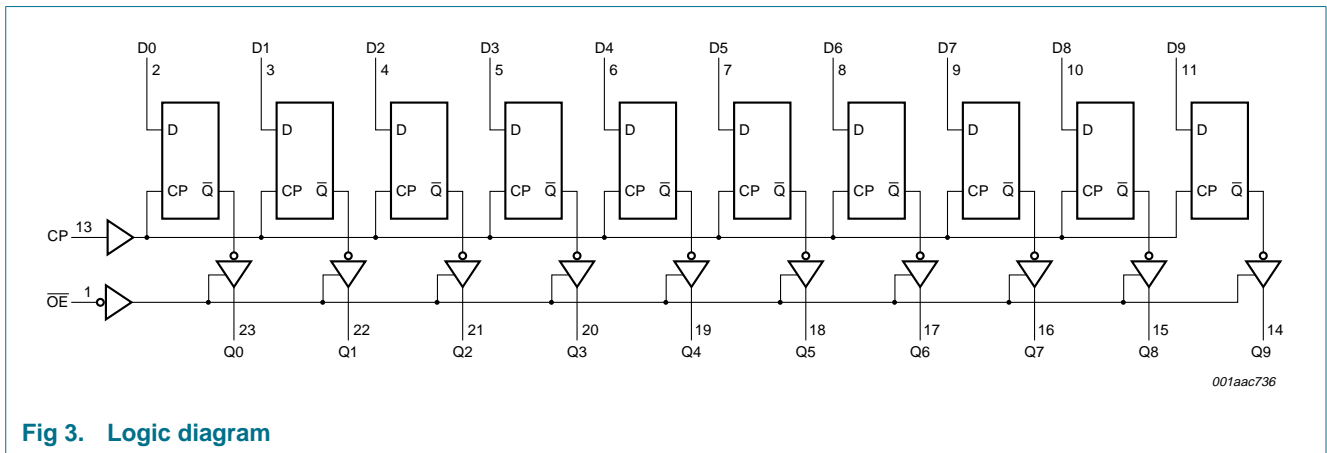
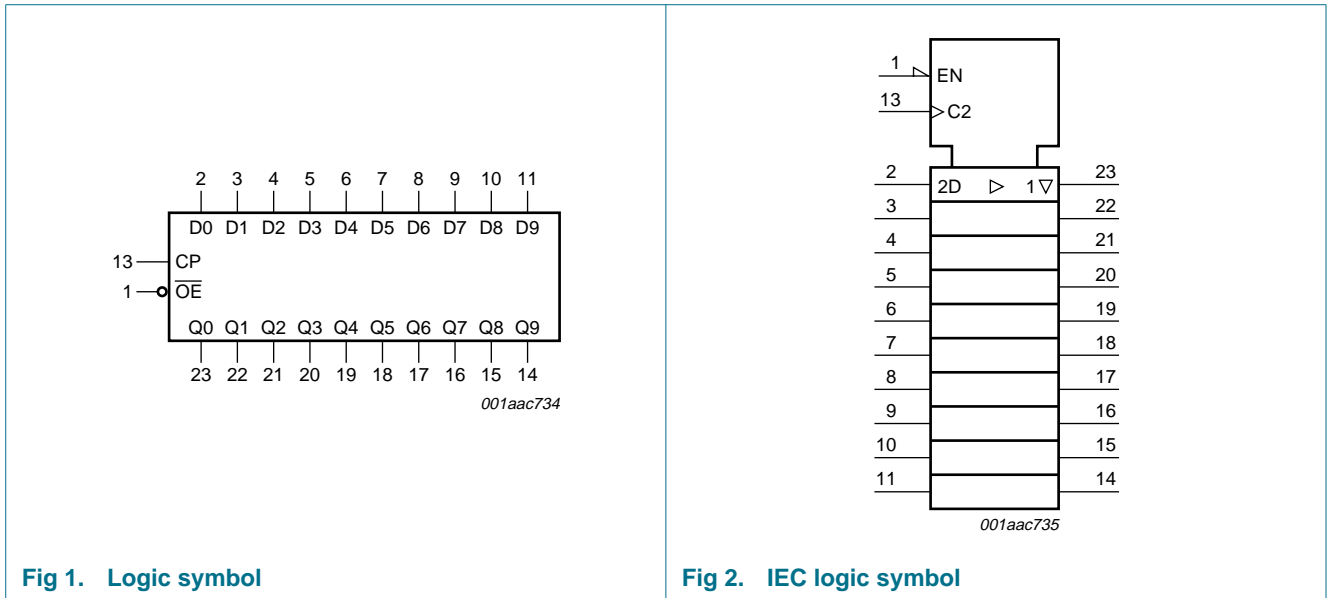


3. Ordering information

Table 1. Ordering information

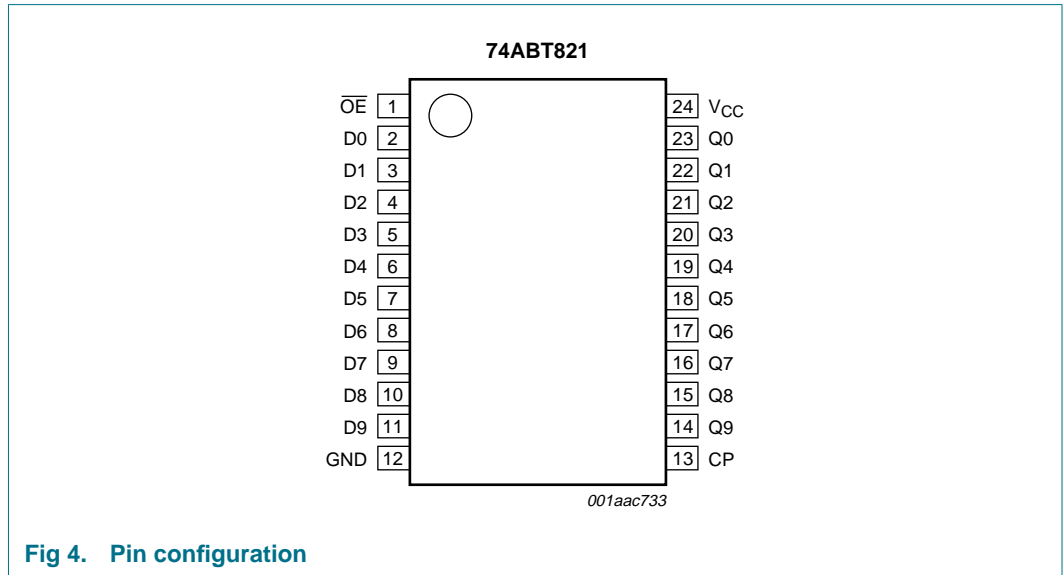
Type number	Package			Version
	Temperature range	Name	Description	
74ABT821D	-40 °C to +85 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74ABT821DB	-40 °C to +85 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
74ABT821PW	-40 °C to +85 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

4. Functional diagram



5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
OE	1	output enable input (active LOW)
D0 to D9	2, 3, 4, 5, 6, 7, 8, 9, 10, 11	data input
GND	12	ground (0 V)
CP	13	clock pulse input (active rising edge)
Q0 to Q9	23, 22, 21, 20, 19, 18, 17, 16, 15, 14	data output
V _{CC}	24	supply voltage

6. Functional description

6.1 Function table

Table 3. Function table^[1]

Input			Internal register	Output Q0 to Q9	Operating mode
OE	CP	D0 to D9			
L	↑	l	L	L	load and read register
L	↑	h	H	H	
L	NC	X	NC	NC	hold
H	NC	X	NC	Z	disable outputs
H	↑	Dn	Dn	Z	

- [1] H = HIGH voltage level;
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
 L = LOW voltage level;
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
 NC = no change;
 X = don't care;
 Z = high-impedance OFF-state;
 ↑ = LOW-to-HIGH clock transition.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage		[1] -1.2	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state	[1] -0.5	+5.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-18	-	mA
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
I_O	output current	output in LOW-state	-	128	mA
T_j	junction temperature		[2] -	150	°C
T_{stg}	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		-32	-	-	mA
I_{OL}	LOW-level output current		-	-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate		0	-	5	ns/V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C

9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit	
			Min	Typ	Max	Min	Max		
V _{IK}	input clamping voltage	V _{CC} = 4.5 V; I _{IK} = -18 mA	-1.2	-0.9	-	-1.2	-	V	
V _{OH}	HIGH-level output voltage	V _I = V _{IL} or V _{IH}							
		V _{CC} = 4.5 V; I _{OH} = -3 mA	2.5	2.9	-	2.5	-	V	
		V _{CC} = 5.0 V; I _{OH} = -3 mA	3.0	3.4	-	3.0	-	V	
		V _{CC} = 4.5 V; I _{OH} = -32 mA	2.0	2.4	-	2.0	-	V	
V _{OL}	LOW-level output voltage	V _{CC} = 4.5 V; I _{OL} = 64 mA; V _I = V _{IL} or V _{IH}	-	0.42	0.55	-	0.55	V	
V _{OL(pu)}	power-up LOW-level output voltage	V _{CC} = 5.5 V; I _O = 1 mA; V _I = GND or V _{CC}	[1]	-	0.13	0.55	-	0.55	V
I _I	input leakage current	V _{CC} = 5.5 V; V _I = GND or 5.5 V	-	±0.01	±1.0	-	±1.0	µA	
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O ≤ 4.5 V	-	±5.0	±100	-	±100	µA	
I _{O(pu/pd)}	power-up/power-down output current	V _{CC} = 2.0 V; V _O = 0.5 V; V _I = GND or V _{CC} ; OE _n HIGH	[2]	-	±5.0	±50	-	±50	µA
I _{OZ}	OFF-state output current	V _{CC} = 5.5 V; V _I = V _{IL} or V _{IH}							
		V _O = 2.7 V	-	5.0	50	-	50	µA	
		V _O = 0.5 V	-	-5.0	-50	-	-50	µA	
I _{LO}	output leakage current	HIGH-state; V _O = 5.5 V; V _{CC} = 5.5 V; V _I = GND or V _{CC}	-	5.0	50	-	50	µA	
I _O	output current	V _{CC} = 5.5 V; V _O = 2.5 V	[3]	-180	-80	-50	-180	-50	mA
I _{CC}	supply current	V _{CC} = 5.5 V; V _I = GND or V _{CC}							
		outputs HIGH-state	-	0.5	250	-	250	µA	
		outputs LOW-state	-	25	38	-	38	mA	
		outputs disabled	-	0.5	250	-	250	µA	
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 5.5 V; one input at 3.4 V; other inputs at V _{CC} or GND	[4]	-	0.5	1.5	-	1.5	mA
C _I	input capacitance	V _I = 0 V or V _{CC}	-	4	-	-	-	pF	
C _O	output capacitance	outputs disabled; V _O = 0 V or V _{CC}	-	7	-	-	-	pF	

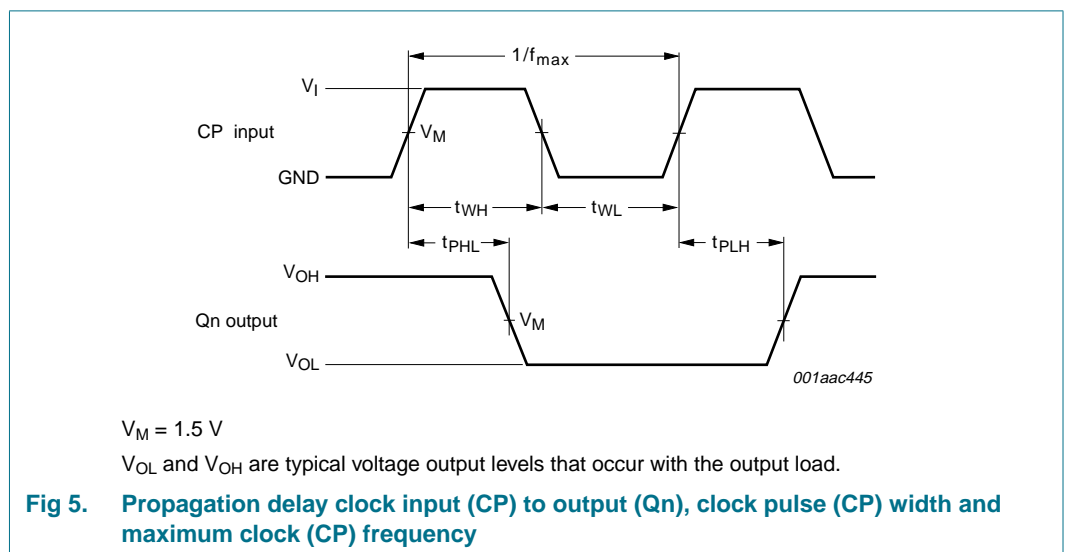
- [1] For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- [2] This parameter is valid for any V_{CC} between 0 V and 2.1 V with a transition time of up to 10 ms. For V_{CC} = 2.1 V to V_{CC} = 5 V ± 10 %, a transition time of up to 100 µs is permitted.
- [3] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- [4] This is the increase in supply current for each input at 3.4 V.

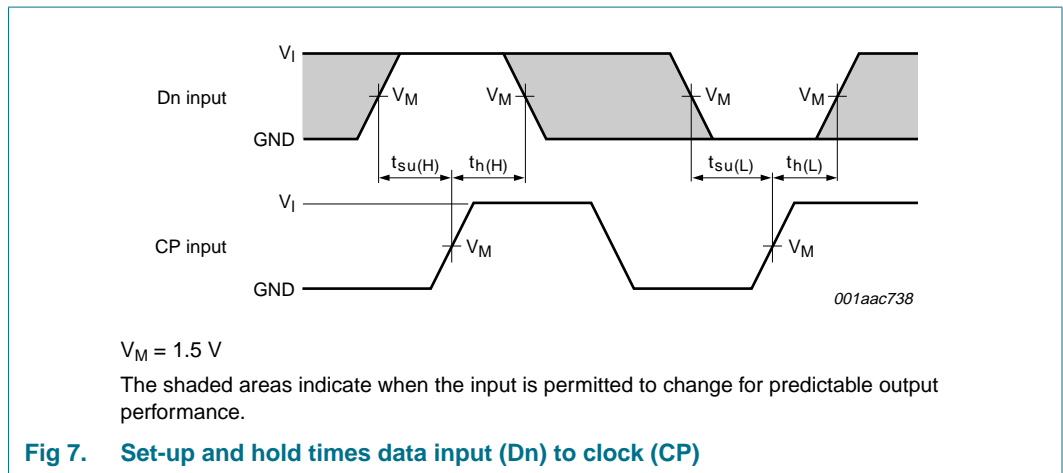
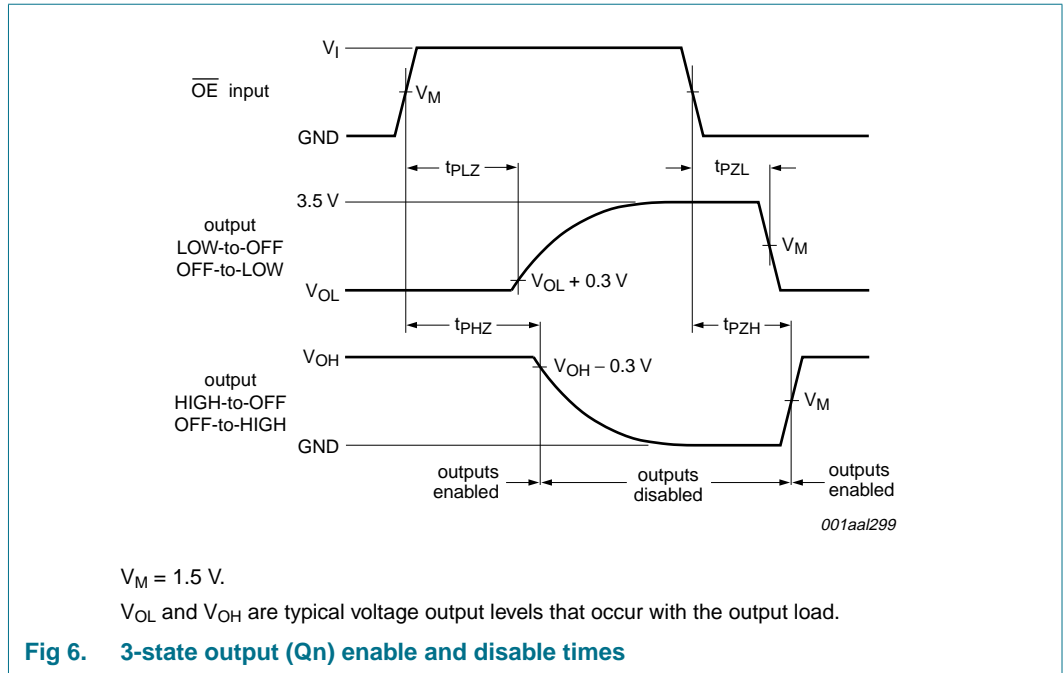
10. Dynamic characteristics

Table 7. Dynamic characteristics
GND = 0 V; for test circuit, see Figure 8.

Symbol	Parameter	Conditions	25 °C; V _{CC} = 5.0 V			-40 °C to +70 °C; V _{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t _{PLH}	LOW to HIGH propagation delay	CP to Qn; see Figure 5	2.1	4.1	5.6	2.1	6.2	ns
t _{PHL}	HIGH to LOW propagation delay	CP to Qn; see Figure 5	2.8	4.6	6.2	2.8	6.7	ns
t _{PZH}	OFF-state to HIGH propagation delay	$\overline{O}E_n$ to Qn; see Figure 6	1.0	3.0	4.5	1.0	5.3	ns
t _{PZL}	OFF-state to LOW propagation delay	$\overline{O}E_n$ to Qn; see Figure 6	2.2	4.1	5.6	2.2	6.3	ns
t _{PHZ}	HIGH to OFF-state propagation delay	$\overline{O}E_n$ to Qn; see Figure 6	2.7	4.7	6.2	2.7	6.7	ns
t _{PLZ}	LOW to OFF-state propagation delay	$\overline{O}E_n$ to Qn; see Figure 6	2.3	4.6	6.1	2.3	6.5	ns
t _{su(H)}	set-up time HIGH	Dn to CP; see Figure 7	2.1	0.5	-	2.1	-	ns
t _{su(L)}	set-up time LOW	Dn to CP; see Figure 7	2.1	0.3	-	2.1	-	ns
t _{h(H)}	hold time HIGH	Dn to CP; see Figure 7	1.3	0	-	1.3	-	ns
t _{h(L)}	hold time LOW	Dn to CP; see Figure 7	1.3	-0.3	-	1.3	-	ns
t _{WH}	pulse width HIGH	CP; see Figure 5	2.9	1.8	-	2.9	-	ns
t _{WL}	pulse width LOW	CP; see Figure 5	3.8	2.8	-	3.8	-	ns
f _{max}	maximum frequency	see Figure 5	125	185	-	125	-	MHz

11. Waveforms





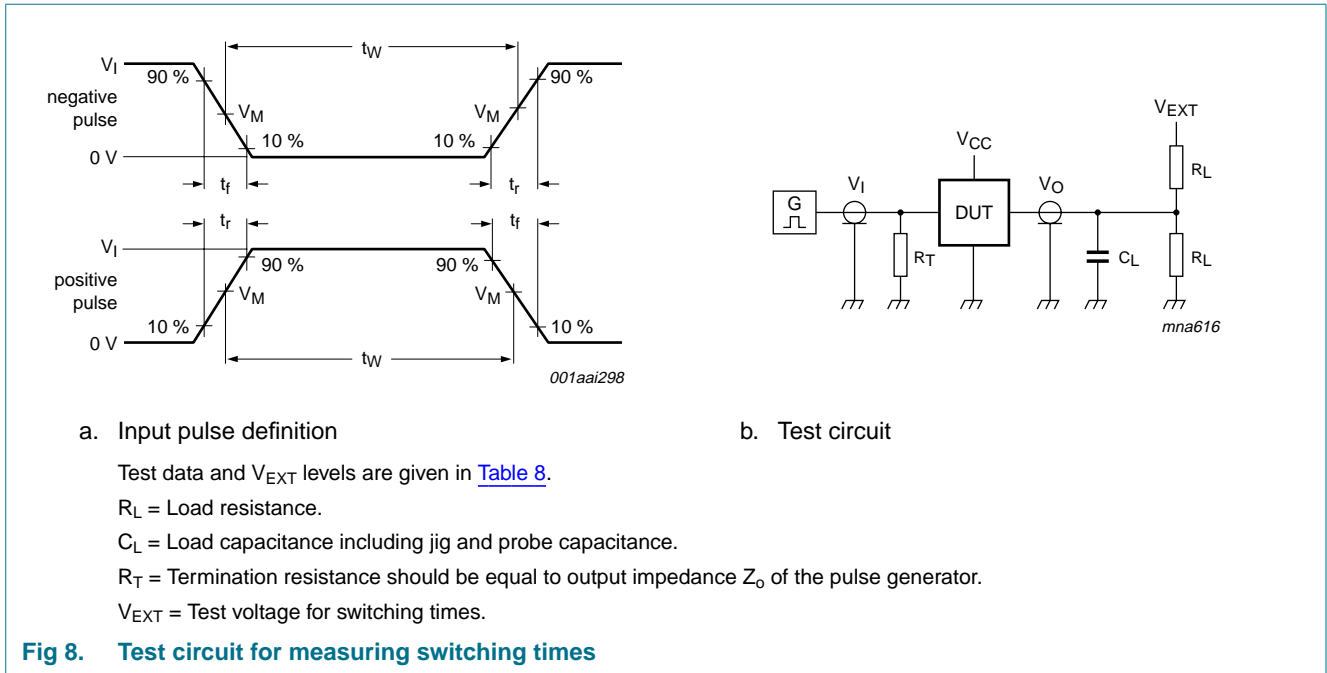


Table 8. Test data

Input				Load		V_{EXT}		
V_I	f_I	t_W	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
3.0 V	1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open	open	7.0 V

12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

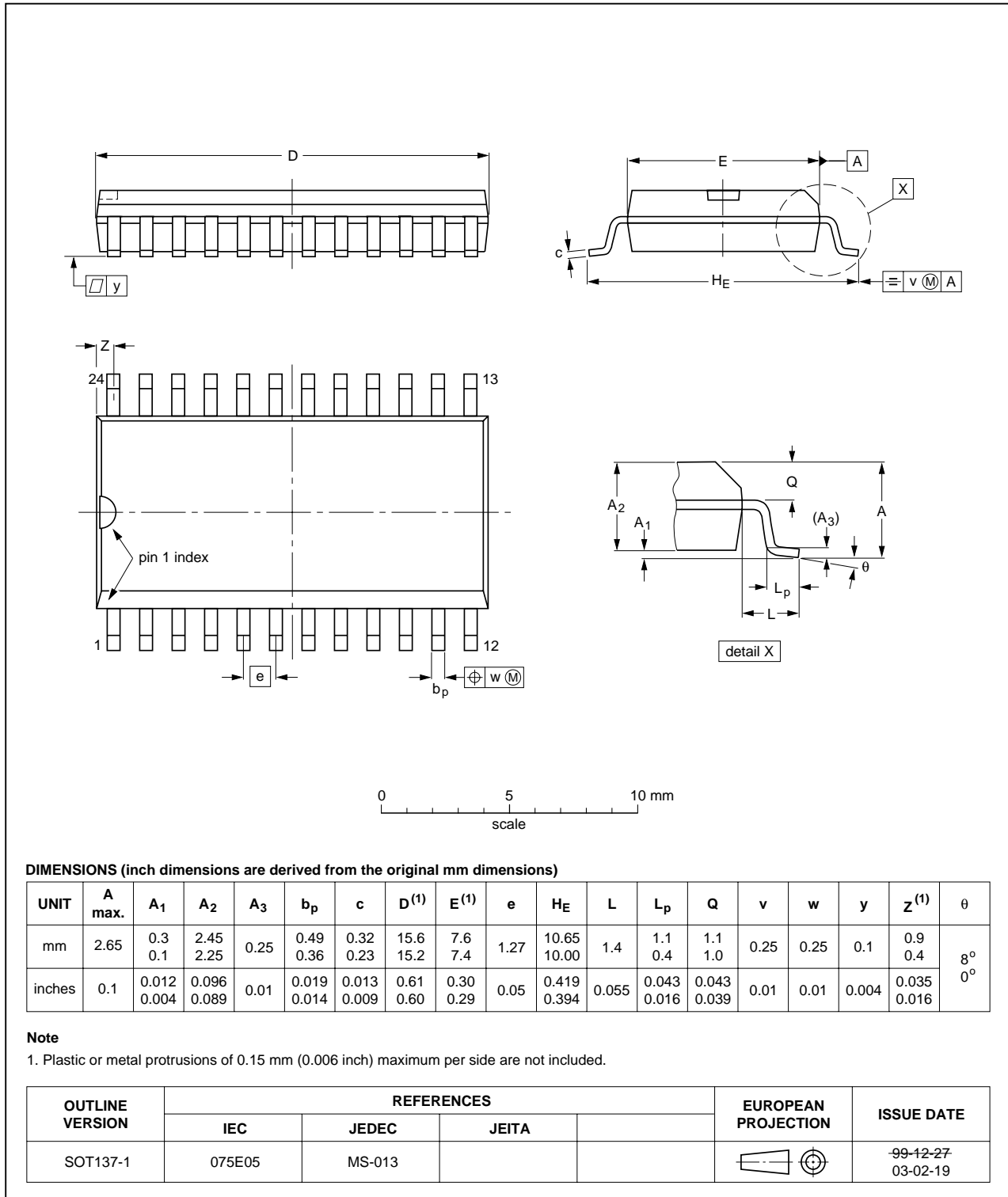


Fig 9. Package outline SOT137-1 (SO24)

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1

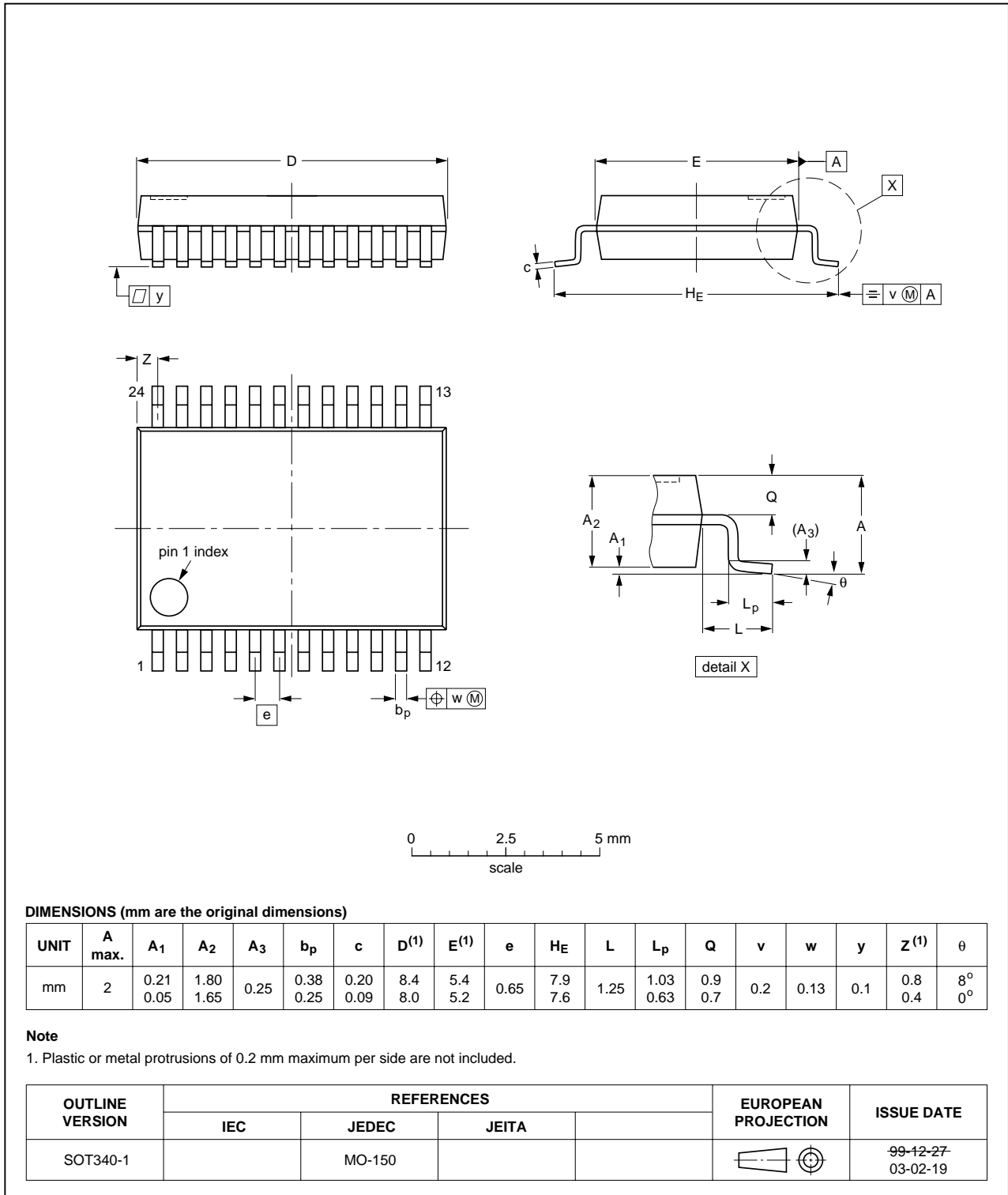


Fig 10. Package outline SOT340-1 (SSOP24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

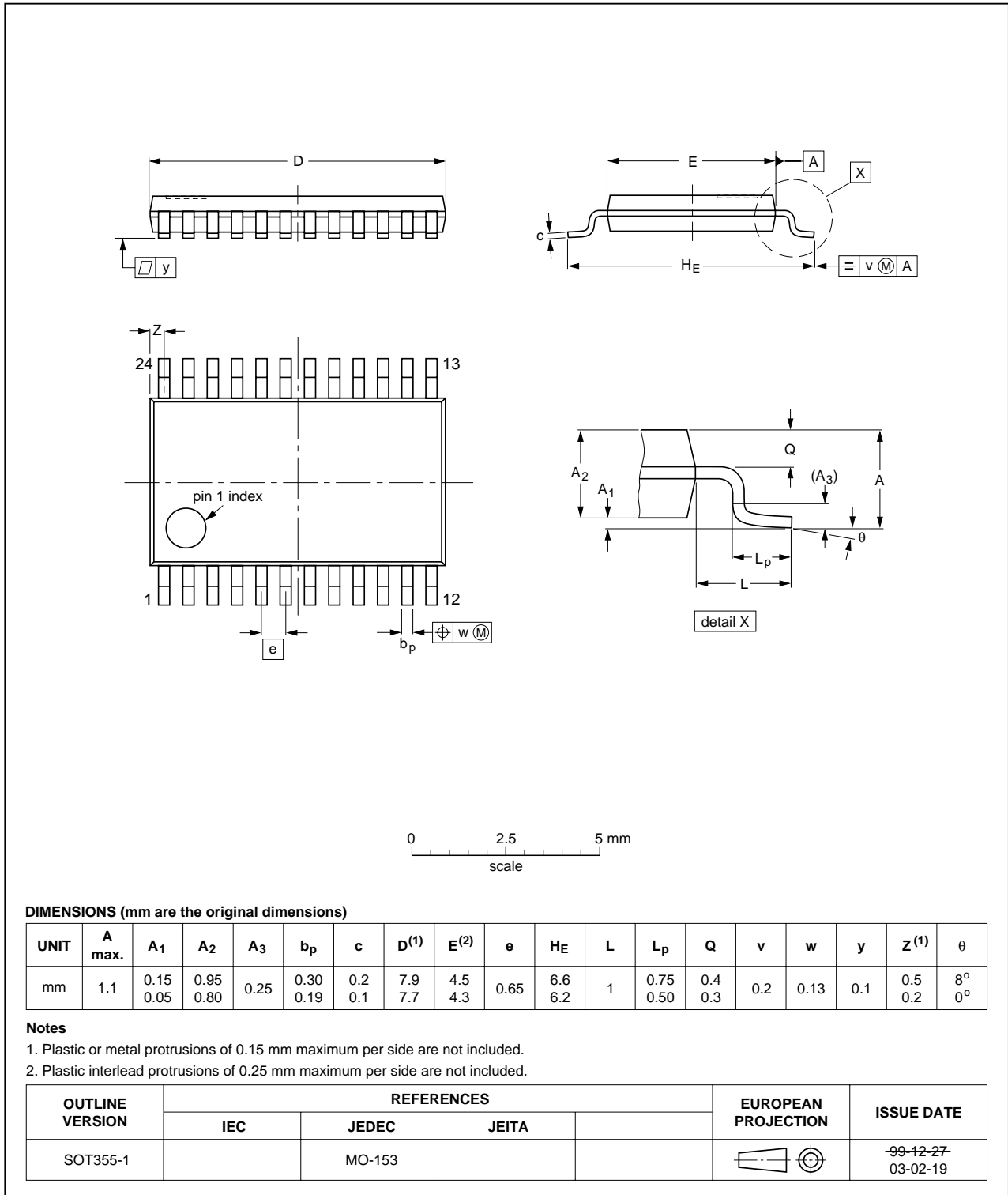


Fig 11. Package outline SOT355-1 (TSSOP24)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT821_3	20100225	Product data sheet	-	74ABT821_2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. DIP 24 (SOT222-1) package removed from Section 3 “Ordering information” and Section 12 “Package outline”. 			
74ABT821_2	20050412	Product specification	-	74ABT821
74ABT821	19950906	Product specification	-	-

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Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[2] The term 'short data sheet' is explained in section "Definitions".

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