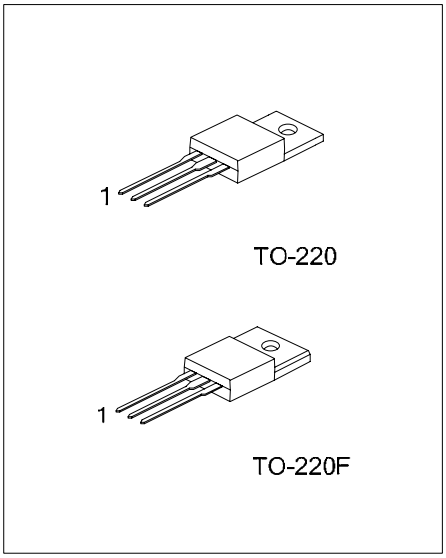
7N60A

Power MOSFET

7 Amps, 600/650 Volts N-CHANNEL MOSFET



*Pb-free plating product number:7N60AL

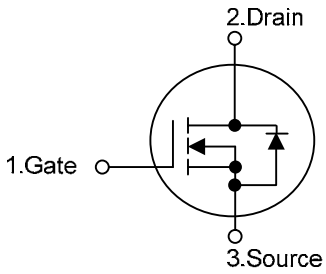
■ DESCRIPTION

The UTC 7N60A is a high voltage N-Channel enhancement mode power field effect transistors and is designed to have minimize on-state resistance , provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. This power MOSFET is well suited for high efficiency switch mode power supply.

■ FEATURES

* $R_{DS(ON)}$ = 1.2Ω @V_{GS} = 10 V
* Ultra low gate charge (typical 28 nC)
* Low reverse transfer Capacitance (C_{RSS}= typical 12 pF)
* Fast switching capability
* Avalanche energy tested
* Improved dv/dt capability, high ruggedness

■ SYMBOL



■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Normal	Lead Free Plating		1	2	3	
7N60A-x-TA3-T	7N60AL-x-TA3-T	TO-220	G	D	S	Tube
7N60A-x-TF3-T	7N60AL-x-TF3-T	TO-220F	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

7N60AL-x-TA3-T
(1)Packing Type
(2)Package Type
(3)Drain-Source Voltage
(4)Lead Plating

(1) T: Tube
(2) TA3: TO-220, TF3: TO-220F
(3) A: 600V, B: 650V
(4) L: Lead Free Plating, Blank: Pb/Sn

■ ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage	7N60A-A	V_{DSS}	600	V
	7N60A-B		650	V
Gate-Source Voltage		V_{GSS}	±30	V
Avalanche Current (Note 1)		I_{AR}	7	A
Continuous Drain Current	T_C = 25°C	I_D	7	A
	T_C = 100°C		3.2	A
Pulsed Drain Current (Note 1)		I_{DM}	28	A
Avalanche Energy	Single Pulsed (Note 2)	E_{AS}	330	mJ
	Repetitive Limited by $T_{J(MAX)}$	E_{AR}	7.5	mJ
Power Dissipation		P_D	30	W
Junction Temperature		T_J	+150	°C
Operating Temperature		T_{OPR}	-55 ~ +150	°C
Storage Temperature		T_{STG}	-55 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Junction-to-Ambient	θ_{JA}			62.5	°C/W
Junction-to-Case	θ_{JC}			4.16	°C/W

■ ELECTRICAL CHARACTERISTICS (T_C =25°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage	7N60A-A	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	600			V
	7N60A-B			650			V
Drain-Source Leakage Current		I_{DSS}	V_{DS} = 600V, V_{GS} = 0V			1	μA
Gate-Source Leakage Current		I_{GSS}	V_{DS} = ±30V, V_{GS} = 0V			±100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS} = 10V, I_D = 3.5A (Note 4)		1.0	1.2	Ω
DYNAMIC CHARACTERISTICS							
Input Capacitance		C_{ISS}	V_{DS}=25V, V_{GS}=0V, f=1.0 MHz		950	1430	pF
Output Capacitance		C_{OSS}			85	130	pF
Reverse Transfer Capacitance		C_{RSS}			12	18	pF
SWITCHING CHARACTERISTICS							
Turn-On Delay Time		$t_{D(ON)}$	V_{DD}=300V, I_D =7A, R_G =25Ω (Note 3, 4)		16		ns
Turn-On Rise Time		t_R			60		ns
Turn-Off Delay Time		$t_{D(OFF)}$			80		ns
Turn-Off Fall Time		t_F			65		ns
Total Gate Charge		Q_G	V_{DS}=300V, I_D=7A, V_{GS}=10 V (Note 3, 4)		28	42	nC
Gate-Source Charge		Q_{GS}			5.5	8.3	nC
Gate-Drain Charge		Q_{GD}			11	17	nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
Drain-Source Diode Forward Voltage (Note 4)		V_{SD}	V_{GS} = 0V, I_S = 7A			1.4	V
Maximum Continuous Drain-Source Diode Forward Current		I_S				7	A
Maximum Pulsed Drain-Source Diode Forward Current (Note 1)		I_{SM}				28	A
Reverse Recovery Time		t_{RR}	V_{GS} = 0V, I_S = 7A, dI_F / dt = 100A/μs		365		ns
Reverse Recovery Charge		Q_{RR}			4.23		μC

■ ELECTRICAL CHARACTERISTICS(Cont.)

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 9.8mH, I_{AS} = 7A, V_{DD}=50V, R_G = 27 Ω
3. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%
4. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

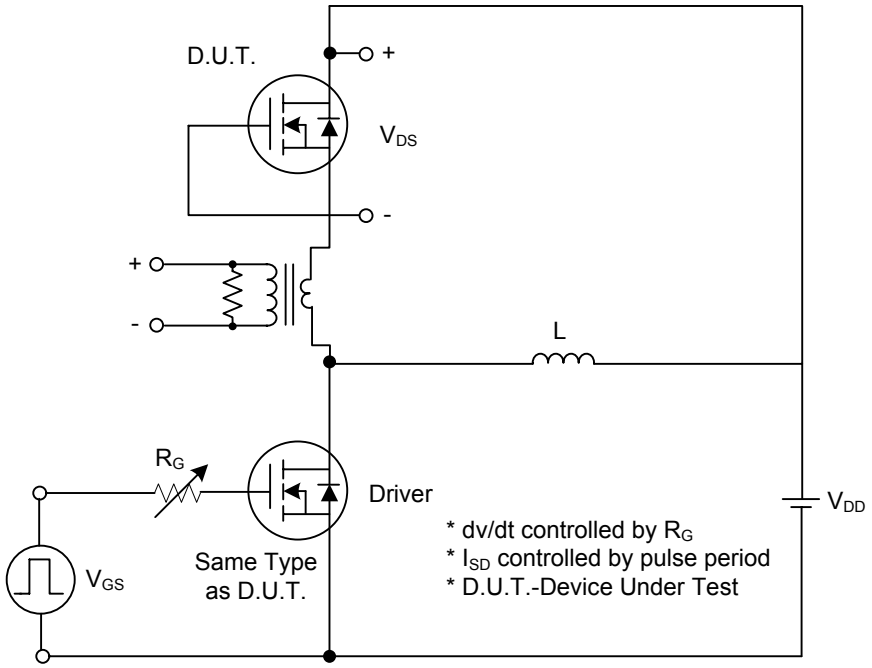


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

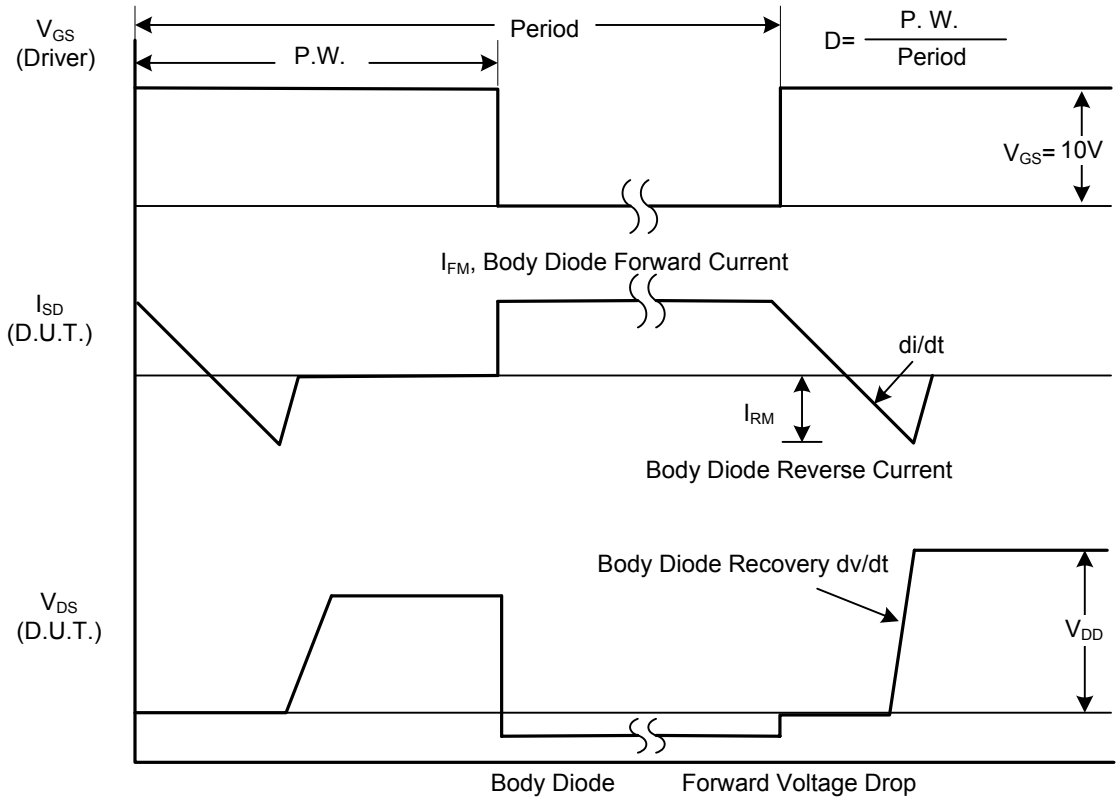


Fig. 1B Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

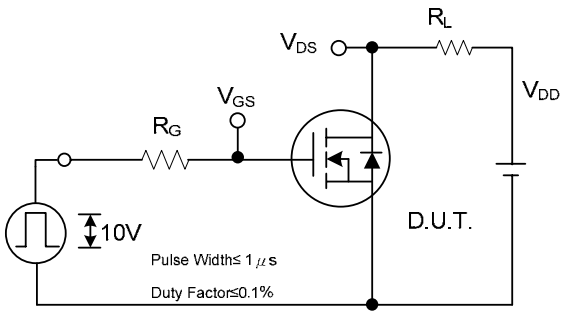


Fig. 2A Switching Test Circuit

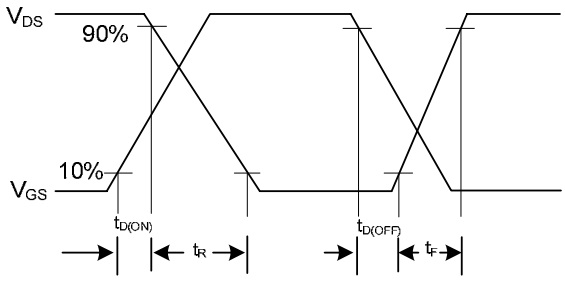


Fig. 2B Switching Waveforms

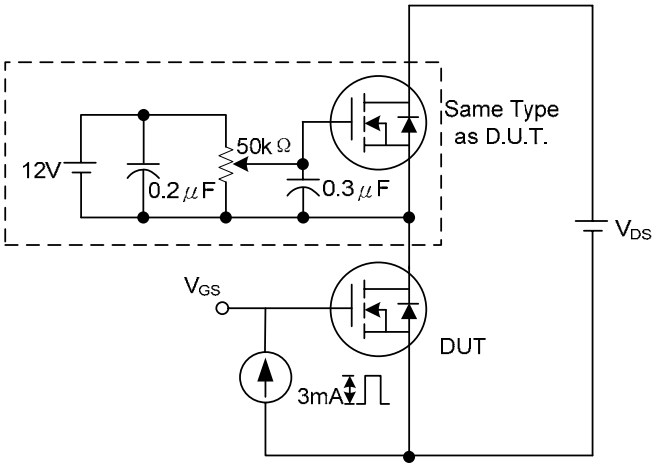


Fig. 3A Gate Charge Test Circuit

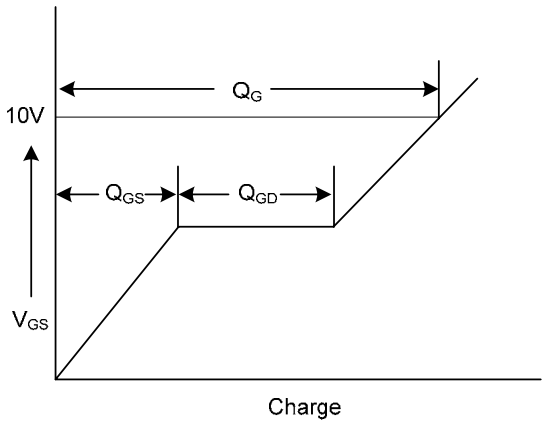


Fig. 3B Gate Charge Waveform

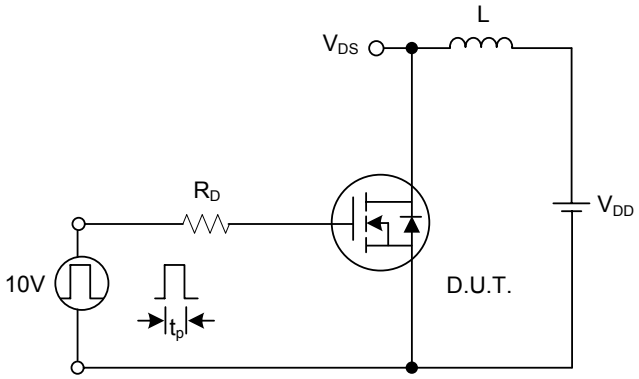


Fig. 4A Unclamped Inductive Switching Test Circuit

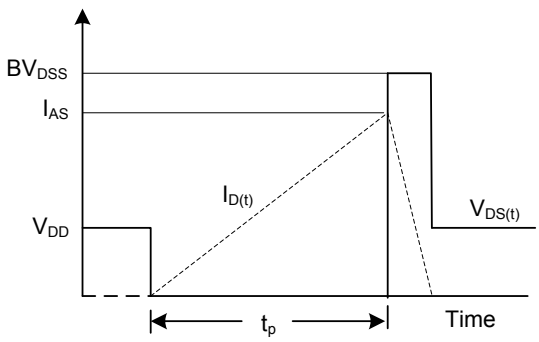
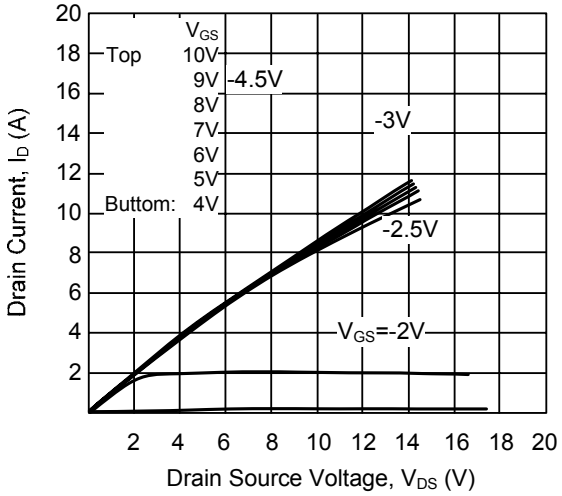


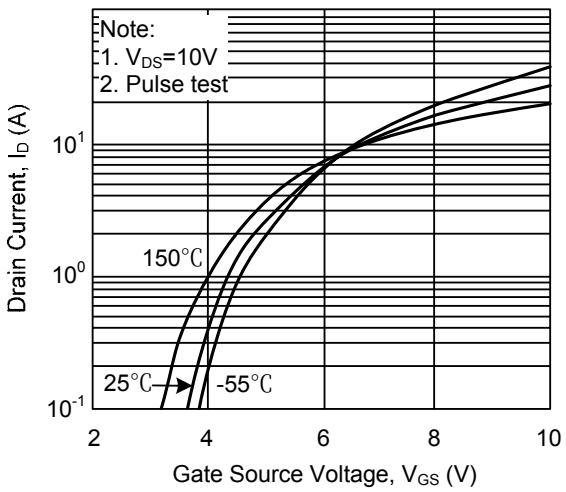
Fig. 4B Unclamped Inductive Switching Waveforms

■ TYPICAL CHARACTERISTICS

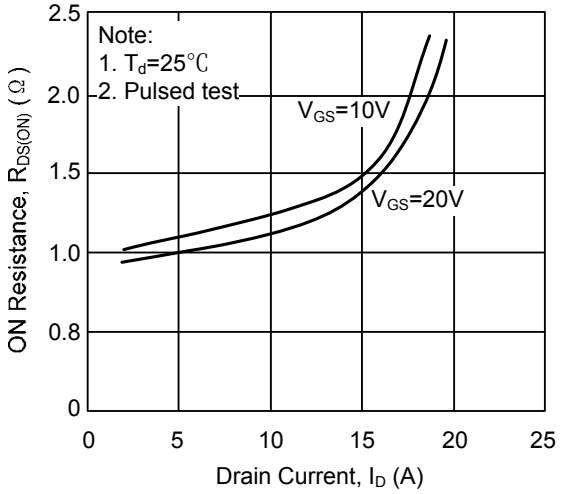
Drain Current vs. Drain-Source Voltage



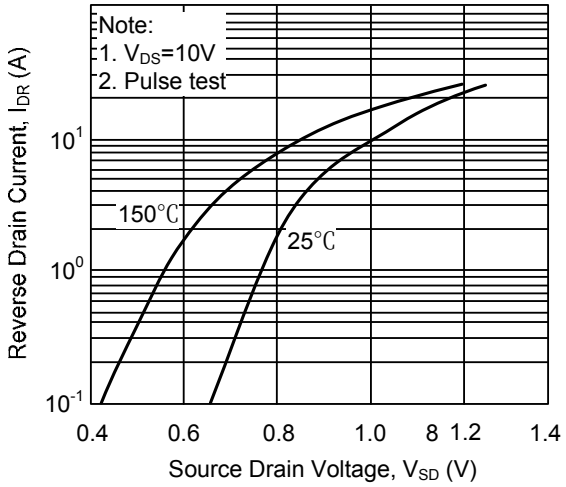
Drain Current vs. Gate-Source Voltage



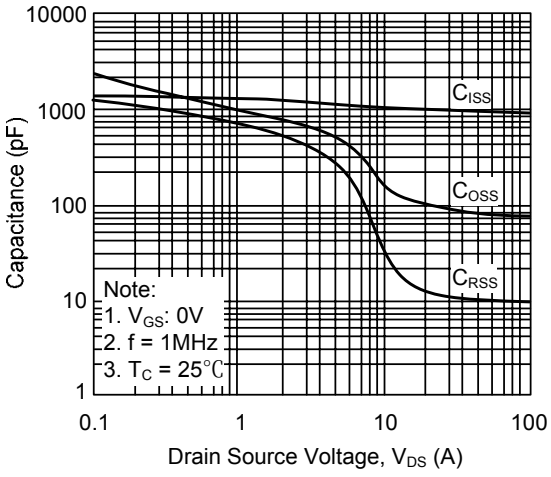
ON Resistance vs. Drain Current



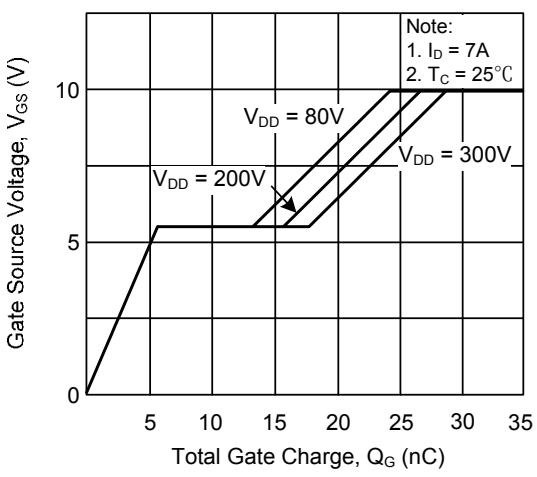
Reverse Drain Current vs. Source Drain Voltage



Capacitance vs. Drain Source Voltage

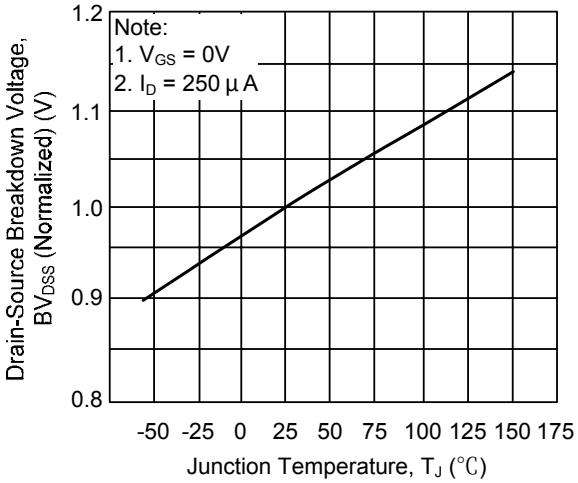


Gate Source Voltage vs. Total Gate Charge

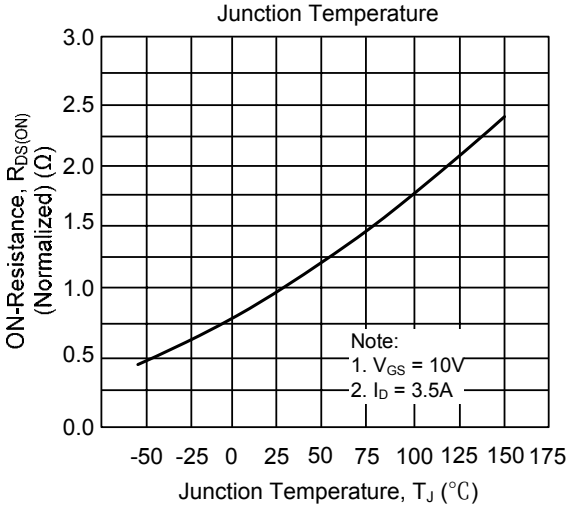


■ TYPICAL CHARACTERISTICS (Cont.)

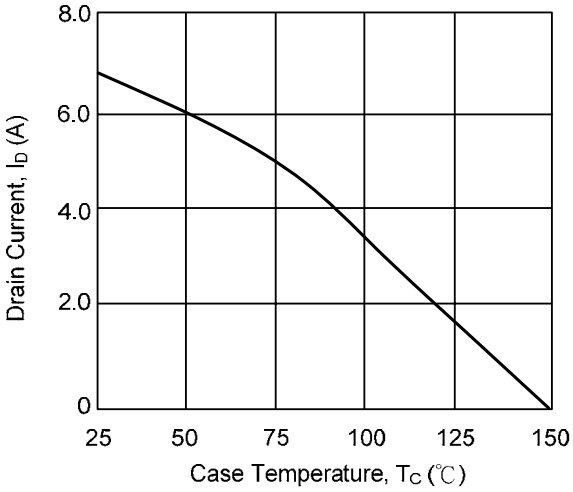
Drain-Source Voltage vs. Junction Temperature



ON-Resistance vs. Junction Temperature



Drain Current vs. Case Temperature



Safe Operating Area