HD74ALVCH16501

18-bit Universal Bus Transceivers with 3-state Outputs

REJ03D0036-0300Z
(Previous ADE-205-168A(Z))
Rev.3.00
Oct.02.2003

Description

Data flow in each direction is controlled by output enable (OEAB and $\overline{\text{OEBA}}$), latch enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A to B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch flip flop on the low to high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high impedance state. Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA. The output enables are complementary (OEAB is active high, and $\overline{\text{OEBA}}$ is active low). Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Features

- V_{CC} = 2.3 V to 3.6 V
- Typical V_{OL} ground bounce < 0.8 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Typical V_{OH} undershoot > 2.0 V (@V_{CC} = 3.3 V, Ta = 25°C)
- High output current ±24 mA (@V_{CC} = 3.0 V)
- Bus hold on data inputs eliminates the need for external pullup / pulldown resistors

Function Table [*3]

Inputs				Output B
OEAB	LEAB	CLKAB	A	
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	□	L	L
H	L	□	H	H
H	L	H	X	B0 *1
H	L	L	X	B0 *2

H : High level

L : Low level

X : Immaterial

Z : High impedance

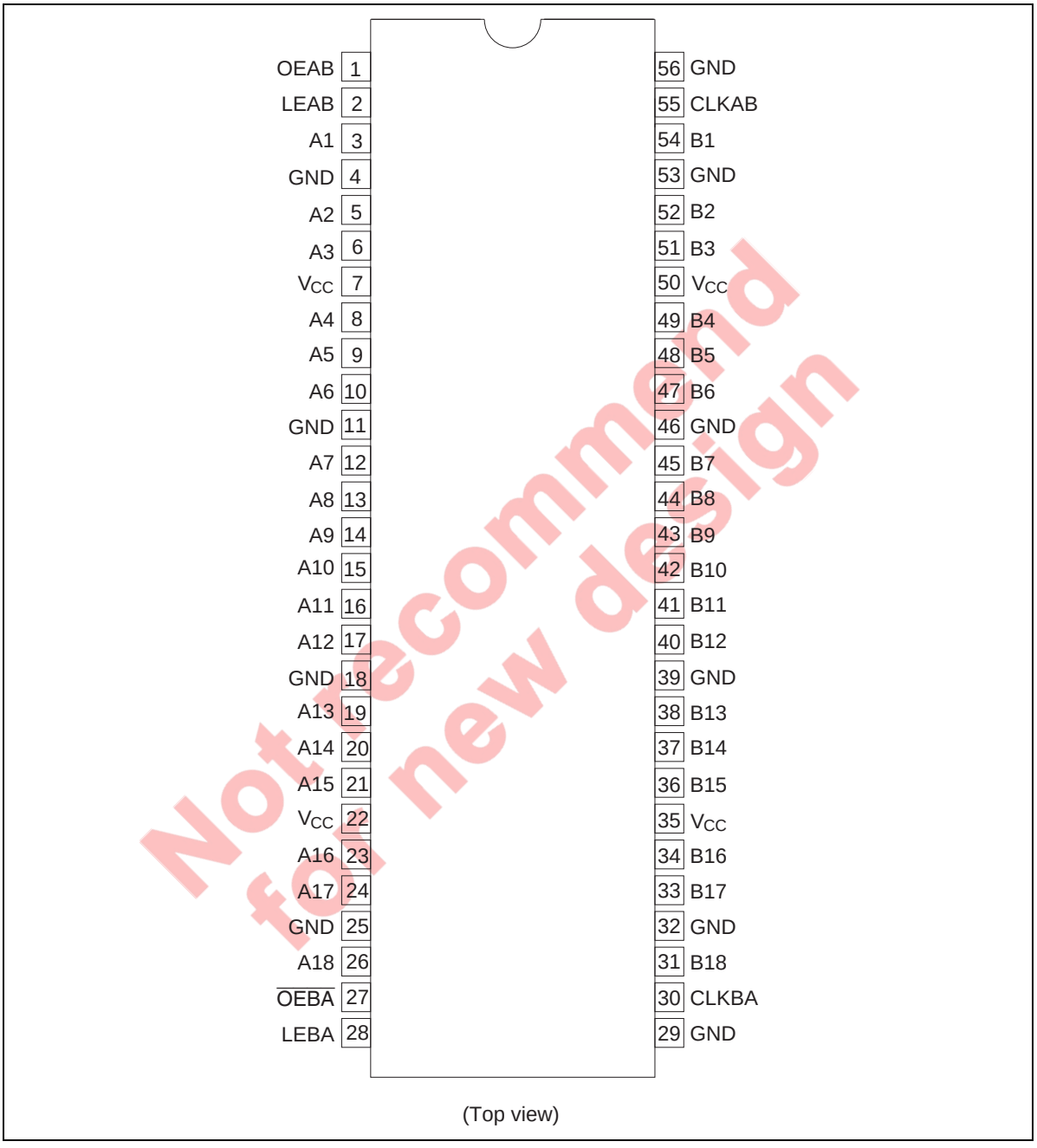
↑ : Low to high transition

Notes: 1. Output level before the indicated steady state input conditions were established.

2. Output level before the indicated steady state input conditions were established, provided that CLKAB was high before LEAB went low.

3. A to B data flow is show; B to A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA.

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	–0.5 to 4.6	V	
Input voltage [*1, 2]	V_I	–0.5 to 4.6	V	Except I/O ports
		–0.5 to V_{CC} +0.5		I/O ports
Output voltage [*1, 2]	V_O	–0.5 to V_{CC} +0.5	V	
Input clamp current	I_{IK}	–50	mA	V_I < 0
Output clamp current	I_{OK}	±50	mA	V_O < 0 or V_O > V_{CC}
Continuous output current	I_O	±50	mA	V_O = 0 to V_{CC}
		±100		
Maximum power dissipation at Ta = 55°C (in still air) [*3]	P_T	1	W	TSSOP
Storage temperature	Tstg	–65 to 150	°C	

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

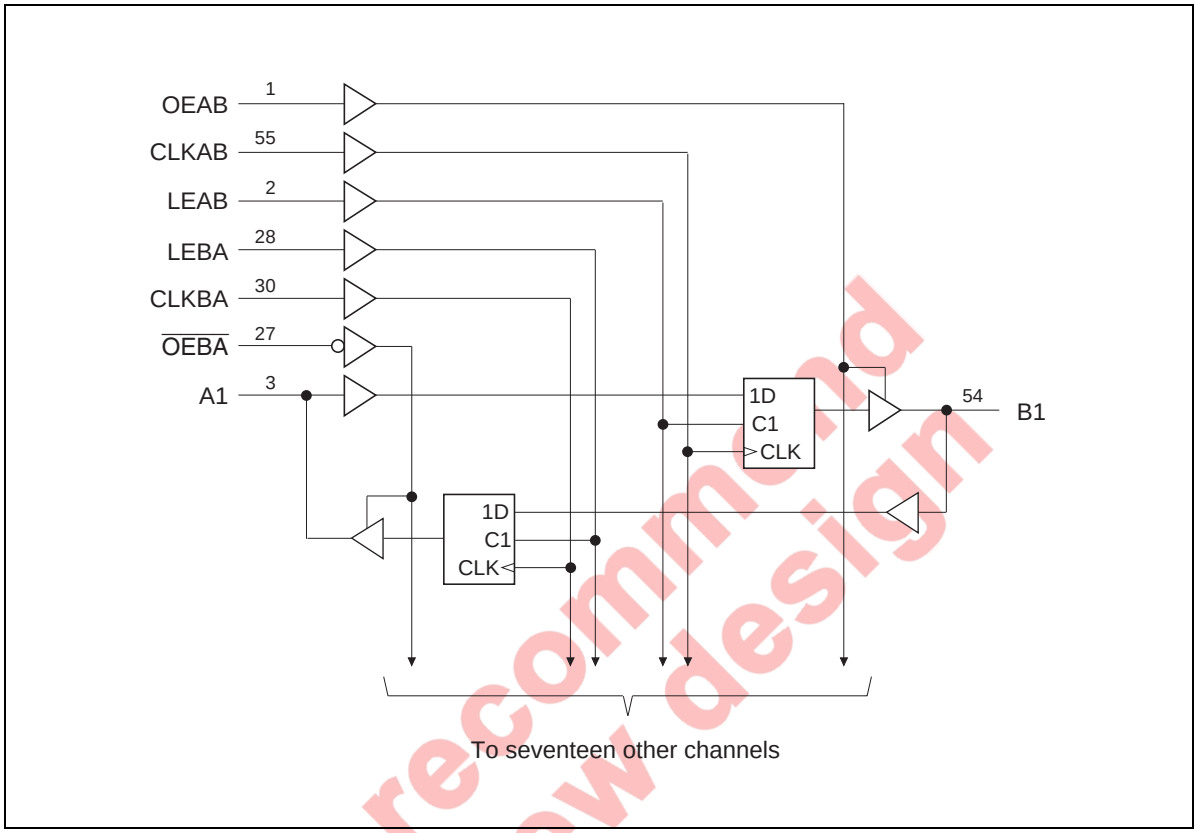
1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

Recommended DC Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{CC}	2.3	3.6	V	
Input voltage	V_I	0	V_{CC}	V	
Output voltage	V_O	0	V_{CC}	V	
High level output current	I_{OH}	—	–12	mA	V_{CC} = 2.3 V
		—	–12		V_{CC} = 2.7 V
		—	–24		V_{CC} = 3.0 V
Low level output current	I_{OL}	—	12	mA	V_{CC} = 2.3 V
		—	12		V_{CC} = 2.7 V
		—	24		V_{CC} = 3.0 V
Input transition rise or fall rate	$\Delta t / \Delta v$	0	10	ns / V	
Operating temperature	Ta	–40	85	°C	

Note: Unused control inputs must be held high or low to prevent them from floating.

Logic Diagram



Electrical Characteristics

(Ta = –40 to 85°C)

Item	Symbol	V_{CC} (V) [*1]	Min	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.3 to 2.7	1.7	—	V	
		2.7 to 3.6	2.0	—		
	V_{IL}	2.3 to 2.7	—	0.7		
		2.7 to 3.6	—	0.8		
Output voltage	V_{OH}	Min to Max	V_{CC}–0.2	—	V	I_{OH} = –100 µA
		2.3	2.0	—		I_{OH} = –6 mA, V_{IH} = 1.7 V
		2.3	1.7	—		I_{OH} = –12 mA, V_{IH} = 1.7 V
		2.7	2.2	—		I_{OH} = –12 mA, V_{IH} = 2.0 V
		3.0	2.4	—		I_{OH} = –12 mA, V_{IH} = 2.0 V
		3.0	2.0	—		I_{OH} = –24 mA, V_{IH} = 2.0 V
	V_{OL}	Min to Max	—	0.2		I_{OL} = 100 µA
		2.3	—	0.4		I_{OL} = 6 mA, V_{IL} = 0.7 V
		2.3	—	0.7		I_{OL} = 12 mA, V_{IL} = 0.7 V
		2.7	—	0.4		I_{OL} = 12 mA, V_{IL} = 0.8 V
		3.0	—	0.55		I_{OL} = 24 mA, V_{IL} = 0.8 V
Input current	I_{IN}	3.6	—	±5	µA	V_{IN} = V_{CC} or GND
	$I_{IN\ (hold)}$	2.3	45	—		V_{IN} = 0.7 V
		2.3	–45	—		V_{IN} = 1.7 V
		3.0	75	—		V_{IN} = 0.8 V
		3.0	–75	—		V_{IN} = 2.0 V
		3.6	—	±500		V_{IN} = 0 to 3.6 V
Off state output current [*2]	I_{OZ}	3.6	—	±10	µA	V_{OUT} = V_{CC} or GND
Quiescent supply current	I_{CC}	3.6	—	40	µA	V_{IN} = V_{CC} or GND
	ΔI_{CC}	3.0 to 3.6	—	750	µA	V_{IN} = one input at (V_{CC}–0.6) V, other inputs at V_{CC} or GND

Notes: 1. For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

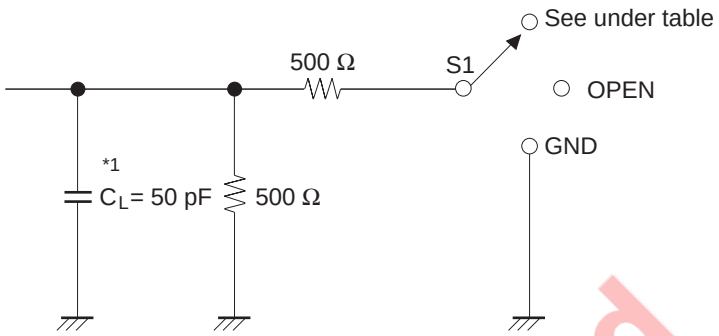
2. For I/O ports, the parameter I_{OZ} includes the input leakage current.

Switching Characteristics

(Ta = 40 to 85°C)

Item	Symbol	V_{CC} (V)	Min	Typ	Max	Unit	FROM (Input)	TO (Output)
Maximum clock frequency	f_{max}	2.5±0.2	150	—	—	MHz		
		2.7	150	—	—			
		3.3±0.3	150	—	—			
Propagation delay time	t_{PLH}	2.5±0.2	1.2	—	4.8	ns	A or B	B or A
	t_{PHL}	2.7	—	—	4.5			
		3.3±0.3	1.0	—	3.9			
		2.5±0.2	1.6	—	5.7		LE	A or B
		2.7	—	—	5.3			
		3.3±0.3	1.3	—	4.6			
		2.5±0.2	1.7	—	6.1		CLK	A or B
		2.7	—	—	5.6			
		3.3±0.3	1.4	—	4.9			
Output enable time	t_{ZH}	2.5±0.2	1.1	—	5.8	ns	OEAB	B
	t_{ZL}	2.7	—	—	5.3			
		3.3±0.3	1.0	—	4.6			
		2.5±0.2	1.4	—	6.3		$\overline{OEBA}$	A
		2.7	—	—	6.0			
		3.3±0.3	1.1	—	5.0			
Output disable time	t_{HZ}	2.5±0.2	2.2	—	6.2	ns	OEAB	B
	t_{LZ}	2.7	—	—	5.7			
		3.3±0.3	1.4	—	5.0			
		2.5±0.2	2.0	—	5.3		$\overline{OEBA}$	A
		2.7	—	—	4.6			
		3.3±0.3	1.3	—	4.2			
Input capacitance	C_{IN}	3.3	—	4.0	—	pF	Control inputs	
Output capacitance	$C_{IN / O}$	3.3	—	8.0	—	pF	A or B ports	

• **Test Circuit**

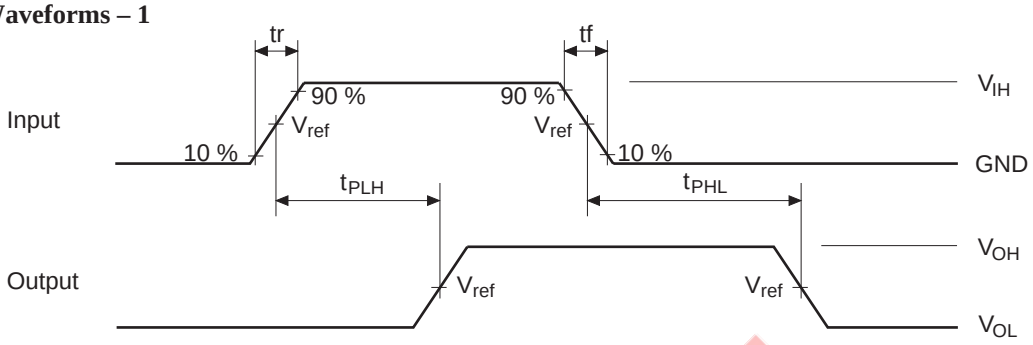


Load Circuit for Outputs

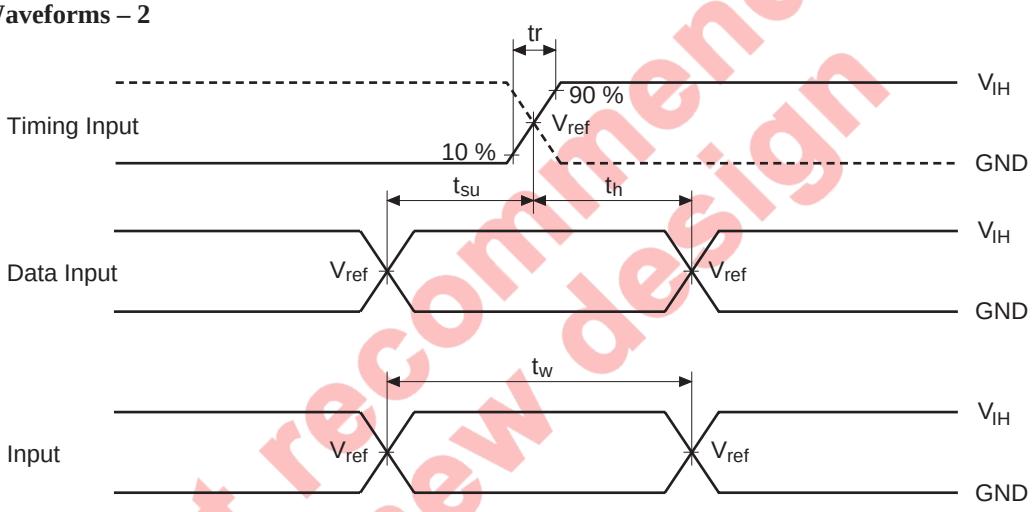
Symbol	Vcc=2.5±0.2 V	Vcc = 2.7 V, 3.3±0.3 V
t_{PLH} / t_{PHL}	OPEN	OPEN
t_{su} / t_h / t_w		
t_{ZH} / t_{HZ}	GND	GND
t_{ZL} / t_{LZ}	4.6 V	6.0 V

Note: 1. C_L includes probe and jig capacitance.

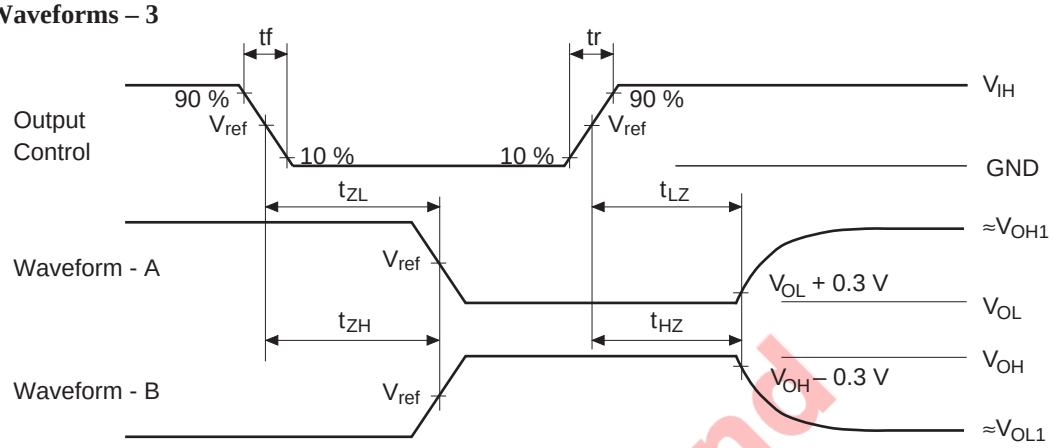
• **Waveforms – 1**



• **Waveforms – 2**



• **Waveforms – 3**



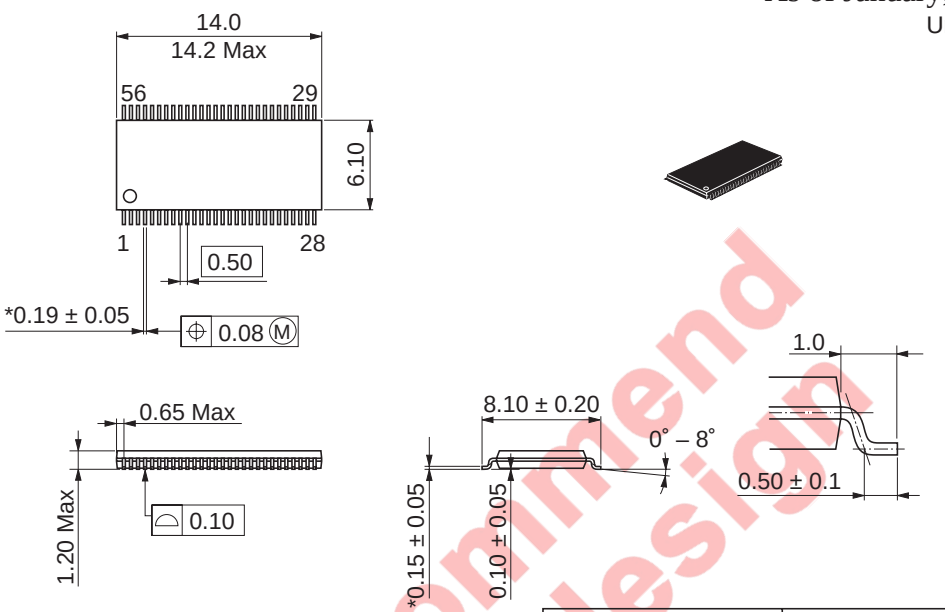
TEST	Vcc=2.5±0.2V	Vcc=2.7V, 3.3±0.3V
V_{IH}	2.3 V	2.7 V
V_{ref}	1.2 V	1.5 V
V_{OH1}	2.3 V	3.0 V
V_{OL1}	GND	GND

Notes: 1. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Zo = 50 Ω, tr ≤ 2.5 ns, tf ≤ 2.5 ns.
2. Waveform – A is for an output with internal conditions such that the output is low except when disabled by the output control.
3. Waveform – B is for an output with internal conditions such that the output is high except when disabled by the output control.
4. The output are measured one at a time with one transition per measurement.

Package Dimensions

As of January, 2003

Unit: mm



*Ni/Pd/Au plating

Package Code	TTP-56DAV
JEDEC	—
JEITA	—
Mass (reference value)	0.23 g

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

http://www.renesas.com

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
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Renesas Technology Europe Limited.
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

Renesas Technology Europe GmbH
Dornacher Str. 3, D-85622 Feldkirchen, Germany
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

Renesas Technology Hong Kong Ltd.
7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2375-6836

Renesas Technology Taiwan Co., Ltd.
FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Colophon 1.0