19-4815; Rev 1; 3/10

EVALUATION KIT AVAILABLE

Low-Cost, 3A, 4.5V to 28V Input, 350kHz, PWM Step-Down DC-DC Regulator with Internal Switches

General Description

The MAX15041 low-cost, synchronous DC-DC converter with internal switches delivers an output current up to 3A. The MAX15041 operates from an input voltage of 4.5V to 28V and provides an adjustable output voltage from 0.606V to 90% of V_{IN}, set with two external resistors. The MAX15041 is ideal for distributed power systems, preregulation, set-top boxes, television, and other consumer applications.

The MAX15041 features a peak-current-mode PWM controller with internally fixed 350kHz switching frequency and a 90% maximum duty cycle. The current-mode control architecture simplifies compensation design, and ensures a cycle-by-cycle current limit and fast response to line and load transients. A high-gain transconductance error amplifier allows flexibility in setting the external compensation by using a type II compensation scheme, thereby allowing the use of all ceramic capacitors.

This synchronous buck regulator features internal MOSFETs that provide better efficiency than asynchronous solutions, while simplifying the design relative to discrete controller solutions. In addition to simplifying the design, the integrated MOSFETs minimize EMI, reduce board space, and provide higher reliability by minimizing the number of external components.

The MAX15041 also features thermal shutdown and overcurrent protection (high-side sourcing and low-side sinking), and an internal 5V LDO with undervoltage lockout. In addition, this device ensures safe startup when powering into a prebiased output.

Other features include an externally adjustable soft-start that gradually ramps up the output voltage and reduces inrush current. Independent enable control and power-good signals allow for flexible power sequencing.

The MAX15041 is available in a space-saving, high-power, 3mm x 3mm, 16-pin TQFN-EP package and is fully specified from -40°C to +85°C.

Applications

Distributed Power Systems

Wall Adapters

Preregulators

Set-Top Boxes

Televisions

xDSL Modems

Consumer Products

Features

- Up to 3A of Continuous Output Current
- ±1% Output Accuracy Over Temperature
- 4.5V to 28V Input Voltage Range
- Adjustable Output Voltage Range from 0.606V to 0.9 x V_{IN}
- Internal 170mΩ R_{DS-ON} High-Side and 105mΩ R_{DS-ON} Low-Side Power Switches
- Fixed 350kHz Switching Frequency
- Up to 93% Efficiency
- Cycle-By-Cycle Overcurrent Protection
- Programmable Soft-Start
- Stable with Low-ESR Ceramic Output Capacitors
- Safe Startup into Prebiased Output
- Enable Input and Power-Good Output
- Fully Protected Against Overcurrent and Overtemperature
- V_{DD} LDO Undervoltage Lockout
- Space-Saving, Thermally Enhanced, 3mm x 3mm Package

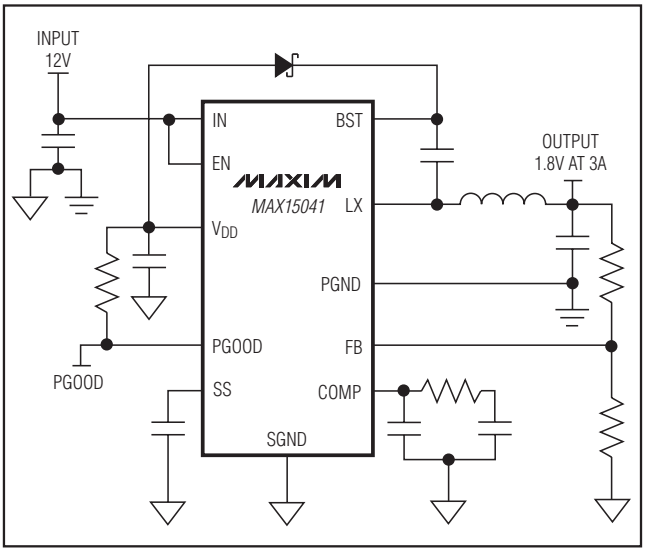
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX15041ETE+	-40°C to +85°C	16 TQFN-EP*	AGV

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Typical Operating Circuit



Low-Cost, 3A, 4.5V to 28V Input, 350kHz, PWM Step-Down DC-DC Regulator with Internal Switches

ABSOLUTE MAXIMUM RATINGS

IN to SGND .....-0.3V to +30V
EN to SGND .....-0.3V to (V_{IN} + 0.3V)
LX to PGND .....-0.3V to min (+30V, V_{IN} + 0.3V)
LX to PGND .....-1V to min (+30V, V_{IN} + 0.3V) for 50ns
PGOOD to SGND .....-0.3V to +6V
V_{DD} to SGND.....-0.3V to +6V
COMP, FB, SS to SGND.....-0.3V to min (+6V, V_{DD} + 0.3V)
BST to LX .....-0.3V to +6V
BST to SGND .....-0.3V to +36V
SGND to PGND .....-0.3V to +0.3V
LX Current (Note 1) .....-5A to +8A
Converter Output Short-Circuit Duration .....Continuous

Continuous Power Dissipation (T_A = +70°C)
16-Pin TQFN (derate 14.7mW/°C above +70°C)
Multilayer Board 1666mW
Package Thermal Resistance (Note 2)
θ_{JA} .....48°C/W
θ_{JC} .....7°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: LX has internal clamp diodes to PGND and IN. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation.

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.**maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, C_{VDD} = 1µF, C_{IN} = 22µF, T_A = T_J = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STEP-DOWN CONVERTER						
Input-Voltage Range	V_{IN}		4.5		28	V
Input Supply Current	I_{IN}	Switching		2.1	4	mA
Shutdown Input Supply Current		V_{EN} = 0V, V_{DD} regulated by internal LDO		2	12	µA
		V_{EN} = 0V, V_{IN} = V_{DD} = 5V		18	28	
ENABLE INPUT						
EN Shutdown Threshold Voltage	V_{EN_SHDN}	V_{EN} rising		1.4		V
EN Shutdown Voltage Hysteresis	V_{EN_HYST}			100		mV
EN Lockout Threshold Voltage	V_{EN_LOCK}	V_{EN} rising	1.7	1.95	2.15	V
	$V_{EN\_LOCK\_HYST}$			100		mV
EN Input Current	I_{EN}	V_{EN} = 2.9V	2	5.3	9	µA
POWER-GOOD OUTPUT						
PGOOD Threshold	V_{PGOOD_TH}	V_{FB} rising	540	560	584	mV
PGOOD Threshold Hysteresis	V_{PGOOD_HYST}			15		mV
PGOOD Output Low Voltage	V_{PGOOD_OL}	I_{PGOOD} = 5mA, V_{FB} = 0.5V		35	100	mV
PGOOD Leakage Current	I_{PGOOD}	V_{PGOOD} = 5V, V_{FB} = 0.7V		10		nA
ERROR AMPLIFIER						
Error Amplifier Transconductance	g_{MV}			1.6		mS
Error Amplifier Voltage Gain	A_{VEA}			90		dB
FB Set-Point Accuracy	V_{FB}		600	606	612	mV
FB Input Bias Current	I_{FB}	V_{FB} = 0.5V	-100		+100	nA
		V_{FB} = 0.7V	-100		+100	

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, C_{VDD} = 1µF, C_{IN} = 22µF, T_A = T_J = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SS Current	I_{SS}	V_{SS} = 0.45V, sourcing	4.5	5	5.5	µA
SS Discharge Resistance	R_{SS}	I_{SS} = 10mA, sinking, V_{EN} = 1.6V		6		Ω
SS Prebiased Mode Stop Voltage				0.65		V
Current Sense to COMP Transconductance	G_{MOD}			9		S
COMP Clamp Low		V_{FB} = 0.7V		0.68		V
PWM Compensation Ramp Valley				830		mV
PWM CLOCK						
Switching Frequency	f_{SW}		315	350	385	kHz
Maximum Duty Cycle	D			90		%
Minimum Controllable On-Time				150		ns
INTERNAL LDO OUTPUT (V_{DD})						
V_{DD} Output Voltage	V_{DD}	I_{VDD} = 1mA to 25mA, V_{IN} = 6.5V	4.75	5.1	5.5	V
V_{DD} Short-Circuit Current		V_{IN} = 6.5V	30	80		mA
LDO Dropout Voltage		I_{VDD} = 25mA, V_{DD} drops by -2%		250	600	mV
V_{DD} Undervoltage Lockout Threshold	V_{UVLO_TH}	V_{DD} rising		4	4.25	V
V_{DD} Undervoltage Lockout Hysteresis	V_{UVLO_HYST}			150		mV
POWER SWITCH						
LX On-Resistance		High-side switch, I_{LX} = 1A		170	305	mΩ
		Low-side switch, I_{LX} = 1A		105	175	
High-Side Switch Source Current-Limit Threshold			5	6	7.2	A
Low-Side Switch Sink Current-Limit Threshold				-3		A
LX Leakage Current		V_{BST} = 33V, V_{IN} = V_{LX} = 28V		10		nA
		V_{BST} = 5V, V_{IN} = 28V, V_{LX} = 0V		10		
BST Leakage Current		V_{BST} = 33V, V_{IN} = V_{LX} = 28V		10		nA
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold		Rising		+155		°C
Thermal-Shutdown Hysteresis				20		°C
HICCUP PROTECTION						
Blanking Time				16 x Soft-Start Time		

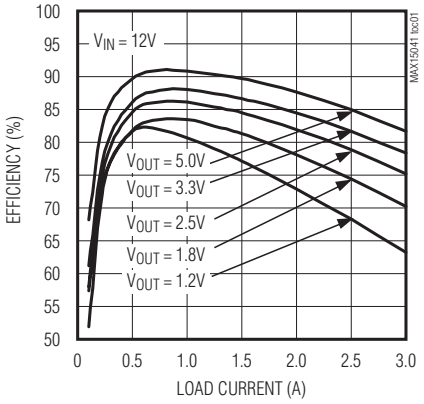
Note 3: Specifications are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.

Low-Cost, 3A, 4.5V to 28V Input, 350kHz, PWM Step-Down DC-DC Regulator with Internal Switches

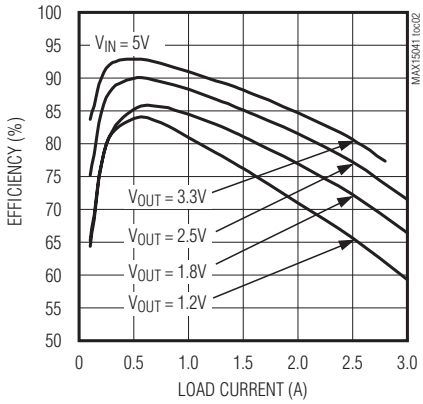
Typical Operating Characteristics

(V_{IN} = 12V, V_{OUT} = 3.3V, C_{VDD} = 1µF, C_{IN} = 22µF, T_A = +25°C, circuit of Figure 3 (see Table 1 for values), unless otherwise specified.)

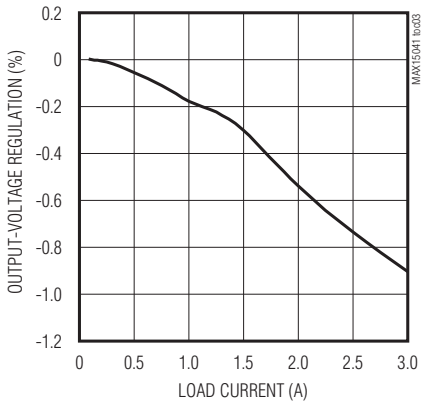
EFFICIENCY vs. LOAD CURRENT



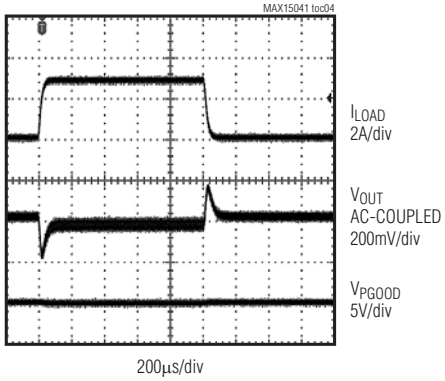
EFFICIENCY vs. LOAD CURRENT



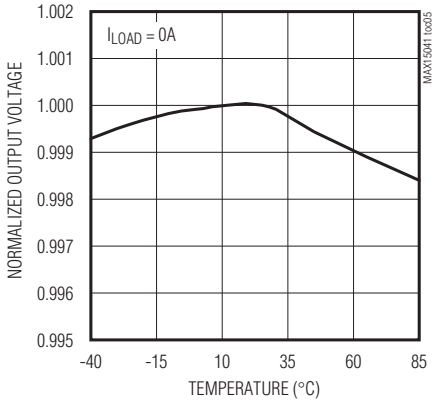
OUTPUT-VOLTAGE REGULATION vs. LOAD CURRENT



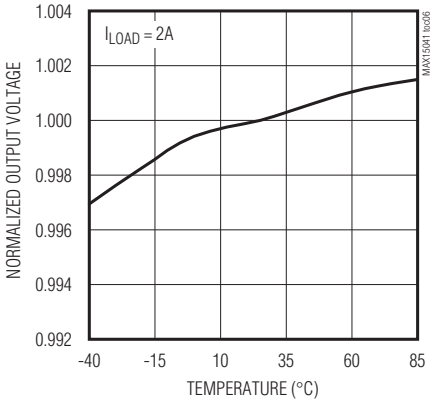
LOAD-TRANSIENT WAVEFORMS



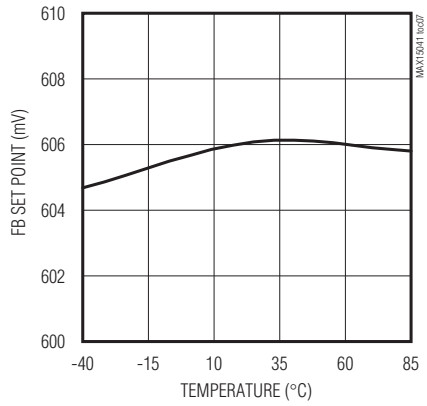
NORMALIZED OUTPUT VOLTAGE vs. TEMPERATURE



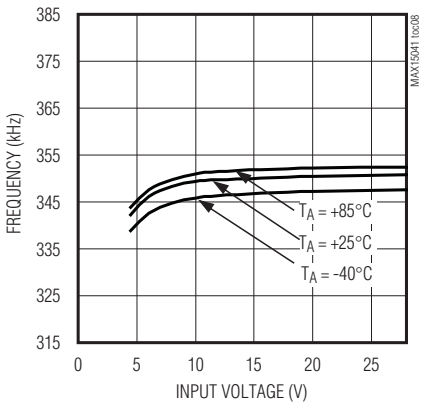
NORMALIZED OUTPUT VOLTAGE vs. TEMPERATURE



FB SET POINT vs.TEMPERATURE



SWITCHING FREQUENCY vs. INPUT VOLTAGE

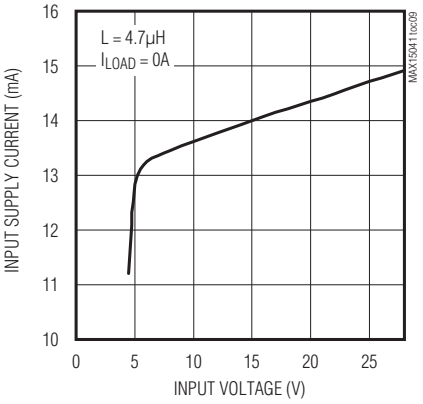


Low-Cost, 3A, 4.5V to 28V Input, 350kHz, PWM Step-Down DC-DC Regulator with Internal Switches

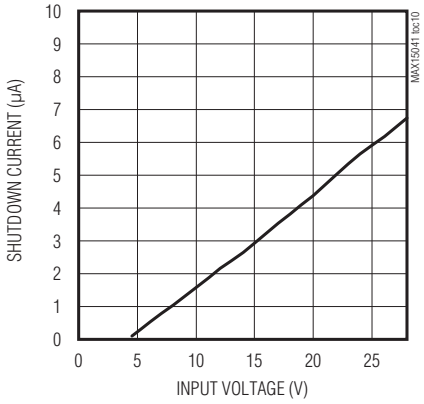
Typical Operating Characteristics (continued)

(V_{IN} = 12V, V_{OUT} = 3.3V, C_{VDD} = 1µF, C_{IN} = 22µF, T_A = +25°C, circuit of Figure 3 (see Table 1 for values), unless otherwise specified.)

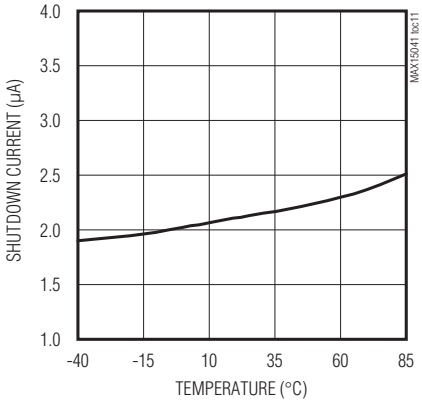
INPUT SUPPLY CURRENT vs. INPUT VOLTAGE



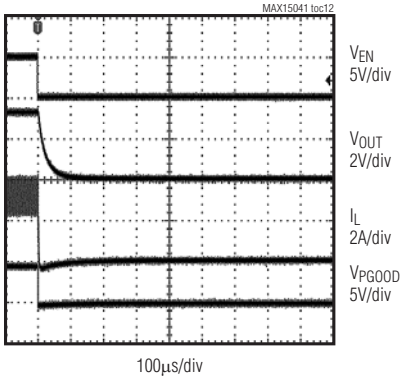
SHUTDOWN CURRENT vs. INPUT VOLTAGE



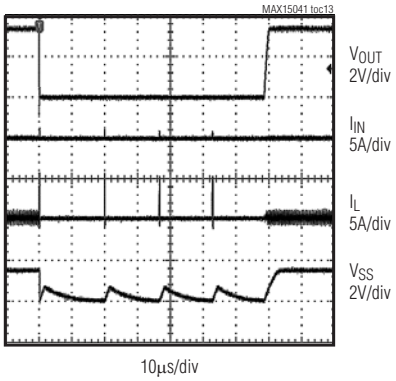
SHUTDOWN CURRENT vs. TEMPERATURE



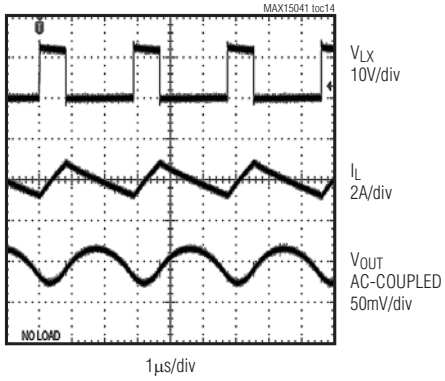
SHUTDOWN WAVEFORMS



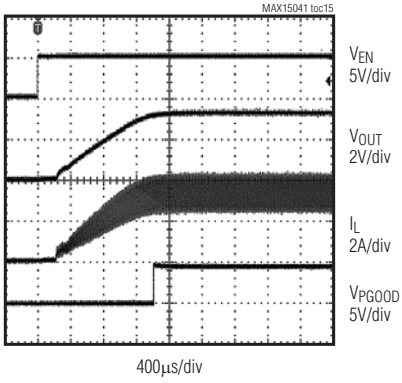
OUTPUT SHORT-CIRCUIT WAVEFORMS



SWITCHING WAVEFORMS



SOFT-START WAVEFORMS

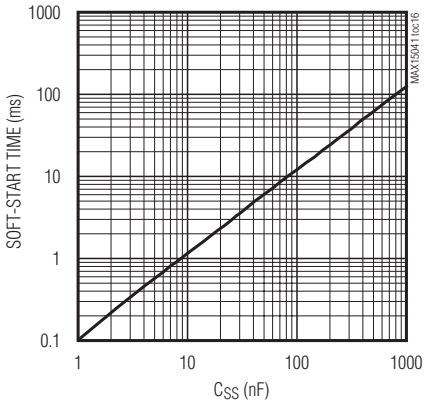


Low-Cost, 3A, 4.5V to 28V Input, 350kHz, PWM Step-Down DC-DC Regulator with Internal Switches

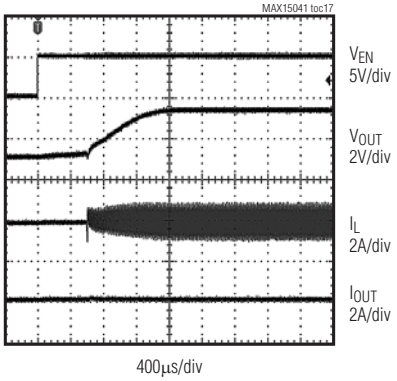
Typical Operating Characteristics (continued)

(V_{IN} = 12V, V_{OUT} = 3.3V, C_{VDD} = 1µF, C_{IN} = 22µF, T_A = +25°C, circuit of Figure 3 (see Table 1 for values), unless otherwise specified.)

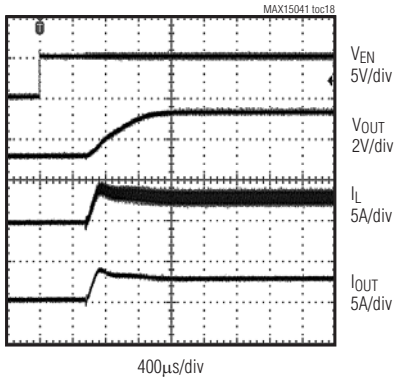
SOFT-START TIME vs. CAPACITANCE



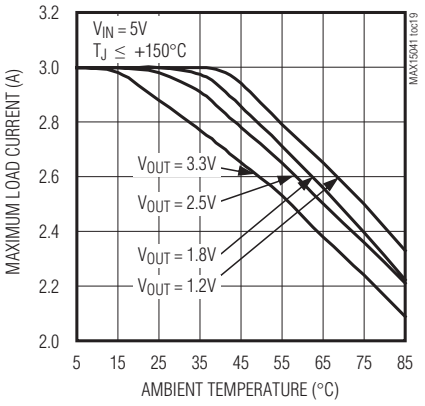
STARTUP INTO PREBIASED OUTPUT



STARTUP INTO PREBIASED OUTPUT



MAXIMUM LOAD CURRENT vs. AMBIENT TEMPERATURE

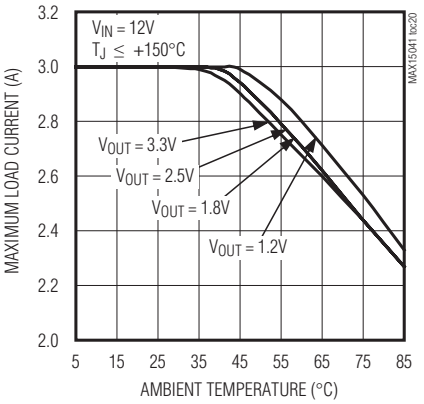


Low-Cost, 3A, 4.5V to 28V Input, 350kHz, PWM Step-Down DC-DC Regulator with Internal Switches

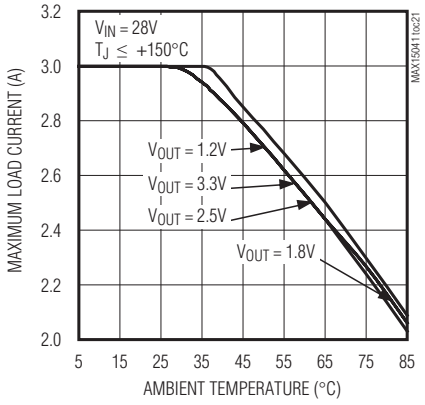
Typical Operating Characteristics (continued)

(V_{IN} = 12V, V_{OUT} = 3.3V, C_{VDD} = 1µF, C_{IN} = 22µF, T_A = +25°C, circuit of Figure 3 (see Table 1 for values), unless otherwise specified.)

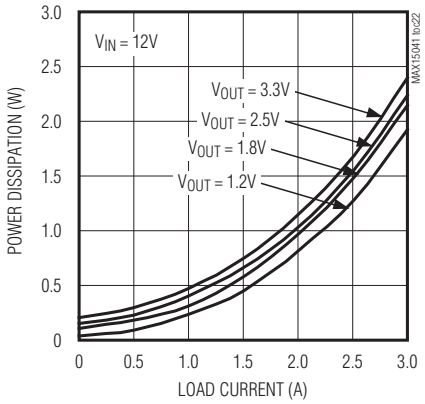
MAXIMUM LOAD CURRENT vs. AMBIENT TEMPERATURE



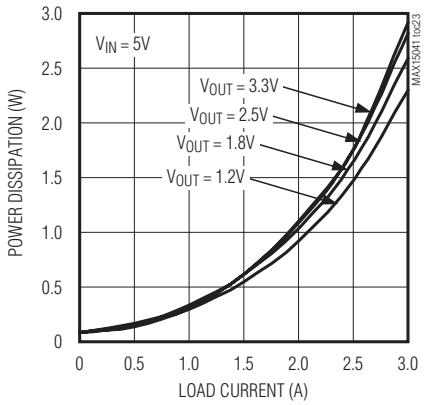
MAXIMUM LOAD CURRENT vs. AMBIENT TEMPERATURE



DEVICE POWER DISSIPATION vs. LOAD CURRENT

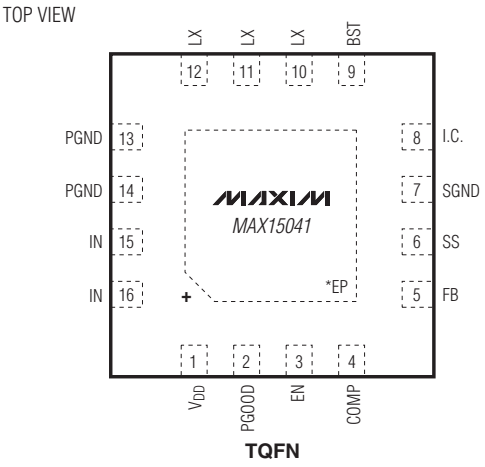


DEVICE POWER DISSIPATION vs. LOAD CURRENT



Low-Cost, 3A, 4.5V to 28V Input, 350kHz, PWM Step-Down DC-DC Regulator with Internal Switches

Pin Configuration



TQFN

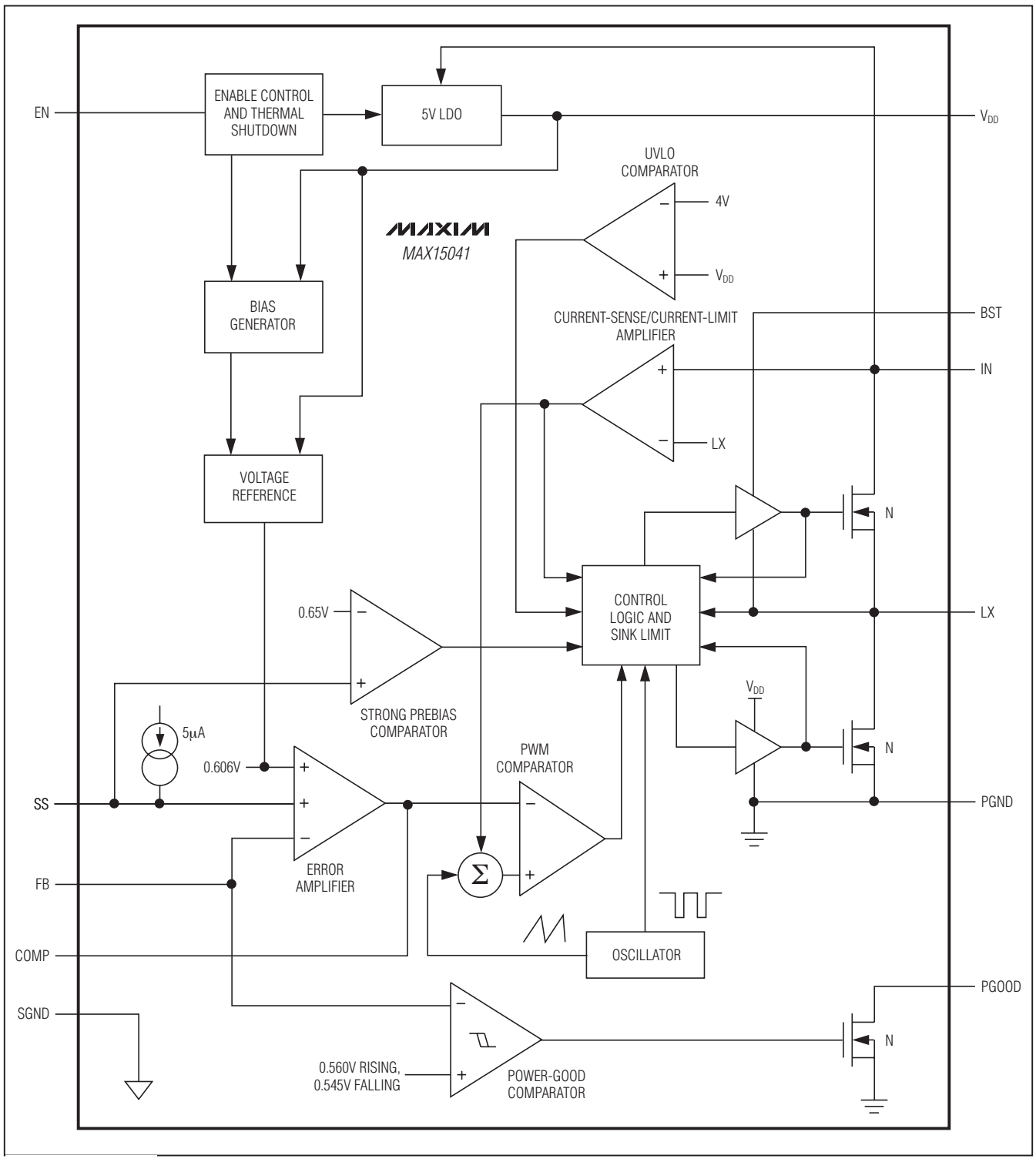
*EXPOSED PAD, CONNECT TO SGND.

Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Internal LDO 5V Output. Supply input for the internal analog core. Bypass with a ceramic capacitor of at least 1µF to SGND. See Figure 3.
2	PGOOD	Power-Good Open-Drain Output. PGOOD goes low if FB is below 545mV.
3	EN	Enable Input. EN is a digital input that turns the regulator on and off. Drive EN high to turn on the regulator. Connect to IN for always-on operations.
4	COMP	Voltage Error-Amplifier Output. Connect the necessary compensation network from COMP to SGND.
5	FB	Feedback Input. Connect FB to the center tap of an external resistor-divider from the output to SGND to set the output voltage from 0.606V to 90% of V_{IN}.
6	SS	Soft-Start Input. Connect a capacitor from SS to SGND to set the soft-start time (see the *Setting the Soft-Start Time* section).
7	SGND	Analog Ground. Connect to PGND plane at one point near the input bypass capacitor return terminal.
8	I.C.	Internally Connected. Connect to SGND.
9	BST	High-Side MOSFET Driver Supply. Bypass BST to LX with a 10nF capacitor. Connect an external diode (see the *Diode Selection* section) from V_{DD} to BST.
10, 11, 12	LX	Inductor Connection. Connect the LX pin to the switched side of the inductor. LX is high impedance when the IC is in shutdown mode, thermal shutdown mode, or V_{DD} is below the UVLO threshold.
13, 14	PGND	Power Ground. Connect to the SGND PCB copper plane at one point near the input bypass capacitor return terminal.
15, 16	IN	Input Power Supply. Input supply range is from 4.5V to 28V. Bypass with a ceramic capacitor of at least 22µF to PGND.
—	EP	Exposed Pad. Connect to SGND externally. Solder the exposed pad to a large contiguous copper plane to maximize thermal performance.

Low-Cost, 3A, 4.5V to 28V Input, 350kHz, PWM Step-Down DC-DC Regulator with Internal Switches

Simplified Block Diagram



Low-Cost, 3A, 4.5V to 28V Input, 350kHz, PWM Step-Down DC-DC Regulator with Internal Switches

Detailed Description

The MAX15041 is a high-efficiency, peak-current-mode, step-down DC-DC converter with integrated high-side (170mΩ, typ) and low-side (105mΩ, typ) power switches. The output voltage is set from 0.606V to 0.9 x V_{IN} by using an adjustable, external resistive divider and can deliver up to 3A load current. The 4.5V to 28V input voltage range makes the device ideal for distributed power systems, notebook computers, and preregulation applications.

The MAX15041 features a PWM, internally fixed 350kHz switching frequency with a 90% maximum duty cycle. PWM current-mode control allows for an all-ceramic capacitor solution. The MAX15041 comes with a high-gain transconductance error amplifier. The current-mode control architecture simplifies compensation design and ensures a cycle-by-cycle current limit and fast reaction to line and load transients. The low R_{DS-ON}, on-chip, MOSFET switches ensure high efficiency at heavy loads and minimize critical inductances, reducing layout sensitivity.

The MAX15041 also features thermal shutdown and overcurrent protection (high-side sourcing and low-side sinking), and an internal 5V, LDO with undervoltage lockout. An externally adjustable voltage soft-start gradually ramps up the output voltage and reduces inrush current. Independent enable control and power-good signals allow for flexible power sequencing. The MAX15041 also provides the ability to start up into a prebiased output, below or above the set point.

Controller Function–PWM Logic

The MAX15041 operates at a constant 350kHz switching frequency. When EN is high, after a brief settling time, PWM operation starts when V_{SS} crosses the FB voltage, at the beginning of soft-start.

The first operation is always a high-side MOSFET turn-on, at the beginning of the clock cycle. The high-side MOSFET is turned off when:

1) COMP voltage crosses the internal current-mode ramp waveform, which is the sum of the compensation ramp and the current-mode ramp derived from the inductor current waveform (current-sense block).
2) The high-side MOSFET current limit is reached.
3) The maximum duty cycle of 90% is reached.

Then, the low-side MOSFET turns on; the low-side MOSFET turns off when the clock period ends.

Starting into a Prebiased Output

The MAX15041 is capable of safely soft-starting into a prebiased output without discharging the output capacitor. Starting up into a prebiased condition, both low-side and high-side MOSFETs remain off to avoid discharging the prebiased output. PWM operation starts only when the SS voltage crosses the FB voltage. The MAX15041 is also capable of soft-starting into an output prebiased above the OUT nominal set point. In this case, forced PWM operation starts when SS voltage reaches 0.65V (typ).

In case of a prebiased output, below or above the OUT nominal set point, if the low-side MOSFET sink current reaches the sink current limit (-3A, typ), the low-side MOSFET turns off before the end of the clock period and the high-side MOSFET turns on until one of the following conditions happens:

1) High-side MOSFET source current hits the reduced high-side MOSFET current limit (0.75A, typ); in this case, the high-side MOSFET is turned off for the remaining clock period.
2) The clock period ends.

Enable Input and Power-Good Output

The MAX15041 features independent device enable control and power-good signals that allow for flexible power sequencing. The enable input (EN) is an input with a 1.95V (typ) threshold that controls the regulator. Assert a voltage exceeding the threshold on EN to enable the regulator, or connect EN to IN for always-on operations. Power-good (PGOOD) is an open-drain output that deasserts (goes high impedance) when V_{FB} is above 560mV (typ), and asserts low if V_{FB} is below 545mV (typ).

When the EN voltage is higher than 1.4V (typ) and lower than 1.95V (typ), most of the internal blocks are disabled, only an internal coarse preregulator, including the EN accurate comparator, is kept on.

Programmable Soft-Start (SS)

The MAX15041 utilizes a soft-start feature to slowly ramp up the regulated output voltage to reduce input inrush current during startup. Connect a capacitor from SS to SGND to set the startup time (see the *Setting the Soft-Start Time* section for capacitor selection details).

Internal LDO (V_{DD})

The MAX15041 has an internal 5.1V (typ) LDO. V_{DD} is externally compensated with a minimum 1µF, low-ESR ceramic capacitor. The V_{DD} voltage is used to supply the low-side MOSFET driver, and to supply the internal control logic. When the input supply (IN) is below 4.5V, V_{DD} is 50mV (typ) lower than IN. The V_{DD} output current limit is 80mA (typ) and an UVLO circuit inhibits switching when V_{DD} falls below 3.85V (typ).

Error Amplifier

A high-gain error amplifier provides accuracy for the voltage feedback loop regulation. Connect the necessary compensation network between COMP and SGND (see the *Compensation Design Guidelines* section). The error-amplifier transconductance is 1.6mS (typ). COMP clamp low is set to 0.68V (typ), just below the PWM ramp compensation valley, helping COMP to rapidly return to correct set point during load and line transients.

PWM Comparator

The PWM comparator compares COMP voltage to the current-derived ramp waveform (LX current to COMP voltage transconductance value is 9A/V, typ.). To avoid instability due to subharmonic oscillations when the duty cycle is around 50% or higher, a compensation ramp is added to the current-derived ramp waveform. The compensation ramp slope (0.45V x 350kHz) is equivalent to half of the inductor current down slope in the worst case (load 3A, current ripple 30% and maximum duty cycle operation of 90%). Compensation ramp valley is set at 0.83V (typ).

Overcurrent Protection and Hiccup Mode

When the converter output is shorted or the device is overloaded, the high-side MOSFET current-limit event (6A, typ) turns off the high-side MOSFET and turns on the low-side MOSFET. In addition, it discharges the SS capacitor, C_{SS} for a fixed period of time (ΔT_0 = 70ns, typ). If the overcurrent condition persists, SS is pulled below 0.606V and a hiccup event is triggered.

During a hiccup event, high-side and low-side MOSFETs are kept off, and COMP is pulled low for a period equal to 16 times the nominal soft-start time (blanking time). This is obtained by charging SS from 0 to 0.606V with a 5µA (typ) current, and then slowly discharging it back to 0V with a 333nA (typ) current. After the blanking time has elapsed, the device attempts to restart. If the overcurrent fault has cleared, the device resumes normal operation, otherwise a new hiccup event is triggered (see the Output Short-Circuit Waveforms in the *Typical Operating Characteristics*).

Thermal-Shutdown Protection

The MAX15041 contains an internal thermal sensor that limits the total power dissipation in the device and protects it in the event of an extended thermal fault condition. When the die temperature exceeds +155°C (typ), the thermal sensor shuts down the device, turning off the DC-DC converter and the LDO regulator to allow the die to cool. After the die temperature falls by 20°C (typ), the device restarts, using the soft-start sequence.

Applications Information

Setting the Output Voltage

Connect a resistive divider (R_1 and R_2, see Figures 1 and 3) from OUT to FB to SGND to set the DC-DC converter output voltage. Choose R_1 and R_2 so that the DC errors due to the FB input bias current do not affect the output-voltage precision. With lower value resistors, the DC error is reduced, but the amount of power consumed in the resistive divider increases. A typical tradeoff value for R_2 is 10kΩ, but values between 5kΩ and 50kΩ are acceptable. Once R_2 is chosen, calculate R_1 using:

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where the feedback threshold voltage V_{FB} = 0.606V (typ).

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Inductor Selection

A larger inductor value results in reduced inductor ripple current, leading to a reduced output ripple voltage. However, a larger inductor value results in either a larger physical size or a higher series resistance (DCR) and a lower saturation current rating. Typically, inductor value is chosen to have current ripple equal to 30% of load current. Choose the inductor with the following formula:

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where f_{SW} is the internally fixed 350kHz switching frequency, and ΔI_L is the estimated inductor ripple current (typically set to 0.3 x I_{LOAD}). In addition, the peak inductor current, I_{L_PK}, must always be below both the minimum high-side MOSFET current-limit value, I_{HSCL_MIN} (5A, typ), and the inductor saturation current rating, I_{L_SAT}. Ensure that the following relationship is satisfied:

$$I_{L\_PK} = I_{LOAD} + \frac{1}{2} \times \Delta I_L < \min(I_{HSCL\_MIN}, I_{L\_SAT})$$

Diode Selection

The MAX15041 requires an external bootstrap steering diode. Connect the diode between V_{DD} and BST. The diode should have a reverse voltage rating, higher than the converter input voltage and a 200mA minimum current rating. Typically, a fast switching or Schottky diode is used in this application, but a simple low-cost diode (1N4007) suffices.

Input Capacitor Selection

For a step-down converter, input capacitor C_{IN} helps to keep the DC input voltage steady, in spite of discontinuous input AC current. Low-ESR capacitors are preferred to minimize the voltage ripple due to ESR.

Size C_{IN} using the following formula:

$$C_{IN} = \frac{I_{LOAD}}{f_{SW} \times \Delta V_{IN\_RIPPLE}} \times \frac{V_{OUT}}{V_{IN}}$$

Output-Capacitor Selection

Low-ESR capacitors are recommended to minimize the voltage ripple due to ESR. Total output-voltage peak-to-peak ripple is estimated by the following formula:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR\_COUT} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right)$$

For ceramic capacitors, ESR contribution is negligible:

$$R_{ESR\_COUT} << \frac{1}{8 \times f_{SW} \times C_{OUT}}$$

For tantalum or electrolytic capacitors, ESR contribution is dominant:

$$R_{ESR\_COUT} >> \frac{1}{8 \times f_{SW} \times C_{OUT}}$$

Compensation Design Guidelines

The MAX15041 uses a fixed-frequency, peak-current-mode control scheme to provide easy compensation and fast transient response. The inductor peak current is monitored on a cycle-by-cycle basis and compared to the COMP voltage (output of the voltage error amplifier). The regulator's duty-cycle is modulated based on the inductor's peak current value. This cycle-by-cycle control of the inductor current emulates a controlled current source. As a result, the inductor's pole frequency is shifted beyond the gain-bandwidth of the regulator.

System stability is provided with the addition of a simple series capacitor-resistor from COMP to SGND. This pole-zero combination serves to tailor the desired response of the closed-loop system.

The basic regulator loop consists of a power modulator (comprising the regulator's pulse-width modulator, compensation ramp, control circuitry, MOSFETs, and inductor), the capacitive output filter and load, an output feedback divider, and a voltage-loop error amplifier with its associated compensation circuitry. See Figure 1 for a graphical representation.

The average current through the inductor is expressed as:

$$I_L = G_{MOD} \times V_{COMP}$$

where I_L is the average inductor current and G_{MOD} is the power modulator's transconductance. For a buck converter:

$$V_{OUT} = R_{LOAD} \times I_L$$

where R_{LOAD} is the equivalent load resistor value. Combining the two previous equations, the power modulator's transfer function in terms of V_{OUT} with respect to V_{COMP} is:

$$\frac{V_{OUT}}{V_{COMP}} = \frac{R_{LOAD} \times I_L}{\left(\frac{I_L}{G_{MOD}}\right)} = R_{LOAD} \times G_{MOD}$$

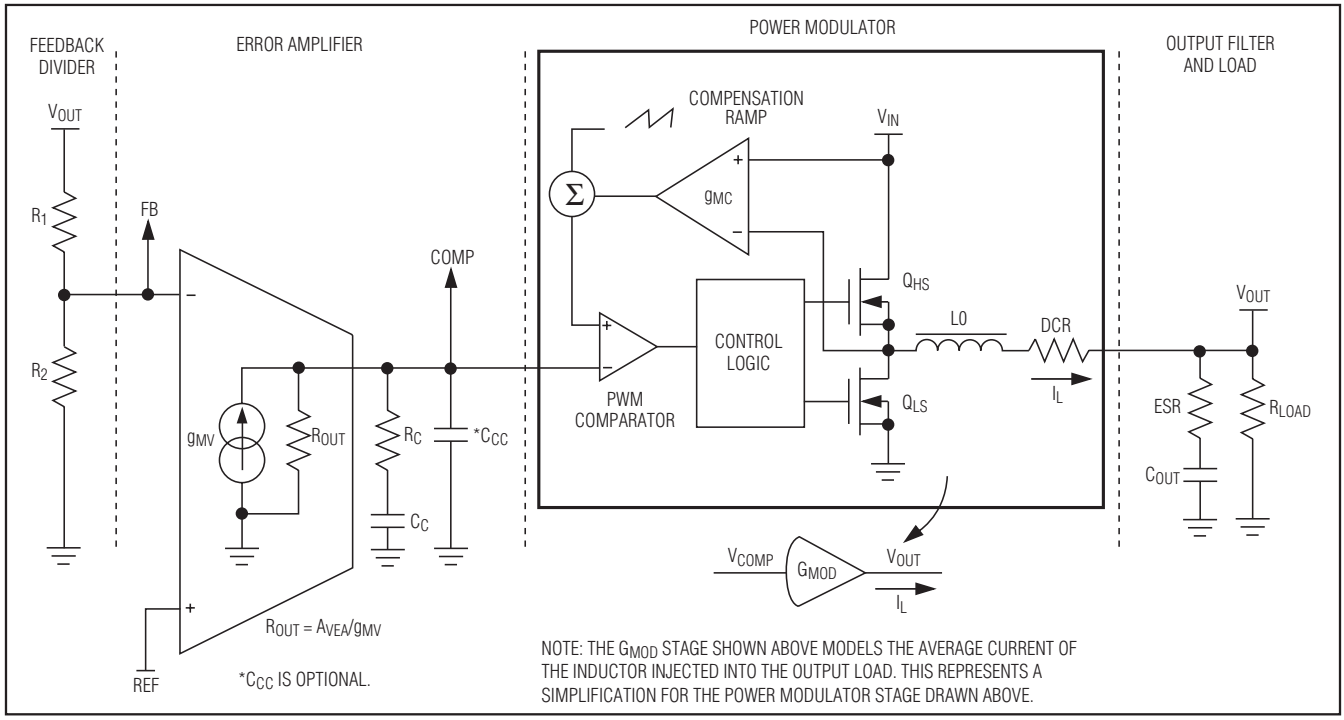

Figure 1. Peak Current-Mode Regulator Transfer Model

Having defined the power modulator's transfer function gain, the total system loop gain can be written as follows (see Figure 1):

$$\alpha = \frac{R_{OUT} \times (sC_CR_C + 1)}{\left[s(C_C + C_{CC})(R_C + R_{OUT}) + 1\right] \times \left[s(C_C \parallel C_{CC})(R_C \parallel R_{OUT}) + 1\right]}$$

$$\beta = G_{MOD} \times R_{LOAD} \times \frac{(sC_{OUT}ESR + 1)}{\left[sC_{OUT}(ESR + R_{LOAD}) + 1\right]}$$

$$Gain = \frac{R_2}{R_1 + R_2} \times \frac{A_{VEA}}{R_{OUT}} \times \alpha \times \beta$$

where R_{OUT} is the quotient of the error amplifier's DC gain, A_{VEA}, divided by the error amplifier's transconductance, g_{MV}; R_{OUT} is much larger than R_C and C_C is much larger than C_{CC}.

Rewriting:

$$Gain = \frac{V_{FB}}{V_{OUT}} A_{VEA} \times \frac{(sC_CR_C + 1)}{\left[sC_C\left(\frac{A_{VEA}}{g_{MV}}\right) + 1\right] \times (sC_{CC}R_C + 1)} \times G_{MOD}R_{LOAD} \times \frac{(sC_{OUT}ESR + 1)}{\left[sC_{OUT}(ESR + R_{LOAD}) + 1\right]}$$

The dominate poles and zeros of the transfer loop gain is shown below:

$$f_{P1} = \frac{g_{MV}}{2\pi \times 10^{A_{VEA}[dB]/20} \times C_C} \quad f_{P2} = \frac{1}{2\pi \times C_{OUT}(ESR + R_{LOAD})}$$

$$f_{P3} = \frac{1}{2\pi \times C_{CC}R_C} \quad f_{Z1} = \frac{1}{2\pi \times C_CR_C}$$

$$f_{Z2} = \frac{1}{2\pi \times C_{OUT}ESR}$$

The order of pole-zero occurrence is:

$$f_{P1} < f_{P2} < f_{Z1} < f_{Z2} \le f_{P3}$$

Note under heavy load, f_{P2}, may approach f_{Z1}.

A graphical representation of the asymptotic system closed-loop response, including the dominant pole and zero locations is shown in Figure 2.

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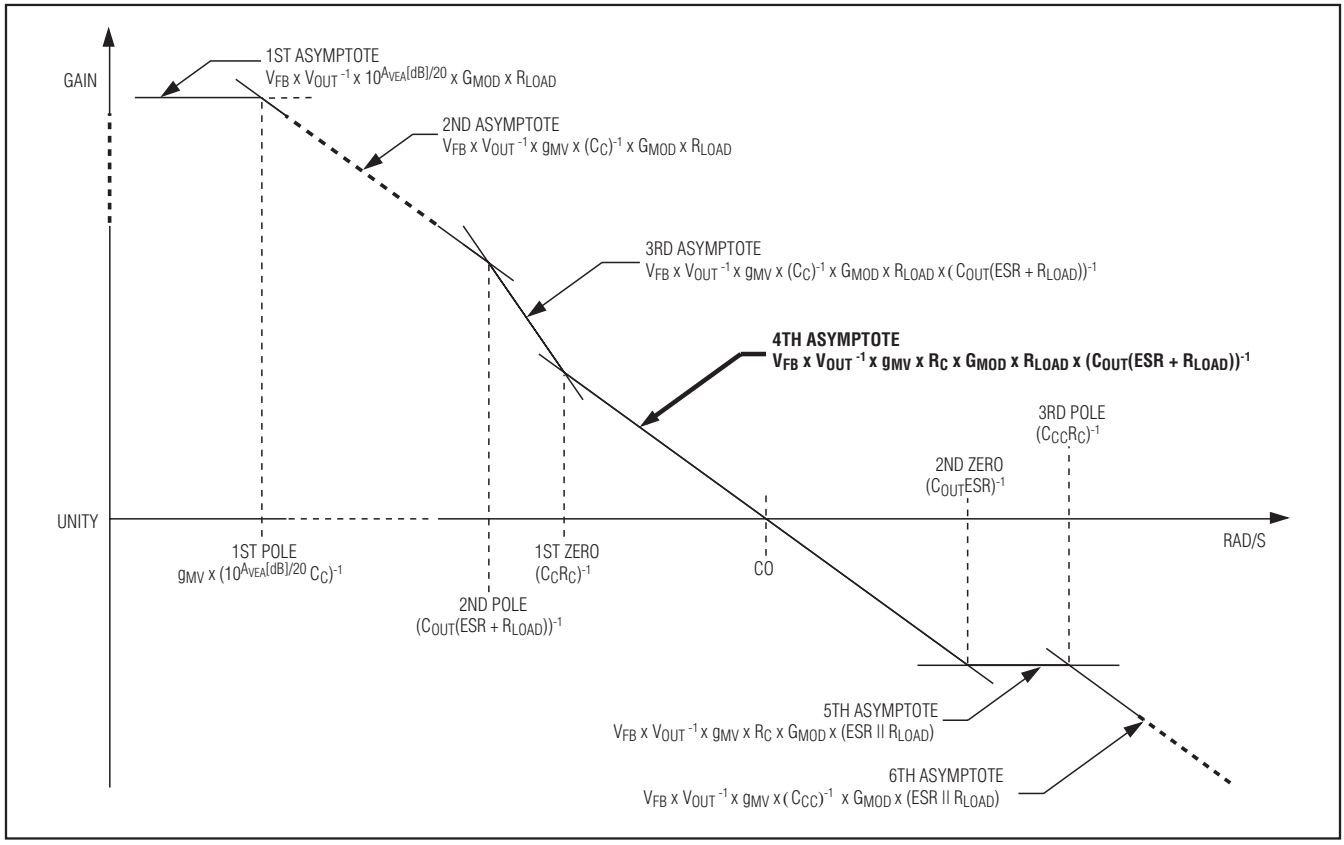

Figure 2. Asymptotic Loop Response of Peak Current-Mode Regulator

If C_{OUT} is large, or exhibits a lossy equivalent series resistance (large ESR), the circuit's second zero may come into play around the crossover frequency ($f_{CO} = \omega_{CO}/2\pi$). In this case, a third pole may be induced by a second (optional) small compensation capacitor (C_{CC}), connected from COMP to SGND.

The loop response's fourth asymptote (in bold, Figure 2) is the one of interest in establishing the desired crossover frequency (and determining the compensation component values). A lower crossover frequency provides for stable closed-loop operation at the expense of a slower load and line transient response. Increasing the crossover frequency improves the transient response at the (potential) cost of system instability. A standard rule of thumb sets the crossover frequency ≤ 1/10 of the switching frequency (for the MAX15041, this is approximately 35kHz for the 350kHz fixed switching frequency).

First, select the passive and active power components that meet the application's requirements. Then, choose the small-signal compensation components to achieve the desired closed-loop frequency response and phase margin as outlined in the *Closing the Loop: Designing the Compensation Circuitry* section.

Closing the Loop: Designing the Compensation Circuitry

1) Select the desired crossover frequency. Choose f_{CO} equal to 1/10th of f_{SW}, or $f_{CO} \approx 35kHz$.

2) Select R_C using the transfer-loop's fourth asymptote gain (assuming $f_{CO} > f_{P1}$, f_{P2}, and f_{Z1} and setting the overall loop gain to unity) as follows:

$$1 = \frac{V_{FB}}{V_{OUT}} \times g_{MV} \times R_C \times G_{MOD} \times R_{LOAD} \times \frac{1}{2\pi \times f_{CO} \times C_{OUT} \times (ESR + R_{LOAD})}$$

therefore:

$$R_C = \frac{V_{OUT}}{V_{FB}} \times \frac{2\pi \times f_{CO} \times C_{OUT} \times (ESR + R_{LOAD})}{g_{MV} \times G_{MOD} \times R_{LOAD}}$$

For R_{LOAD} much greater than ESR, the equation can be further simplified as follows:

$$R_C = \frac{V_{OUT}}{V_{FB}} \times \frac{2\pi \times f_{CO} \times C_{OUT}}{g_{MV} \times G_{MOD}}$$

where V_{FB} is equal to 0.606V.

3) Select C_C. C_C is determined by selecting the desired first system zero, f_{Z1}, based on the desired phase margin. Typically, setting f_{Z1} below 1/5th of f_{CO} provides sufficient phase margin.

$$f_{Z1} = \frac{1}{2\pi \times C_C R_C} \le \frac{f_{CO}}{5}$$

therefore:

$$C_C \ge \frac{5}{2\pi \times f_{CO} \times R_C}$$

4) If the ESR output zero is located at less than one-half the switching frequency use the (optional) secondary compensation capacitor, C_{CC}, to cancel it, as follows:

$$\frac{1}{2\pi \times C_{CC} R_C} = f_{P3} = f_{Z2} = \frac{1}{2\pi \times C_{OUT} ESR}$$

therefore:

$$C_{CC} = \frac{C_{OUT} \times ESR}{R_C}$$

If the ESR zero exceeds 1/2 the switching frequency, use the following equation:

$$f_{P3} = \frac{1}{2\pi \times C_{CC} R_C} = \frac{f_{SW}}{2}$$

therefore:

$$C_{CC} = \frac{2}{2\pi \times f_{SW} \times R_C}$$

The downside of C_{CC} is that it detracts from the overall system phase margin. Care should be taken to guarantee this third-pole placement is well beyond the desired crossover frequency, minimizing its interaction with the system loop response at crossover. If C_{CC} is smaller than 10pF, it can be neglected in these calculations.

Setting the Soft-Start Time

The soft-start feature ramps up the output voltage slowly, reducing input inrush current during startup. Size the C_{SS} capacitor to achieve the desired soft-start time t_{SS} using:

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{FB}}$$

I_{SS}, the soft-start current, is 5µA (typ) and V_{FB}, the output feedback voltage threshold, is 0.606V (typ). When using large C_{OUT} capacitance values, the high-side current limit may trigger during the soft-start period. To ensure the correct soft-start time, t_{SS}, choose C_{SS} large enough to satisfy:

$$C_{SS} >> C_{OUT} \times \frac{V_{OUT} \times I_{SS}}{(I_{HSCL\_MIN} - I_{OUT}) \times V_{FB}}$$

I_{HSCL_MIN} is the minimum high-side switch, current-limit value.

Power Dissipation

The MAX15041 is available in a thermally enhanced TQFN package and can dissipate up to 1.666W at T_A = +70°C. The exposed pad should be connected to SGND externally, preferably soldered to a large ground plane to maximize thermal performance. When the die temperature exceeds +155°C, The thermal-shutdown protection is activated (see the *Thermal-Shutdown Protection* section).

Layout Procedure

Careful PCB layout is critical to achieve clean and stable operation. It is highly recommended to duplicate the MAX15041 evaluation kit layout for optimum performance. If deviation is necessary, follow these guidelines for good PCB layout:

1) Connect input and output capacitors to the power ground plane; connect all other capacitors to the signal ground plane.

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2) Place capacitors on V_{DD}, IN, and SS as close as possible to the IC and the corresponding pin using direct traces. Keep the power ground plane (connected to PGND) and signal ground plane (connected to SGND) separate. PGND and SGND connect at only one common point near the input bypass capacitor return terminal.
3) Keep the high-current paths as short and wide as possible. Keep the path of switching current short and minimize the loop area formed by LX, the output capacitors, and the input capacitors.
4) Connect IN, LX, and PGND separately to a large copper area to help cool the IC to further improve efficiency.
5) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close as possible to the IC.
6) Route high-speed switching nodes (such as LX and BST) away from sensitive analog areas (such as FB and COMP).

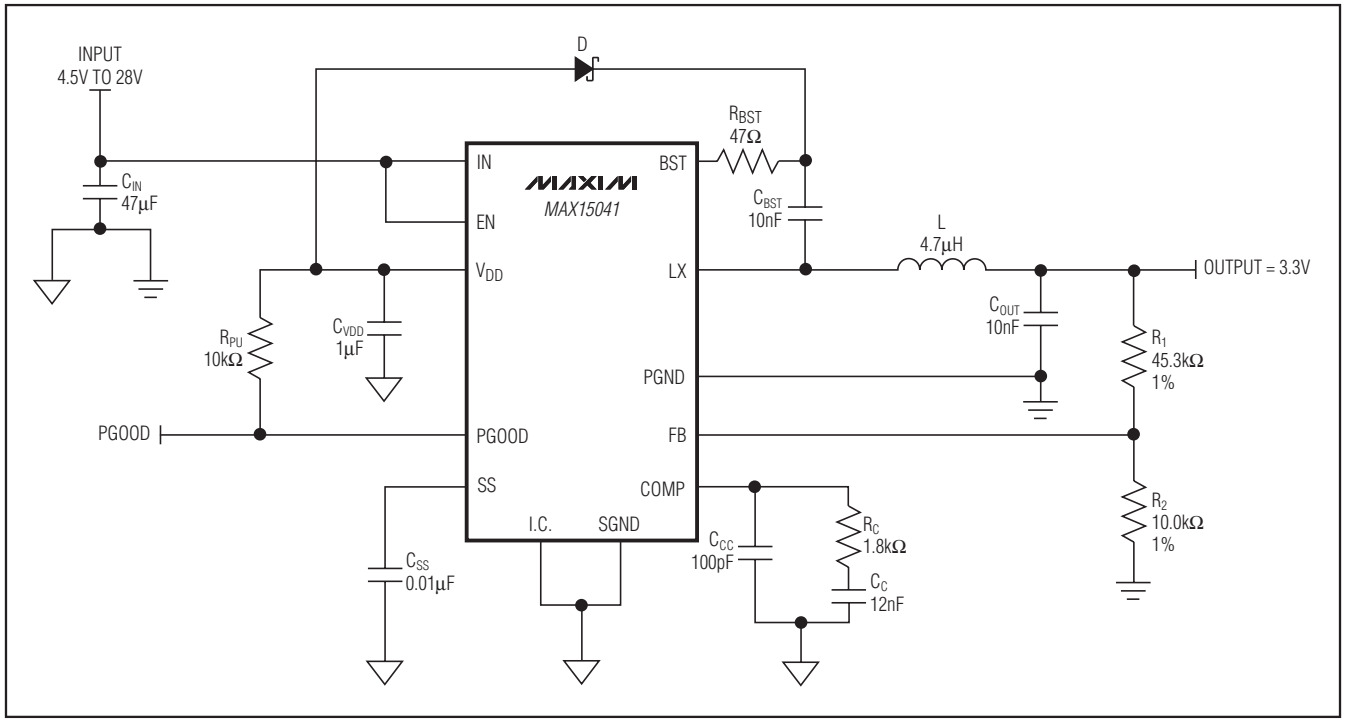

Figure 3. Typical Operating Circuit (4.5V to 28V Input Buck Converter)

Table 1. Typical Component Values for Common Output-Voltage Settings

V_{OUT} (V)	L (µH)	C_C (nF)	R_C (kΩ)	R_1 and R_2
5.0	4.7	8	2.70	Select R_2 so that: $5k\Omega \le R_2 \le 50k\Omega$ Calculate R_1 using the equation in the *Setting the Output Voltage* section.
3.3	4.7	12	1.80	
2.5	3.3	22	1.50	
1.8	2.2	33	1.00	
1.2	2.2	47	0.68	

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
16 TQFN-EP	T1633+4	**21-0136**

Low-Cost, 3A, 4.5V to 28V Input, 350kHz, PWM Step-Down DC-DC Regulator with Internal Switches

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/09	Initial release	—
1	3/10	Revised *General Description*, *Absolute Maximum Ratings*, *Applications Information*, Figures 2 and 3.	1, 2, 3, 7, 10-13, 15, 16