Low Frequency Timing-Safe™ Peak EMI reduction IC

General Features

- Low Frequency Clock Distribution with Timing-Safe™ and Peak EMI Reduction
- Input frequency range: 4MHz - 20MHz
- Zero input - output propagation delay
- Low-skew outputs
  - Output-output skew less than 250pS
  - Device-device skew less than 700pS
- Less than 200pS Cycle-to-cycle jitter
- 3.3V Operation
- Commercial temperature range
- Available in 8pin TSSOP(4.4MM-Body)
- First True Drop-in solution

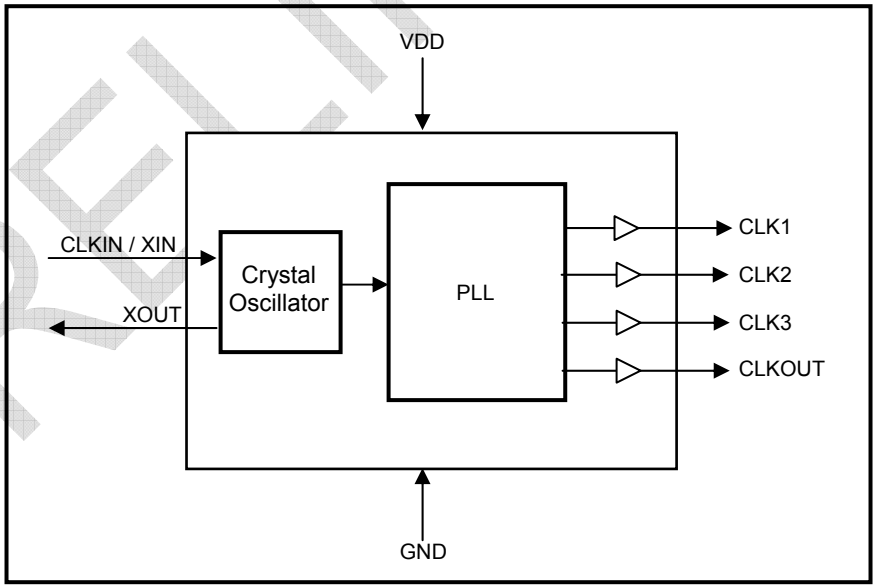
Product Description

PCS3P622S04J is a versatile, 3.3V Zero-delay buffer designed to distribute low frequency Timing-Safe™ clocks with Peak EMI Reduction. PCS3P622S04J accepts one reference input and drives out four low-skew clocks. PCS3P622S04J has an on-chip PLL that locks to an input clock on the XIN/CLKIN pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad, internal to the device. PCS3P622S04J has a crystal oscillator interface. An inexpensive crystal will provide the clock source for distribution. It is available in 8 pin TSSOP.

All outputs have less than 200pS of Cycle-to-cycle jitter. The input and output propagation delay is guaranteed to be less than 350pS, and the output-to-output skew is guaranteed to be less than 250pS.

Refer "Spread Spectrum Control and Input-Output Skew Table" for values of deviation and Input-Output Skew

Block Diagram



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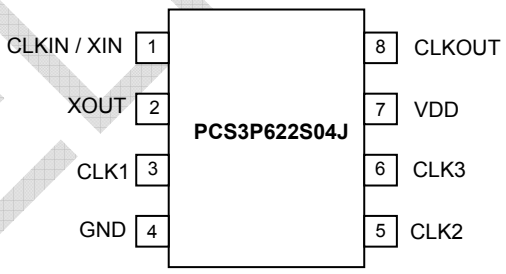
Spread Spectrum Frequency Generation

The clocks in digital systems are typically square waves with a 50% duty cycle and as frequencies increase the edge rates also get faster. Analysis shows that a square wave is composed of fundamental frequency and harmonics. The fundamental frequency and harmonics generate the energy peaks that become the source of EMI. Regulatory agencies test electronic equipment by measuring the amount of peak energy radiated from the equipment. In fact, the peak level allowed decreases as the frequency increases. The standard methods of reducing EMI are to use shielding, filtering, multi-layer PCBs etc. These methods are expensive. Spread spectrum clocking reduces the peak energy by reducing the Q factor of the clock. This is done by slowly modulating the clock frequency. PCS3P622S04J uses the center modulation spread spectrum technique in which the modulated output frequency varies above and below the reference frequency with a specified modulation rate. With center modulation, the average frequency is the same as the unmodulated frequency and there is no performance degradation

Timing-Safe™ technology

Timing-Safe™ technology is the ability to modulate a clock source with Spread Spectrum technology and maintain synchronization with any associated data path.

Pin Configuration



rev 0.3

Pin Description

Pin #	Pin Name	Description
1	XIN/CLKIN	Crystal connection or external reference frequency input. This pin has dual functions. It can be connected either to an external crystal or an external reference clock.
2	XOUT	Crystal connection. If using an external reference, this pin must be left unconnected.
3	CLK1	Buffered clock output
4	GND	Ground
5	CLK2	Buffered clock output
6	CLK3	Buffered clock output
7	V_{DD}	3.3V supply
8	CLKOUT	Buffered clock output, internal feedback on this pin

Notes: 1. Weak pull-down on all outputs
2. Weak pull-up on the Inputs
3. Buffered clock outputs are Timing-Safe™

Spread Spectrum Control and Input-Output Skew Table

Device	Input Frequency	Deviation	Input-Output Skew($\pm T_{SKEW}$)
PCS3P622S04J	16MHz	±0.35%	0.375

Note: T_{SKEW} is measured in units of the Clock Period

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VDD, V_{IN}	Voltage on any pin with respect to Ground	-0.5 to +4.6	V
T_{STG}	Storage temperature	-65 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Operating Conditions for PCS3P622S04J

Parameter	Description	Min	Max	Unit
VDD	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	0	+70	°C
C_L	Load Capacitance		30	pF
C_{IN}	Input Capacitance		7	pF

Electrical Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input LOW Voltage[1]				0.8	V
V_{IH}	Input HIGH Voltage[1]		2.0			V
I_{IL}	Input LOW Current	V_{IN} = 0V			50	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}			100	µA
V_{OL}	Output LOW Voltage[2]	I_{OL} = 8mA			0.4	V
V_{OH}	Output HIGH Voltage[2]	I_{OH} = -8mA	2.4			V
I_{DD}	Supply Current	Unloaded outputs		14		mA
Z_o	Output Impedance			23		Ω

Note: 1. REF input has a threshold voltage of $V_{DD}/2$
2. Parameter is guaranteed by design and characterization. Not 100% tested in production

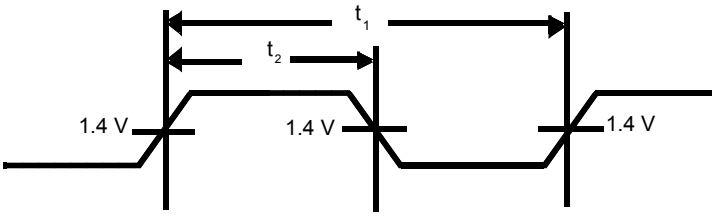
Switching Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
$1/t_1$	Output Frequency	30pF load	4		20	MHz
	Duty Cycle [2] = $(t_2 / t_1) * 100$	Measured at $V_{DD}/2$	40	50	60	%
t_3	Output Rise Time [1,2]	Measured between 0.8V and 2.0V			2.5	nS
t_4	Output Fall Time [1,2]	Measured between 2.0V and 0.8V			2.5	nS
t_5	Output-to-output skew [2]	All outputs equally loaded			250	pS
t_6	Delay, REF Rising Edge to CLKOUT Rising Edge [2]	Measured at V_{DD} /2			±350	pS
t_7	Device-to-Device Skew [2]	Measured at $V_{DD}/2$ on the CLKOUT pins of the device			700	pS
t_J	Cycle-to-cycle jitter [2]	Loaded outputs			200	pS
t_{LOCK}	PLL Lock Time [2]	Stable power supply, valid clock presented on REF pin			1.0	mS

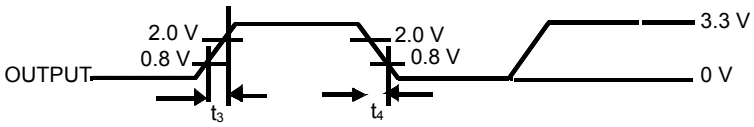
Note: 1. All parameters specified with loaded outputs.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production

Switching Waveforms

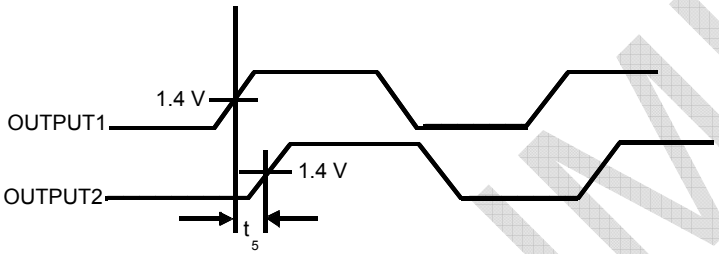
Duty Cycle Timing



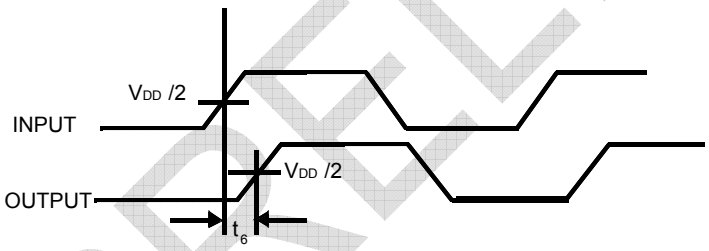
All Outputs Rise/Fall Time



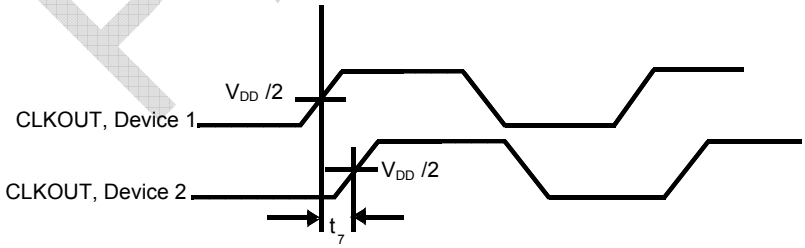
Output - Output Skew



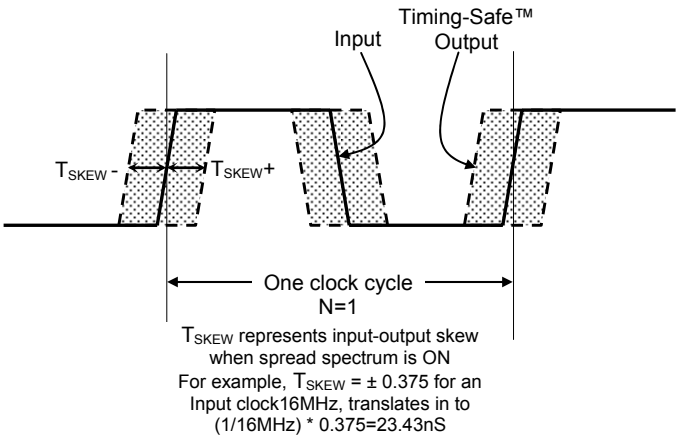
Input - Output Propagation Delay



Device - Device Skew

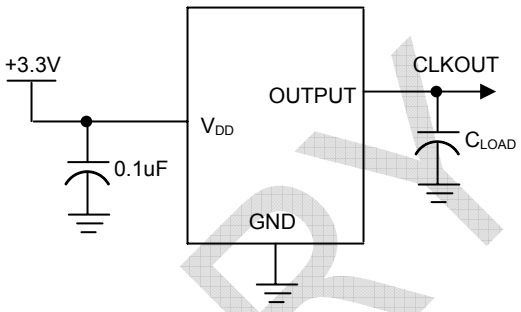


Input-Output Skew

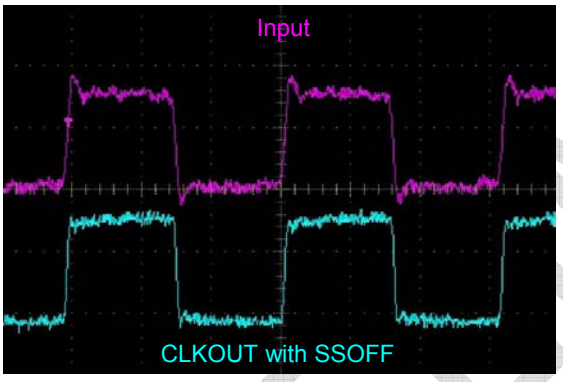


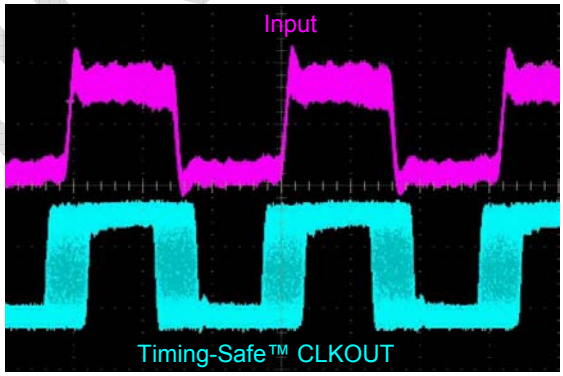
T_{SKEW} represents input-output skew when spread spectrum is ON
For example, T_{SKEW} = ± 0.375 for an Input clock16MHz, translates in to (1/16MHz) * 0.375=23.43nS

Test Circuit



A Typical example of Timing-Safe™ waveform





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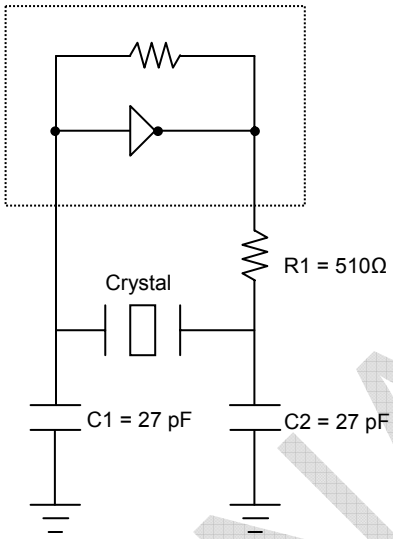
Typical Crystal Oscillator Circuit



Typical Crystal Specifications

Fundamental AT cut parallel resonant crystal	
Nominal frequency	16 MHz
Frequency tolerance	± 50 ppm or better at 25°C
Operating temperature range	-25°C to +85°C
Storage temperature	-40°C to +85°C
Load capacitance	18pF
Shunt capacitance	7pF maximum
ESR	25 Ω

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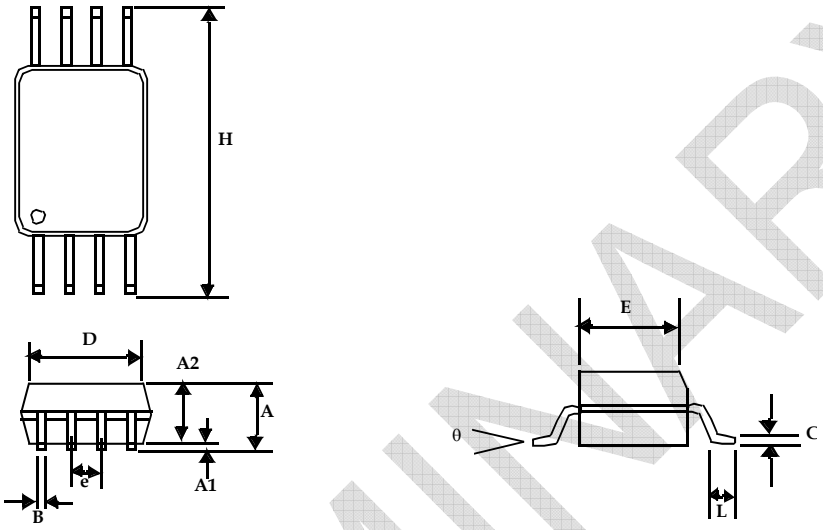
Package Information

8-lead Thin Shrunk Small Outline Package (4.40-MM Body)



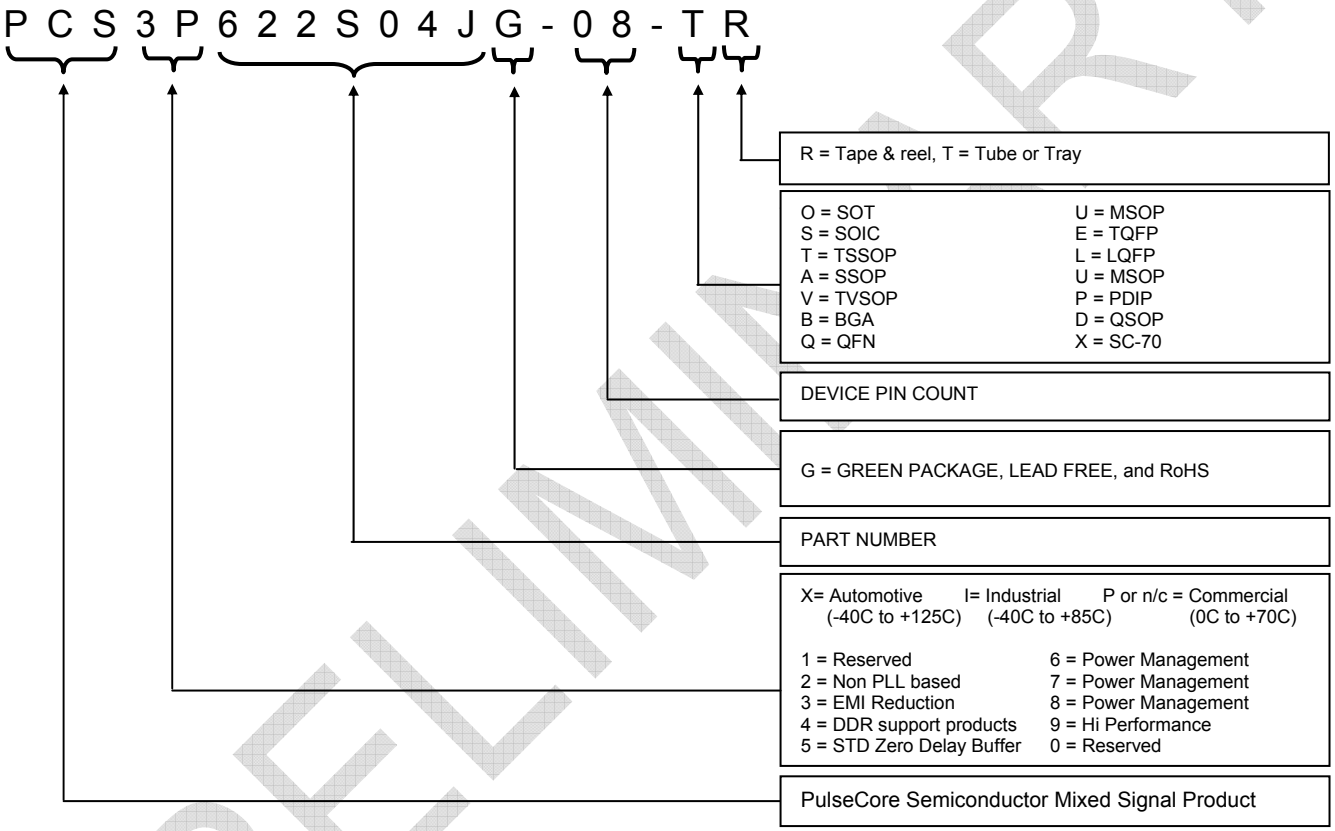
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.10
A1	0.002	0.006	0.05	0.15
A2	0.033	0.037	0.85	0.95
B	0.008	0.012	0.19	0.30
c	0.004	0.008	0.09	0.20
D	0.114	0.122	2.90	3.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.028	0.50	0.70
θ	0°	8°	0°	8°

rev 0.3

Ordering Codes

Ordering Code	Marking	Package Type	Temperature
PCS3P622S04JG-08-TT	3P622S04JG	8-pin 4.4-mm TSSOP - TUBE, Green	Commercial
PCS3P622S04JG-08-TR	3P622S04JG	8-pin 4.4-mm TSSOP - TAPE & REEL, Green	Commercial

Device Ordering Information



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Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003
Timing-Safe™ US patent pending