TWO-CELL LITHIUM-ION BATTERY PROTECTION IC

FEATURES

- Ultra-Low Quiescent Current at 10μA (V_{CC}=7V, V_C=3.5V).
- Ultra-Low Power-Down Current at 0.2μA (V_{CC} =3.8V, V_C=1.9V).
- Wide Supply Range: 2 to 18V.
- Precision Overcharge Protection Voltage
  4.35V ± 30mV for the SS6802A
  4.30V ± 30mV for the SS6802B
  4.25V ± 30mV for the SS6802C
- Built-in Delay Circuits for Overcharge, Over-discharge and Overcurrent Protection.
- Overcharge and Overdischarge Delay Time can be Extended by External Capacitors.
- Built-in Cell-balancing Bleeding Network under Overcharge Condition.

APPLICATIONS

- Protection IC for Two-Cell Lithium-Ion Battery Pack.

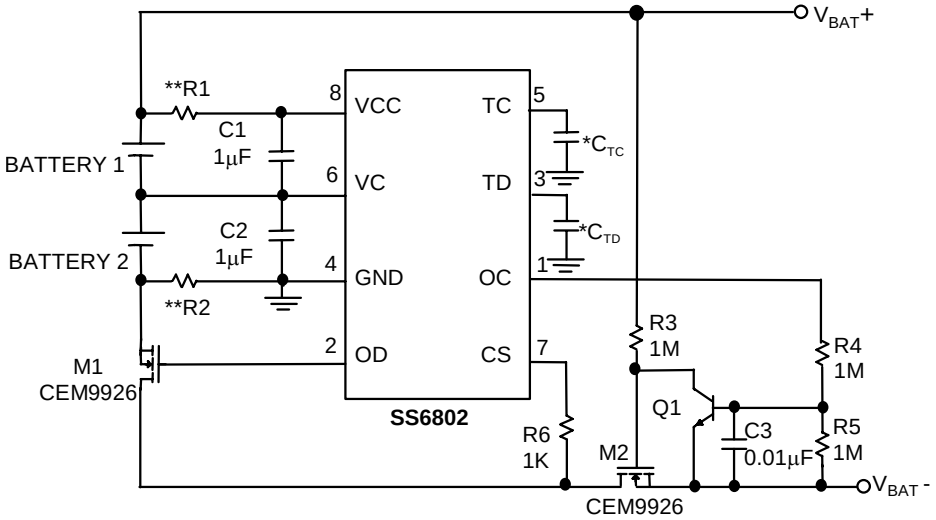
DESCRIPTION

The SS6802 battery protection IC is designed to protect lithium-ion batteries from damage due to overcharging, overdischarging, and overcurrent for two series cells in portable phones and laptop computers. It can be a part of the low-cost charge control system within a two-cell lithium-ion battery pack.

Safe and full utilization charging is ensured by the accurate ±30mV overcharge detection. Three different specification values for overcharge protection voltage are provided for various protection requirements. The very low standby current drains little current from the cells while in storage.

Pb-free; RoHS-compliant

TYPICAL APPLICATION CIRCUIT



*C_{TC} & C_{TD} are optional for delay time adjustment.
**R1 & R2: Refer application informations.

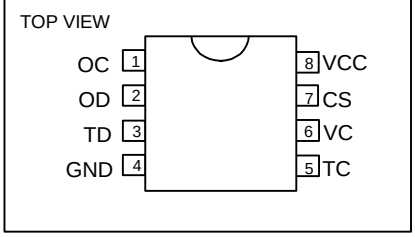
Protection Circuit for Two-Cell Lithium-Ion Battery Pack

ORDERING INFORMATION

SS6802XXXXX

- PACKING TYPE
  TR: TAPE & REEL
  TB: TUBE
- PACKAGE TYPE
  S: SOP-8
- G: LEAD FREE COMMERCIAL
- OVERCHARGE PROTECTION VOLTAGE
  A: 4.35V
  B: 4.30V
  C: 4.25V

PIN CONFIGURATION



Example: SS6802AGSTR
→ 4.35V version, in SO-8 Lead Free Package & Tape & Reel Packing Type

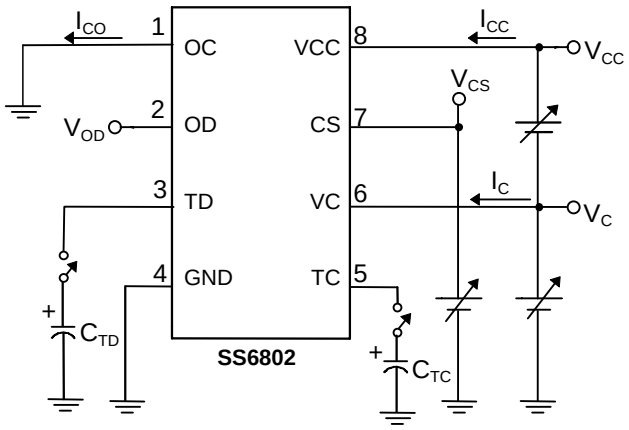
ABSOLUTE MAXIMUM RATINGS

Supply Voltage		18V
DC Voltage Applied on VC, CS, OC, OD Pins		18V
DC Voltage Applied on TC, TD Pins		5V
Operating Temperature Range		-40°C~85°C
Storage Temperature Range		- 65°C~150°C
Junction Temperature		125°C
Lead Temperature (Soldering 10s)		260°C
Thermal Resistance Junction to Case	SOP-8	40°C/W
Thermal Resistance Junction to Ambient	SOP-8	160°C/W

(Assume no ambient airflow, no heatsink)

Absolute Maximum Rating are those value beyond which the life of a device may be impaired.

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Current in Normal Mode	V_{CC}=7V, V_C=3.5V	I_{CC}		10	15	μA
Supply Current in Power-Down Mode	V_{CC}=4.8V, V_C=2.4V	I_{PD}		0.8	1.2	μA
VC Pin Input Current	V_{CC}=7V, V_C=3.5V	I_C		400	600	nA
Overcharge Protection Voltage	AIC1802A	V_{OCP}	4.32	4.35	4.38	V
	AIC1802B		4.27	4.30	4.33	
	AIC1802C		4.22	4.25	4.28	
Overcharge Release Voltage		V_{OCR}	3.85	4.0	4.15	V
Overdischarge Protection Voltage		V_{ODP}	2.25	2.4	2.55	V
Overdischarge Release Voltage		V_{ODR}	2.85	3.0	3.15	V
Overcurrent Protection Voltage	V_{CC}=7V	V_{OIP}	135	150	165	mV
Overcharge Delay Time (1)	V_{CC}=8.6V, V_C=4.3V, C_{TC}=0μF	T_{OC1}	12	25	38	mS
Overcharge Delay Time (2)	V_{CC}=8.6V, V_C=4.3V, C_{TC}=0.47μF	T_{OC2}	0.7	1.1	1.5	S
Overdischarge Delay Time (1)	V_{CC}=4.8V, V_C=2.4V, C_{TD}=0μF	T_{OD1}	12	25	38	mS
Overdischarge Delay Time (2)	V_{CC}=4.8V, V_C=2.4V, C_{TD}=0.47μF	T_{OD2}	0.7	1.1	1.5	S
Overcurrent Delay Time (1)	V_{CC}=7V, V_C=3.5V, V_{CS}=0.15V	T_{OI1}	4	9	14	mS
Overcurrent Delay Time (2)	V_{CC}=7V, V_C=3.5V, V_{CS}=0.36V	T_{OI2}	1.0	2.0	3.0	mS
OC Pin Source Current	V_{CC}=8.6V, V_C=4.3V, OC Pin Short to GND	I_{CO}	270	400	530	μA
OD Pin Output “H” Voltage		V_{DL}	V_{CC}-0.1		V_{CC}-0.02	V

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
OD Pin Output "L" Voltage		V_{DH}		0.01	0.1	V
Charge Detection Threshold Voltage	V_{CC}=4.8V	V_{CH}	-0.55	-0.4		V
Unbalance Discharge Current	V_{CC}=8.3V, V_C=4V	I_{UD}	5.4	7.7	10	mA

Note1: Specifications are production tested at TA = 25°C. Specifications over the -40°C to 85°C operating Temperature range are assured by design, characterization and correlation with Statistical Quality Controls (SQC).

TYPICAL PERFORMANCE CHARACTERISTICS

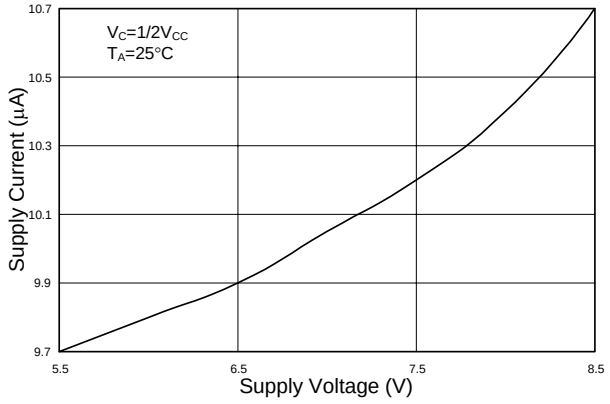


Fig. 1 Supply Current vs. Supply Voltage

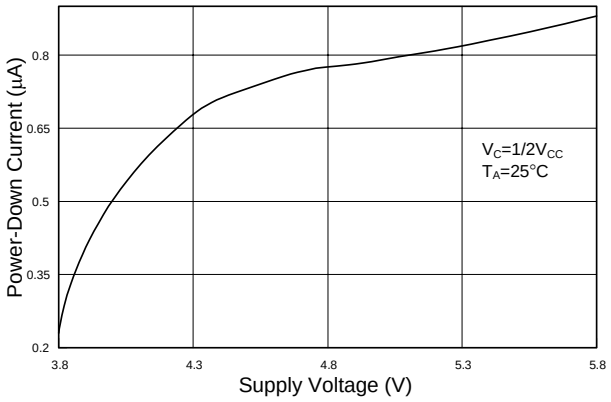


Fig. 2 Power-down Current vs. Supply Voltage

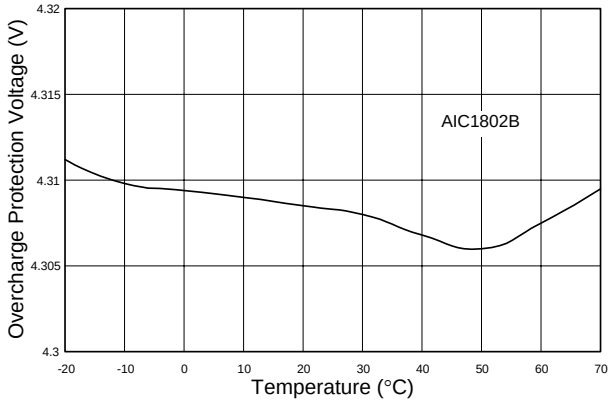


Fig. 3 Overcharge Protection Voltage vs. Temperature

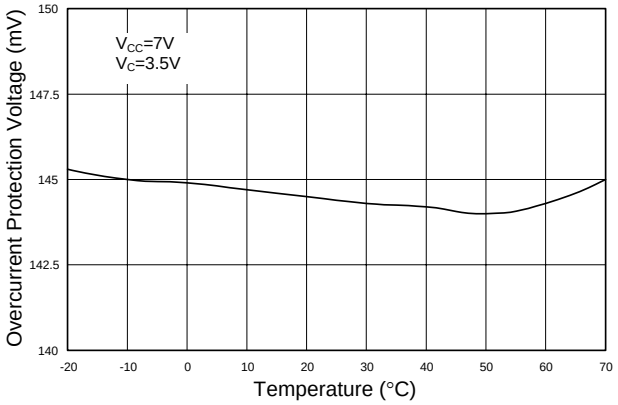


Fig. 4 Overcurrent Protection Voltage vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

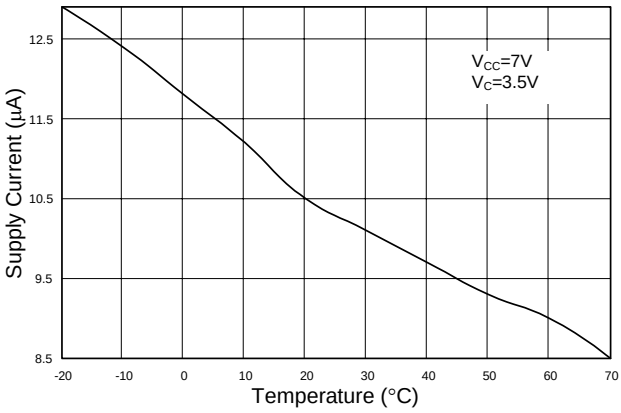


Fig. 5 Supply Current vs. Temperature

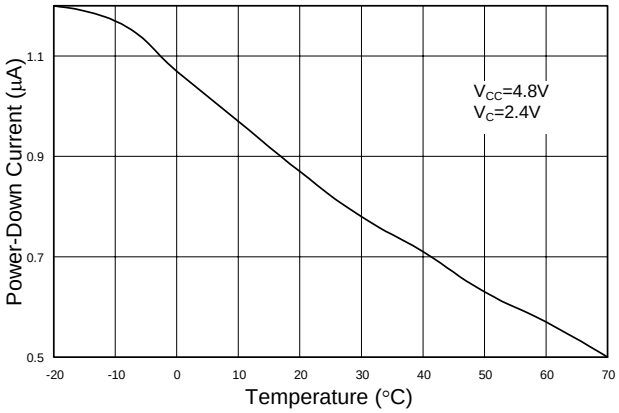


Fig. 6 Power-Down Current vs. Temperature

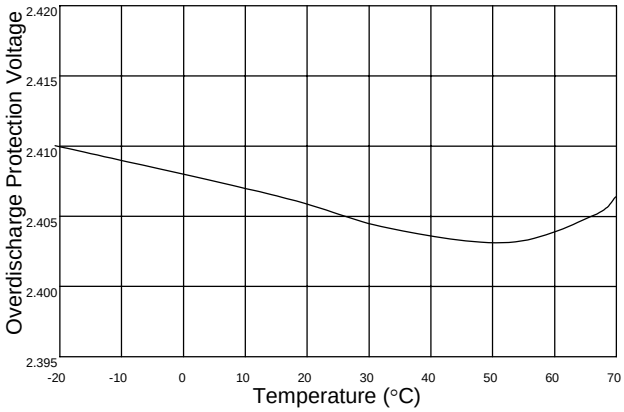


Fig. 7 Overdischarge Protection Voltage vs. Temperature

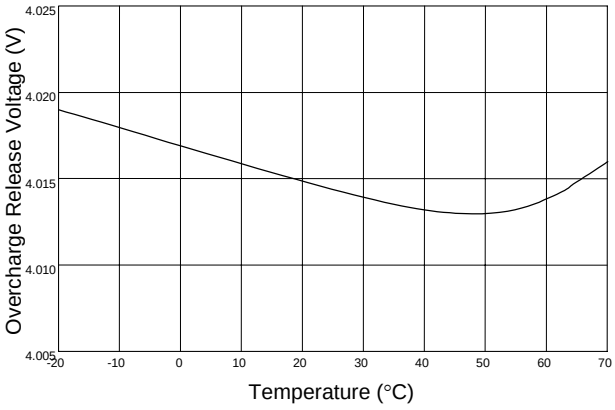


Fig. 8 Overcharge Release Voltage vs. Temperature

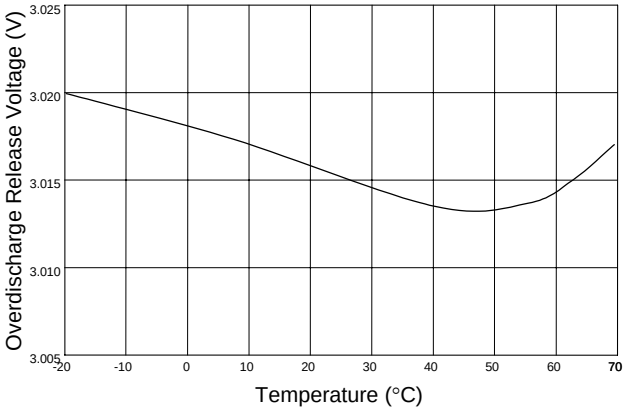
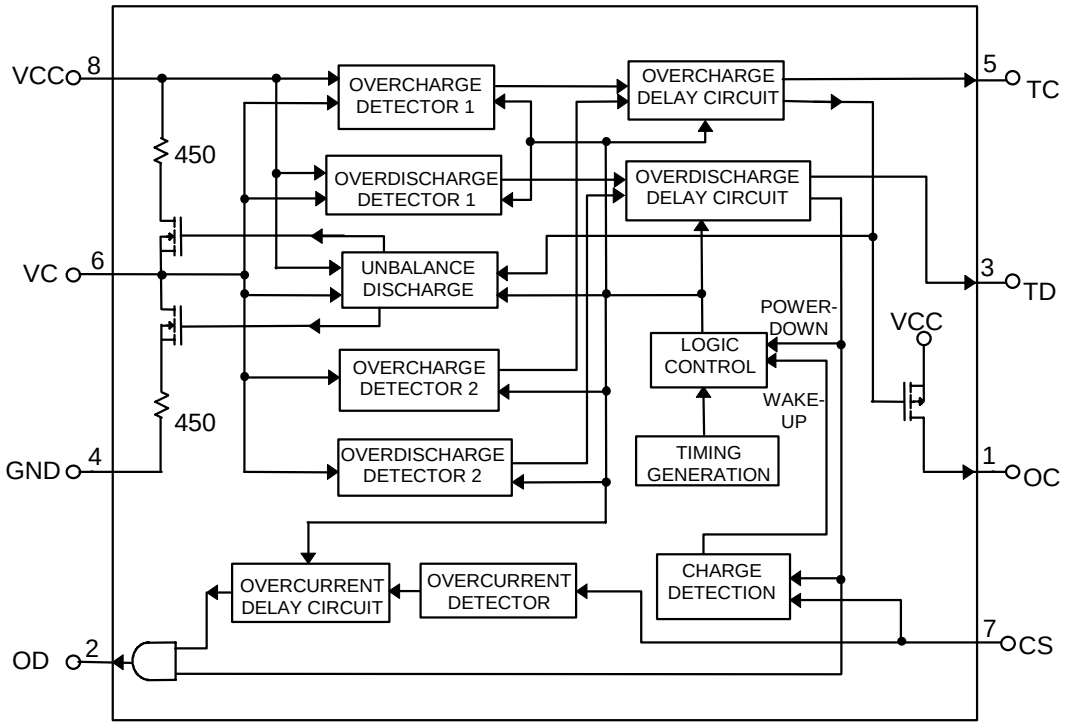


Fig. 9 Overdischarge Release Voltage vs. Temperature

BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN 1: OC - PMOS open drain output for control of the charge control MOSFET M2. When overcharge occurs, this pin sources current to switch the external NPN Q1 on, and charging is inhibited by turning off the charge control MOSFET M2.

PIN 2: OD - Output pin for control of the discharge control MOSFET M1. When overdischarge occurs, this pin goes low to turn off the discharge control MOSFET M1 and discharging is inhibited.

PIN 3: TD - Overdischarge delay time setting pin.

PIN 4: GND - Ground pin. This pin is to be connected to the negative terminal of the lower battery cell.

PIN 5: TC - Overcharge delay time setting pin.

PIN 6: VC - To be connected to the positive terminal of the lower cell and the negative terminal of the upper cell.

PIN 7: CS - Input pin for current sensing. Using the drain-source voltage of the discharge control MOSFET M1 (voltage between CS and GND), it senses discharge current during normal mode and detects whether charging current is present during power down mode.

PIN 8: VCC - Power supply pin. It is to be connected to the positive terminal of the upper cell.

APPLICATION INFORMATION

THE OPERATION

Overcharge Protection

When the voltage of either of the battery cells exceeds V_{OCP} (overcharge protection voltage) beyond the overcharge delay time period, charging is inhibited by the turning-off of the charge control MOSFET M2. The overcharge delay time (T_{OC}) defaults to 25mS and can be extended by adding a capacitor C_{TC}. Inhibition of charging is immediately released when the voltage of the overcharged cell becomes lower than V_{OCR} (overcharge release voltage) through discharge.

Overdischarge Protection

When the voltage of either of the battery cells goes below V_{ODP} (overdischarge protection voltage) beyond the overdischarge delay time period, discharging is inhibited by the turning-off of the discharge control MOSFET M1. The overdischarge delay time (T_{OD}) defaults to 25mS and can be extended by adding a capacitor C_{TD}. Inhibition of discharging is immediately released when the voltage of the overdischarged cell becomes higher than V_{ODR} (overdischarge release voltage) through charging.

Power-Down after Overdischarge

When overdischarge occurs, the SS6802 will go into power-down mode, turning off all the timing generation and detection circuitry to reduce the quiescent current to 0.8μA (V_{CC}=4.8V). In the unusual case where one battery cell is overdischarged while the other under overcharge condition, the SS6802 will turn off all the detection circuits except the overcharge detection circuit for the cell under overcharge condition.

Charge Detection after Overdischarge

When overcharge occurs, the discharge control MOSFET M1 turns off and discharging is inhibited. However, charging is still permitted through the parasitic diode of M1. Once the charger is connected to the battery pack, the SS6802 immediately turns on all the timing generation and detection circuitry and goes into normal mode. Charging is determined to be in progress if the voltage between CS and GND is below –0.4V (charge detection threshold voltage V_{CH})

Overcurrent Protection

In normal mode, the SS6802 continuously monitors the discharge current by sensing the voltage of CS pin. If the voltage of CS pin exceeds V_{OIP} (overcurrent protection voltage) beyond overcurrent delay time T_{OI} period, the overcurrent protection circuit operates and discharging is inhibited by turning-off of the discharge control MOSFET M1. Discharging must be inhibited for at least 256mS after overcurrent takes place to avoid damage to external control MOSFETs due to rapidly switching transient between V_{BAT+} and V_{BAT-} terminals. The overcurrent condition returns to the normal mode when the load is released and the impedance between the V_{BAT+} and V_{BAT-} terminals is 10MΩ or higher. For the sake of protection of the external MOSFETs, the larger the CS pin voltage (which means the larger discharge current) the shorter the overcurrent delay time. The relationship between voltage of

CS pin and overcurrent delay time T_{OI} is tabulated as below.

V_{CS} (V)	T_{OI} (S)
150m	9.0m
200m	5.6m
300m	2.8m
360m	2.0m
1V	540μ
3V	290μ
5V	270μ

Unbalanced Discharge after Overcharge

When either of the battery cells is overcharged, the SS6802 will automatically discharge the overcharged cell at about 7.7mA until the voltage of the overcharged cell is equal to the voltage of the other cell. If the voltage of the other cell is below V_{OCR}, the internal cell-balance "bleeding" will proceed until the voltage of the overcharged cell decreases to V_{OCR}.

DESIGN GUIDE

Adjustment of Overcharge and Overdischarge Delay Time

Both the overcharge and overdischarge delay times default to 25mS and can be extended by adding the external capacitors C_{TC} and C_{TD}, respectively. Increasing the capacitance value will increase the delay time. The relationship between capacitance of the external capacitors and delay time is tabulated as below:

C_{TC} (F)	T_{OC} (S)
0μ	25m
0.1μ	320m
0.3μ	890m
0.47μ	1.12
0.57μ	1.43

C_{TD} (F)	T_{OD} (S)
0μ	25m
0.1μ	320m
0.3μ	820m
0.47μ	1.08
0.57μ	1.39

Selection of External Control MOSFETs

Because the overcurrent protection voltage is preset, the threshold current for overcurrent detection is determined by the turn-on resistance of the discharge control MOSFET M1. The turn-on resistance of the external control MOSFETs can be determined by the equation: $R_{ON}=V_{OIP}/I_T$ (I_T is the overcurrent threshold current). For example, if the overcurrent threshold current I_T is designed to be 5A, the turn-on resistance of the external control MOSFETs must be 30mΩ. Users should be aware that turn-on resistance of the MOSFET changes with temperature variation due to heat dissipation. It changes with the voltage between gate and source as well. (Turn-on resistance of a MOSFET increases as the voltage between gate and source decreases). Once the turn-on resistance of the external MOSFET changes, the

overcurrent threshold current will change accordingly.

Suppressing the Ripple and Disturbance from Charger

To suppress the ripple and disturbance from charger, connecting C1 to cell 1 and C2 to cell 2 is necessary.

Controlling the Charge Control MOSFET

R3, R4, R5 and NPN transistor Q1 are used to switch the charge control MOSFET M2. If overcharge does not occur, no current flows out from OC pin and Q1 are turned off, then M2 is turned on. When overcharge occurs, current flows out from OC pin and Q1 is turned on, which turns off M2 in turn. High resistance for R3, R4, and R5 is recommended for reducing loading of the batteries.

Latch-Up Protection at CS Pin

R6 is used for latch-up protection when charger is connected under overdischarge condition, and also for overstress protection when charger is connected in reverse. The charge detection function after overdischarge is possibly disabled by larger value of R6. Resistance of 1KΩ is recommended.

Selection of R1 and R 2

R1 and R2 are used to avoid large current flow through the battery pack under the situation of IC damage or pin short. On the other hand, resistance of R1 and R2 will affect overcharge release voltage and bleeding function. The relationship among Vrelease1,Vrelease2, R1, and R2 is shown as following equations:

$Vrelease1=V_{OCR}+I_{UD}*R1$

$Vrelease2=V_{OCR}+I_{UD}*R2$

where

Vrelease1 is Battery 1, real overcharge release voltage

Vrelease2 is Battery 2, real overcharge release voltage

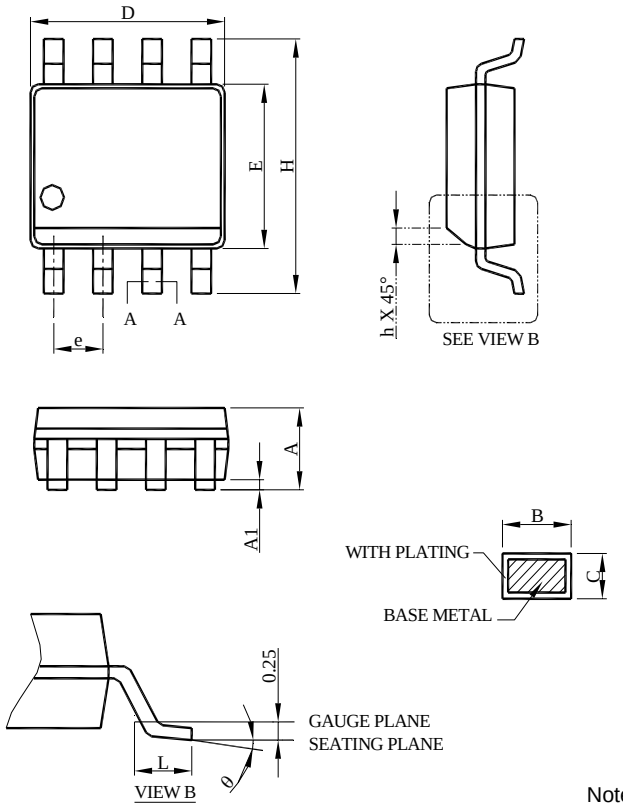
Therefore, resistance of R1 and R2 should not higher than 30Ω. Otherwise, overcharge release voltage would be higher than overcharge protection voltage and the charging current may oscillate. In addition, if overcharge protection function occurs, SS6802 will discharge the overcharged cell and will stop bleeding function even if the voltage is not equal to the other. The recommended resistance of R1 and R2 is from 20 to 30Ω.

Effect of C3

C3 has to be applied to the circuit. Because C3 will keep SS6802 to be charged after overdischarge occurred. In addition, when the differential voltage between charger and battery pack is higher than 2.1V and overcharge protection function work, C3 will avoid battery pack from being charged even if the battery voltage lower than 4V (To avoid battery pack from being charged under charger malfunction situation). The battery pack can be charged again till remove it from charger.

PHYSICAL DIMENSIONS

- **SOP-8 (unit: mm)**



SYMBOL	SOP-8	
	MILLIMETERS	
	MIN.	MAX.
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
θ	0°	8°

Note:
1.Refer to JEDEC MS-012AA.
2.Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3.Dimension “E” does not include inter-lead flash or protrusions. Inter-lead flash or protrusion shall not exceed 10 mil per side.
4.Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.