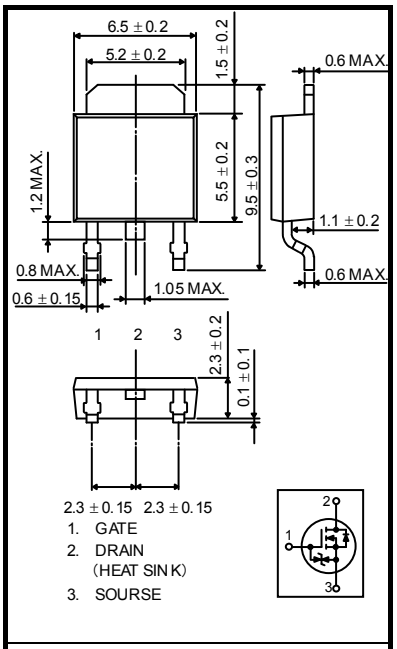
TOSHIBA Field Effect Transistor Silicon N-Channel MOS Type (π-MOSV)

2SK3462

Switching Regulator, DC/DC Converter and Motor Drive Applications

- 4 V gate drive
- Low drain-source ON-resistance: $R_{DS\ (ON)}$ = 1.2 Ω (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 2.2 S (typ.)
- Low leakage current: I_{DSS} = 100 μA (V_{DS} = 250 V)
- Enhancement mode: V_{th} = 1.5 to 3.5 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-7J1B

Weight: 0.36 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	250	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	250	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	DC (Note 1)	I_D	3	A
	Pulse (t = 1 ms) (Note 1)	I_{DP}	6	
Drain power dissipation (Tc = 25°C)		P_D	20	W
Single pulse avalanche energy (Note 2)		E_{AS}	36.2	mJ
Avalanche current		I_{AR}	3	A
Repetitive avalanche energy (Note 3)		E_{AR}	2	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristic	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch\text{-}c)}$	6.25	°C/W
Thermal resistance, channel to ambient	$R_{th\ (ch\text{-}a)}$	125	°C/W

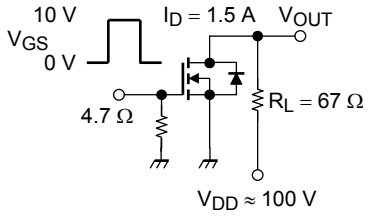
Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: V_{DD} = 50 V, T_{ch} = 25°C, L = 6.7 mH, I_{AR} = 3 A, R_G = 25 Ω

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic-sensitive device. Handle with care.

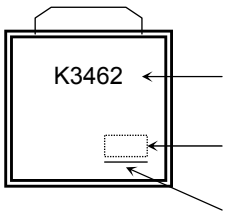
Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cutoff current		I_{DSS}	V_{DS} = 250 V, V_{GS} = 0 V	—	—	100	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	250	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	1.5	—	3.5	V
Drain-source ON-resistance		$R_{DS\ (ON)}$	V_{GS} = 10 V, I_D = 1.5 A	—	1.2	1.7	Ω
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 1.5 A	0.5	2.2	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	267	—	pF
Reverse transfer capacitance		C_{rss}		—	32	—	
Output capacitance		C_{oss}		—	98	—	
Switching time	Rise time	t_r		—	5	—	ns
	Turn-on time	t_{on}		—	20	—	
	Fall time	t_f		—	5	—	
	Turn-off time	t_{off}	Duty ≤ 1%, t_w = 10 μs	—	30	—	
Total gate charge		Q_g	V_{DD} ≈ 200 V, V_{GS} = 10 V, I_D = 3 A	—	12	—	nC
Gate-source charge		Q_{gs}		—	6	—	
Gate-drain charge		Q_{gd}		—	6	—	

Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	3	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	6	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 3 A, V_{GS} = 0 V	—	—	−2.0	V
Reverse recovery time	t_{rr}	I_{DR} = 3 A, V_{GS} = 0 V,	—	125	—	ns
Reverse recovery charge	Q_{rr}	dI_{DR}/dt = 100 A/μs	—	470	—	nC

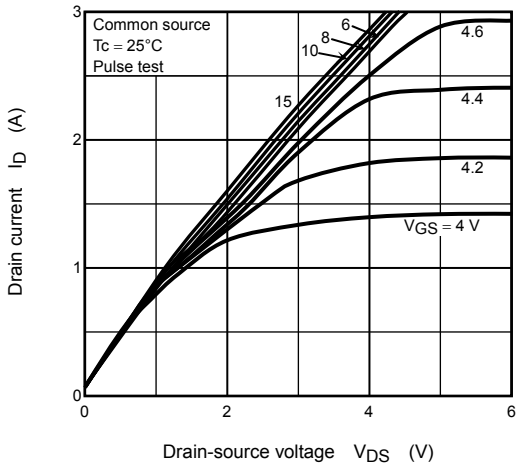
Marking



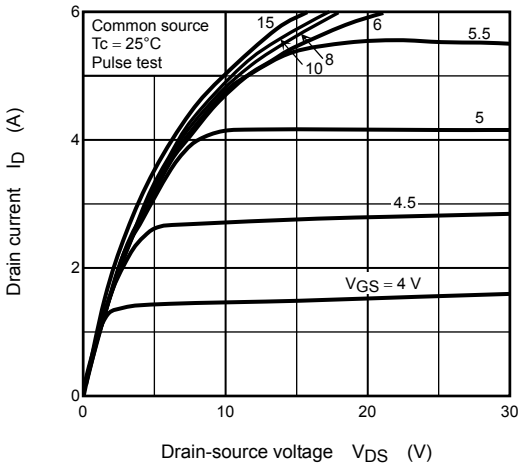
Note 4: A line under a Lot No. identifies the indication of product Labels.
Not underlined: [[Pb]]/INCLUDES > MCV
Underlined: [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. The RoHS is the Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

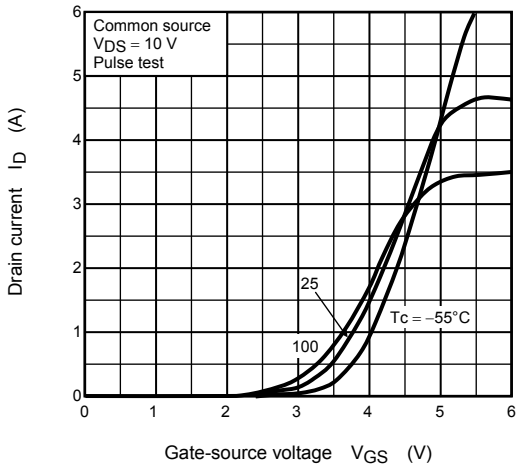
$I_D - V_{DS}$



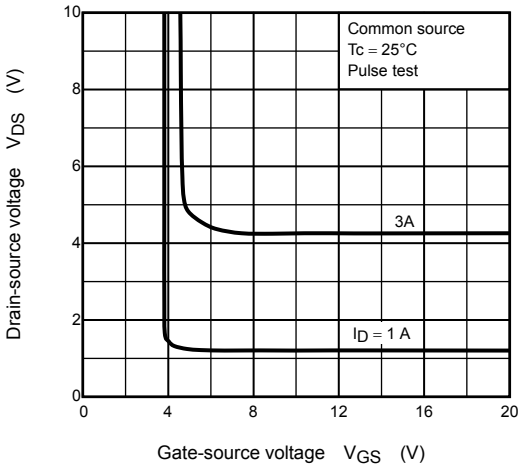
$I_D - V_{DS}$



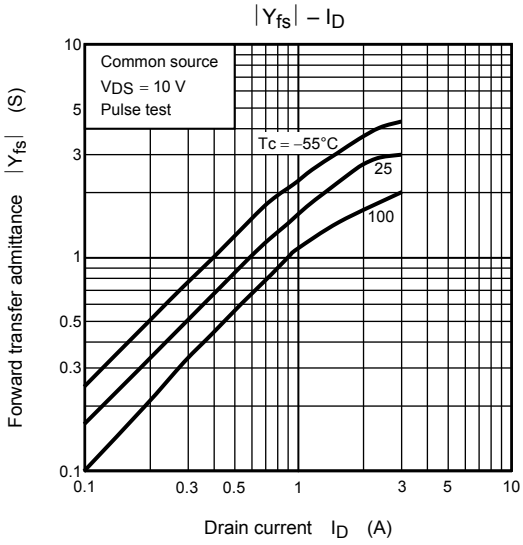
$I_D - V_{GS}$



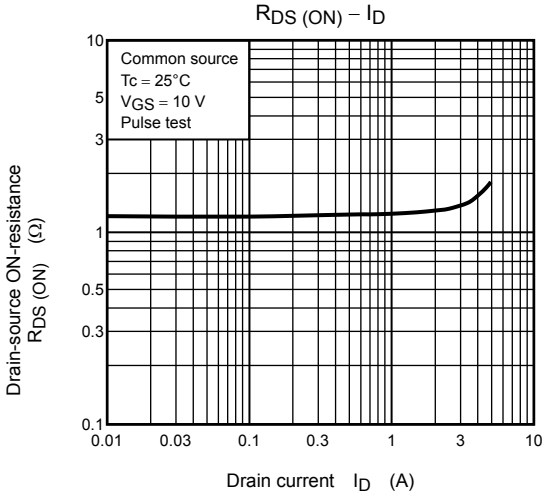
$V_{DS} - V_{GS}$



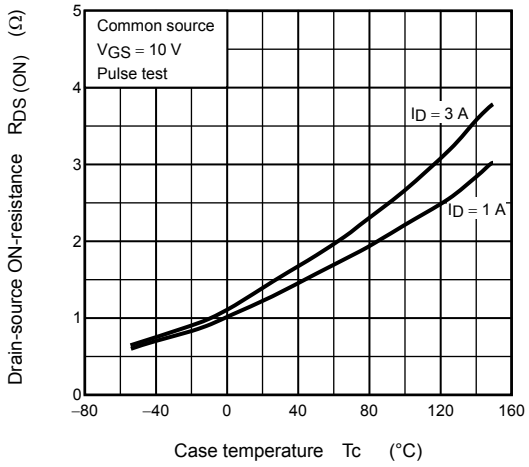
$|Y_{fs}| - I_D$



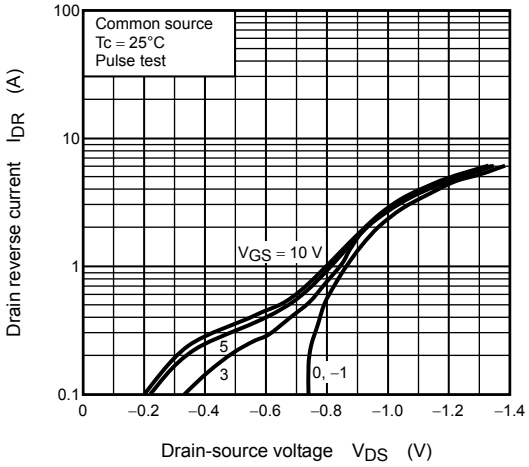
$R_{DS\ (ON)} - I_D$



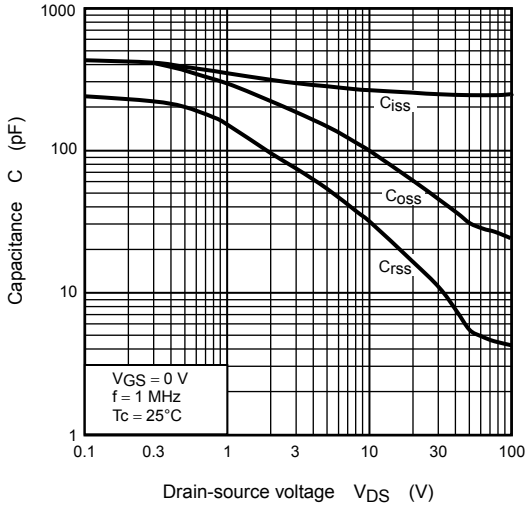
$R_{DS\ (ON)}$ – Tc



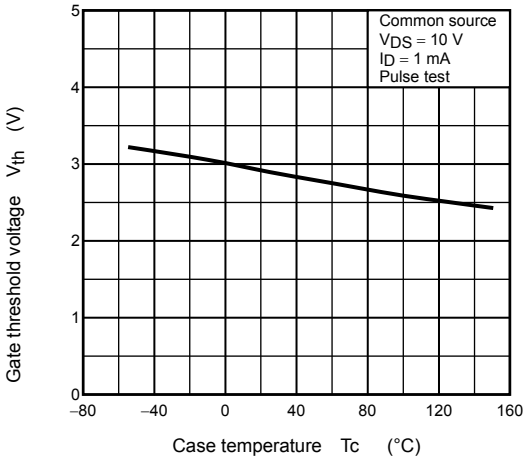
I_{DR} – V_{DS}



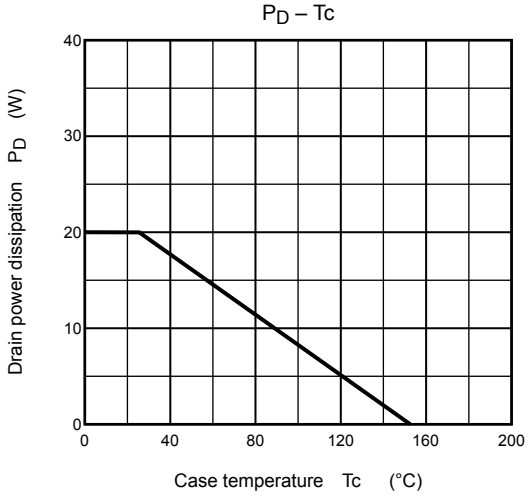
Capacitance – V_{DS}



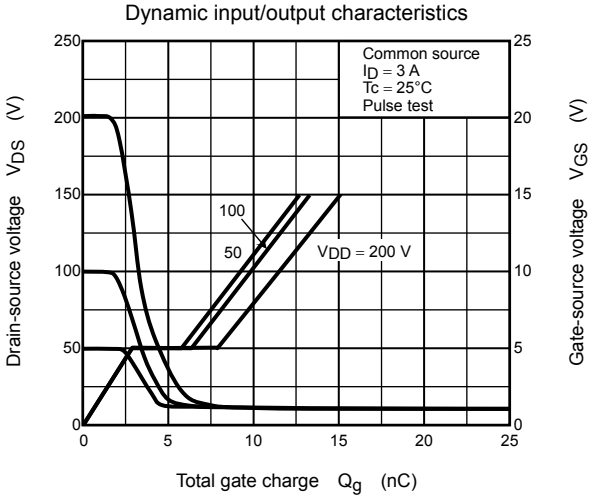
V_{th} – Tc



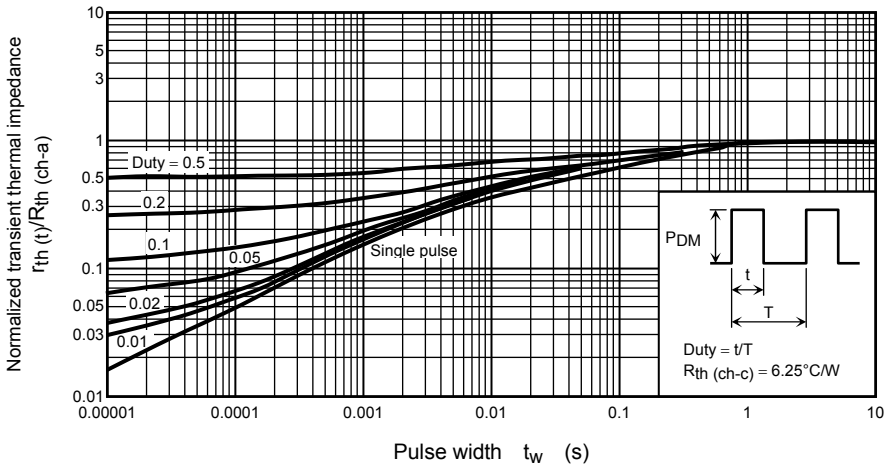
P_D – Tc



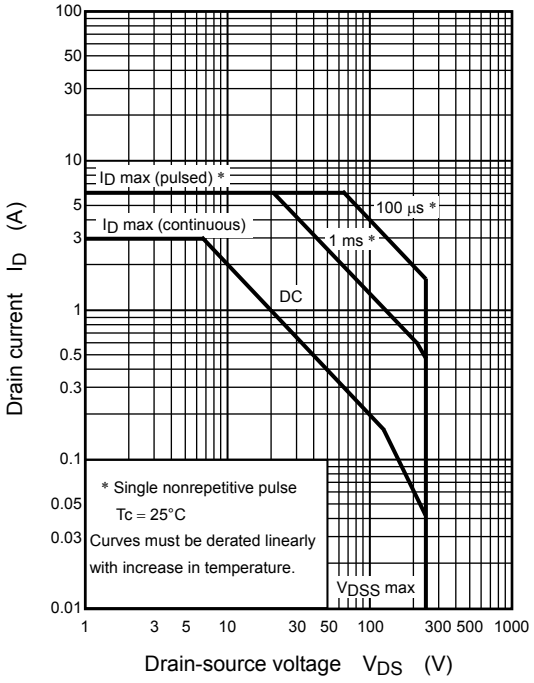
Dynamic input/output characteristics



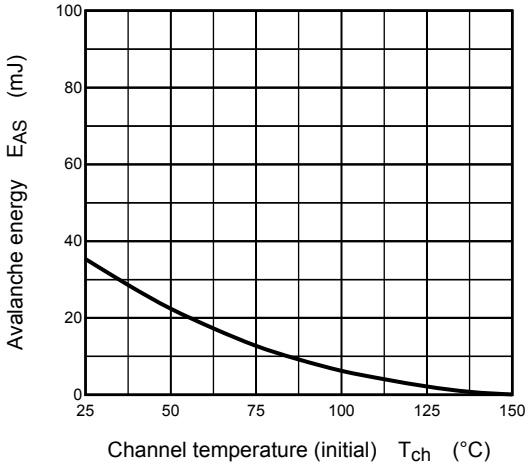
$r_{th} - t_w$

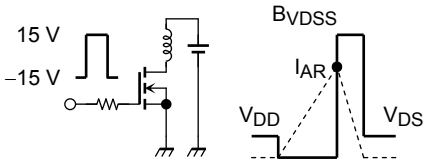


Safe operating area



$E_{AS} - T_{ch}$





Test circuit Waveform

$R_G = 25\ \Omega$
$V_{DD} = 50$ V, L = 6.7 mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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