

## Features

- Very high speed: 45 ns
- Wide voltage range: 2.2V to 3.6V and 4.5V to 5.5V
- Ultra low standby power
  - Typical standby current: 1  $\mu$ A
  - Maximum standby current: 7  $\mu$ A
- Ultra low active power
  - Typical active current: 2 mA at f = 1 MHz
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Available in Pb-free 44-pin TSOP II package

## Functional Description

The CY62136ESL is a high performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL<sup>®</sup>) in portable applications such as cellular telephones. The device also has an automatic power down feature that reduces power consumption when addresses are not toggling. Placing the device into standby

mode reduces power consumption by more than 99% when deselected ( $\overline{CE}$  HIGH). The input and output pins (IO<sub>0</sub> through IO<sub>15</sub>) are placed in a high impedance state when:

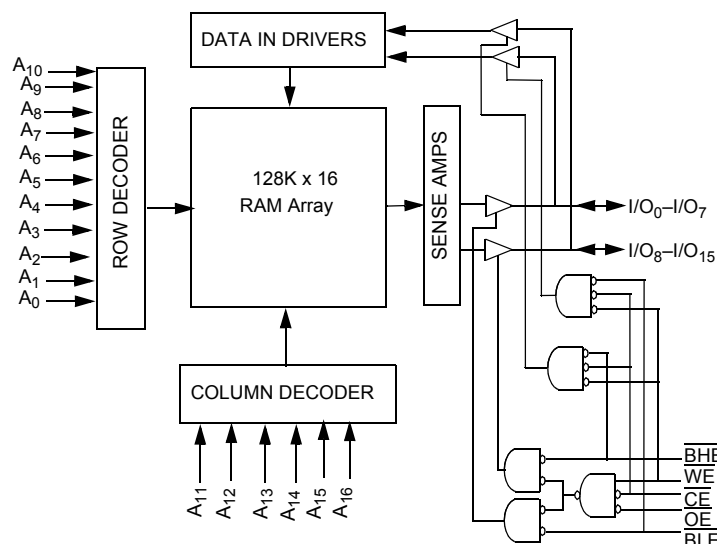
- Deselected ( $\overline{CE}$  HIGH)
- Outputs are disabled ( $\overline{OE}$  HIGH)
- Both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH)
- Write operation is active ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW)

To write to the device, take Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from IO pins (IO<sub>0</sub> through IO<sub>7</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>). If Byte High Enable (BHE) is LOW, then data from IO pins (IO<sub>8</sub> through IO<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>).

To read from the device, take Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appears on IO<sub>0</sub> to IO<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory appears on IO<sub>8</sub> to IO<sub>15</sub>. See the "Truth Table" on page 10 for a complete description of read and write modes.

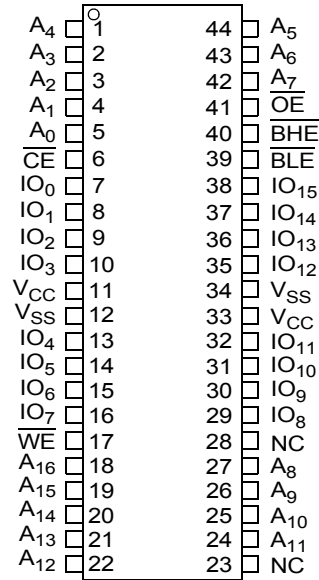
For best practice recommendations, refer to the Cypress application note [AN1064, SRAM System Guidelines](#).

## Logic Block Diagram



## Pin Configuration

Figure 1. 44-Pin TSOP II (Top View) <sup>[1]</sup>



## Product Portfolio

Product	Range	V <sub>CC</sub> Range (V) <sup>[2]</sup>	Speed (ns)	Power Dissipation					
				Operating I <sub>CC</sub> , (mA)				Standby, I <sub>SB2</sub> (μA)	
				f = 1MHz		f = f <sub>max</sub>			
				Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max
CY62136ESL	Industrial	2.2V to 3.6V and 4.5V to 5.5V	45	2	2.5	15	20	1	7

### Notes

1. NC pins are not connected on the die.
2. Datasheet specifications are not guaranteed for V<sub>CC</sub> in the range of 3.6V to 4.5V.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = 3V, and V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature .....	-65°C to +150°C
Ambient Temperature with Power Applied .....	-55°C to +125°C
Supply Voltage to Ground Potential.....	-0.5V to 6.0V
DC Voltage Applied to Outputs in High-Z State <sup>[4, 5]</sup> .....	-0.5V to 6.0V
DC Input Voltage <sup>[4, 5]</sup> .....	-0.5V to 6.0V

Output Current into Outputs (LOW).....	20 mA
Static Discharge Voltage..... (MIL-STD-883, Method 3015)	>2001V
Latch up Current.....	>200 mA

## Operating Range

Device	Range	Ambient Temperature	V <sub>CC</sub> <sup>[6]</sup>
CY62136ESL	Industrial	-40°C to +85°C	2.2V–3.6V, and 4.5V–5.5V

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns			Unit	
			Min	Typ <sup>[3]</sup>	Max		
V <sub>OH</sub>	Output HIGH Voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7	I <sub>OH</sub> = -0.1 mA	2.0		V	
		2.7 ≤ V <sub>CC</sub> ≤ 3.6	I <sub>OH</sub> = -1.0 mA	2.4			
		4.5 ≤ V <sub>CC</sub> ≤ 5.5	I <sub>OH</sub> = -1.0 mA	2.4			
V <sub>OL</sub>	Output LOW Voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7	I <sub>OL</sub> = 0.1 mA		0.4	V	
		2.7 ≤ V <sub>CC</sub> ≤ 3.6	I <sub>OL</sub> = 2.1 mA		0.4		
		4.5 ≤ V <sub>CC</sub> ≤ 5.5	I <sub>OL</sub> = 2.1 mA		0.4		
V <sub>IH</sub>	Input HIGH Voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7		1.8	V <sub>CC</sub> + 0.3	V	
		2.7 ≤ V <sub>CC</sub> ≤ 3.6		2.2	V <sub>CC</sub> + 0.3		
		4.5 ≤ V <sub>CC</sub> ≤ 5.5		2.2	V <sub>CC</sub> + 0.5		
V <sub>IL</sub>	Input LOW Voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7		-0.3	0.6	V	
		2.7 ≤ V <sub>CC</sub> ≤ 3.6		-0.3	0.8		
		4.5 ≤ V <sub>CC</sub> ≤ 5.5		-0.5	0.8		
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-1	+1	μA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled		-1	+1	μA	
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>max</sub> = 1/t <sub>RC</sub>	V <sub>CC</sub> = V <sub>CCmax</sub>		15	20	mA
		f = 1 MHz	I <sub>OUT</sub> = 0 mA, CMOS levels		2	2.5	
I <sub>SB1</sub>	Automatic CE Power Down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = f <sub>max</sub> (Address and Data Only), f = 0 ( $\overline{OE}$ , $\overline{BHE}$ , $\overline{BLE}$ and $\overline{WE}$ ), V <sub>CC</sub> = V <sub>CC(max)</sub>			1	7	μA
I <sub>SB2</sub>	Automatic CE Power Down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0, V <sub>CC</sub> = V <sub>CC(max)</sub>			1	7	μA

### Notes

- V<sub>IL</sub>(min) = -2.0V for pulse durations less than 20 ns.
- V<sub>IH</sub>(max) = V<sub>CC</sub> + 0.75V for pulse durations less than 20 ns.
- Full Device AC operation assumes a 100 μs ramp time from 0 to V<sub>CC</sub>(min) and 200 μs wait time after V<sub>CC</sub> stabilization.

### Capacitance

Tested initially and after any design or process changes that may affect these parameters.

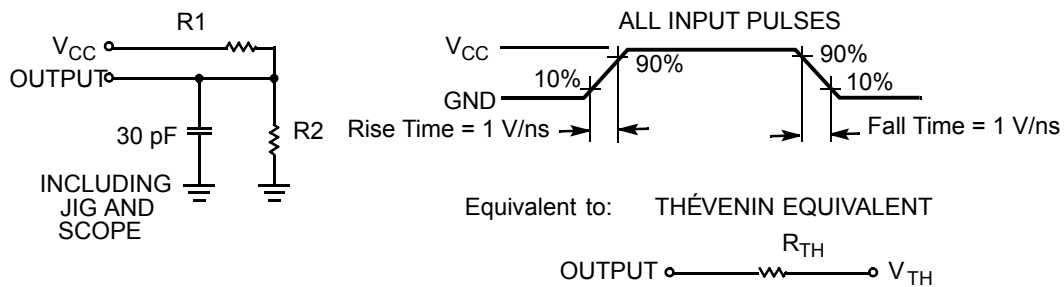
Parameter	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC</sub> (typ)	10	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

### Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	TSOP II	Unit
Θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	77	°C/W
Θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		13	°C/W

Figure 2. AC Test Loads and Waveforms



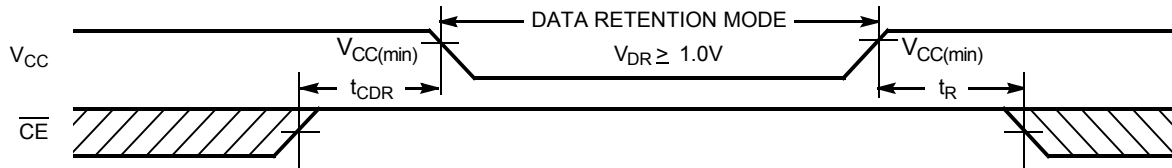
Parameters	2.5V	3.0V	5.0V	Unit
R1	16667	1103	1800	Ω
R2	15385	1554	990	Ω
R <sub>TH</sub>	8000	645	639	Ω
V <sub>TH</sub>	1.20	1.75	1.77	V

### Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		1.0			V
$I_{CCDR}$	Data Retention Current	$\overline{CE} \geq V_{CC} - 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		0.8	3	$\mu A$
$t_{CDR}^{[7]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[8]}$	Operation Recovery Time		$t_{RC}$			ns

Figure 3. Data Retention Waveform



**Notes**

- 7. Tested initially and after any design or process changes that may affect these parameters.
- 8. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 100 \mu s$  or stable at  $V_{CC(min)} \geq 100 \mu s$ .

## Switching Characteristics

 Over the Operating Range <sup>[9]</sup>

Parameter	Description	45 ns		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{RC}$	Read Cycle Time	45		ns
$t_{AA}$	Address to Data Valid		45	ns
$t_{OHA}$	Data Hold from Address Change	10		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		45	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		22	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low-Z <sup>[10]</sup>	5		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High-Z <sup>[10, 11]</sup>		18	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low-Z <sup>[10]</sup>	10		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High-Z <sup>[10, 11]</sup>		18	ns
$t_{PU}$	$\overline{CE}$ LOW to Power Up	0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power Down		45	ns
$t_{DBE}$	$\overline{BLE/BHE}$ LOW to Data Valid		22	ns
$t_{LZBE}$	$\overline{BLE/BHE}$ LOW to Low-Z <sup>[10]</sup>	5		ns
$t_{HZBE}$	$\overline{BLE/BHE}$ HIGH to High-Z <sup>[10, 11]</sup>		18	ns
<b>Write Cycle<sup>[12]</sup></b>				
$t_{WC}$	Write Cycle Time	45		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	35		ns
$t_{AW}$	Address Setup to Write End	35		ns
$t_{HA}$	Address Hold from Write End	0		ns
$t_{SA}$	Address Setup to Write Start	0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	35		ns
$t_{BW}$	$\overline{BLE/BHE}$ LOW to Write End	35		ns
$t_{SD}$	Data Setup to Write End	25		ns
$t_{HD}$	Data Hold from Write End	0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High-Z <sup>[10, 11]</sup>		18	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low-Z <sup>[10]</sup>	10		ns

### Notes

9. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3V, and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the [AC Test Loads and Waveforms on page 4](#).
10. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.
11.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high-impedance state.
12. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  or both =  $V_{IL}$ . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

### Switching Waveforms

Figure 4. Read Cycle No.1: Address Transition Controlled. [13, 14]

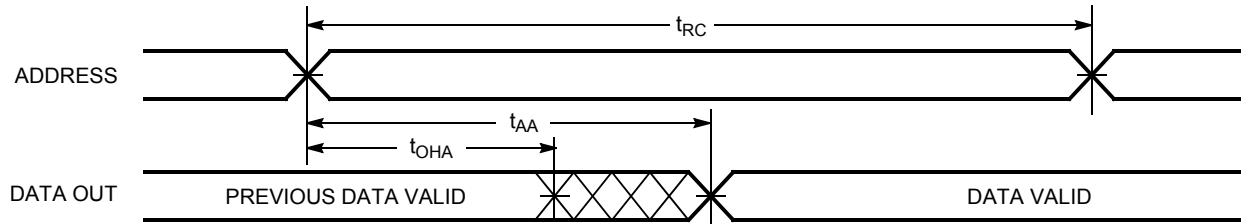
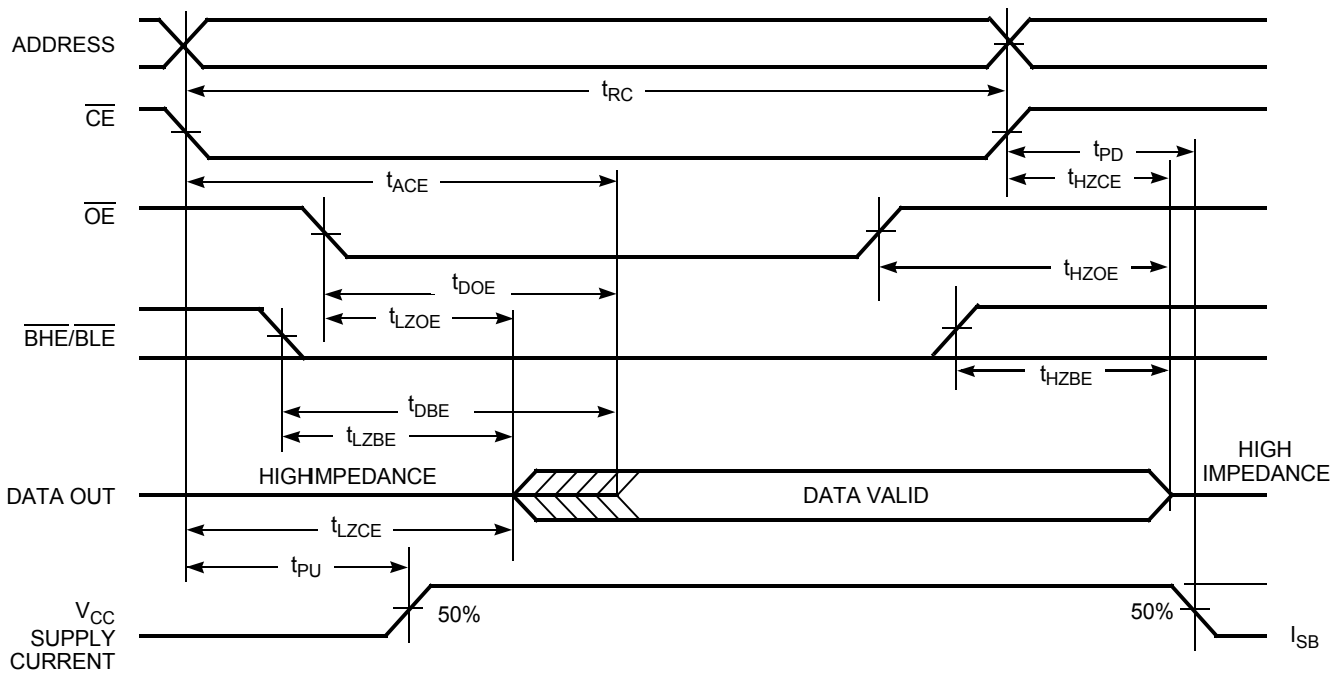


Figure 5. Read Cycle No. 2:  $\overline{\text{OE}}$  Controlled [14, 15]



**Notes**

- 13. The device is continuously selected.  $\overline{\text{OE}}$ ,  $\overline{\text{CE}}$  =  $V_{\text{IL}}$ ,  $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$ , or both =  $V_{\text{IL}}$ .
- 14.  $\overline{\text{WE}}$  is HIGH for read cycle.
- 15. Address valid before or similar to  $\overline{\text{CE}}$ ,  $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$  transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle No 1:  $\overline{WE}$  Controlled [12, 16, 17]

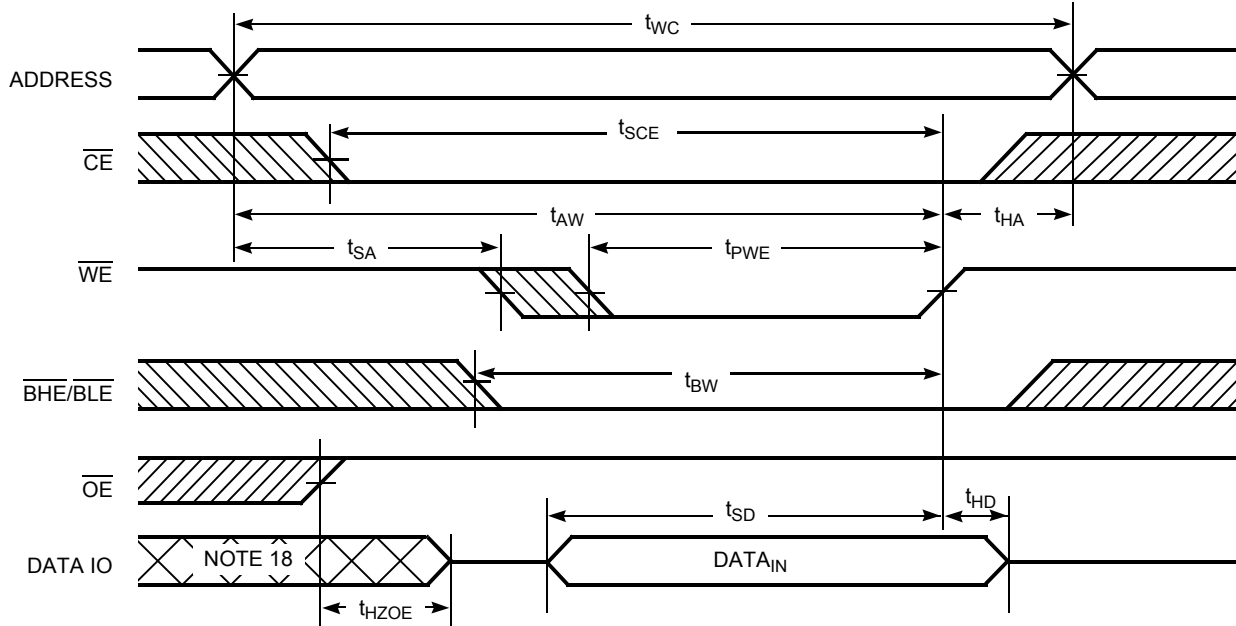
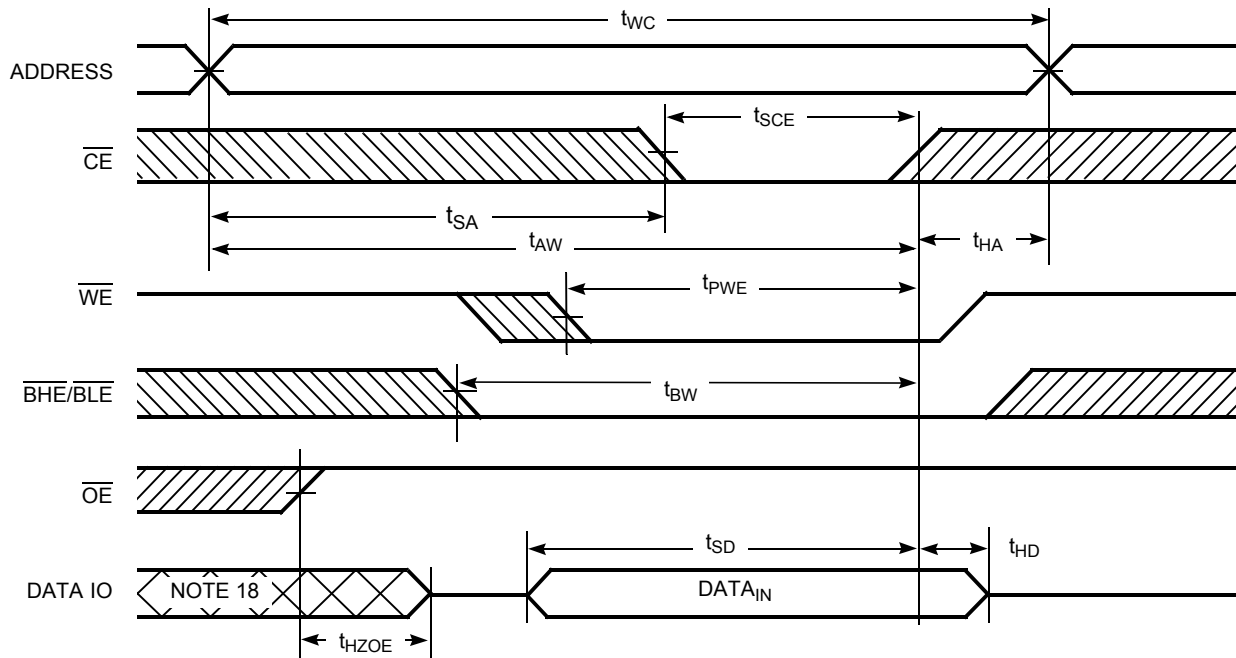


Figure 7. Write Cycle 2:  $\overline{CE}$  Controlled [12, 16, 17]



Notes

- 16. Data IO is high impedance if  $\overline{OE} = V_{IH}$ .
- 17. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.
- 18. During this period, the IOs are in output state. Do not apply input signals.



Switching Waveforms (continued)

Figure 8. Write Cycle 3:  $\overline{WE}$  Controlled,  $\overline{OE}$  LOW <sup>[17]</sup>

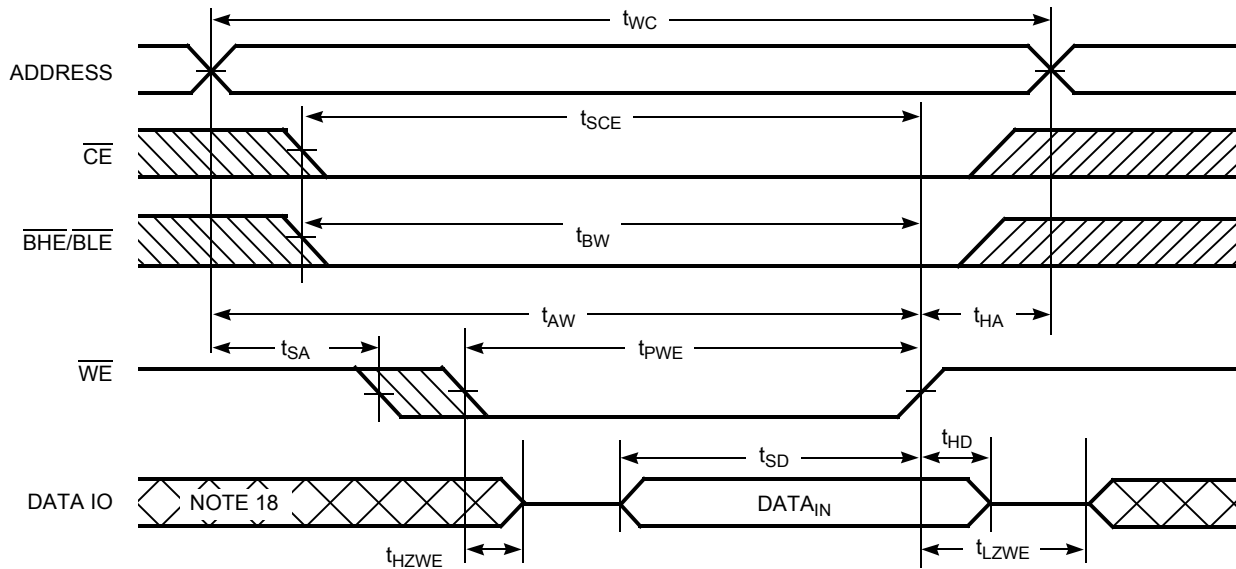
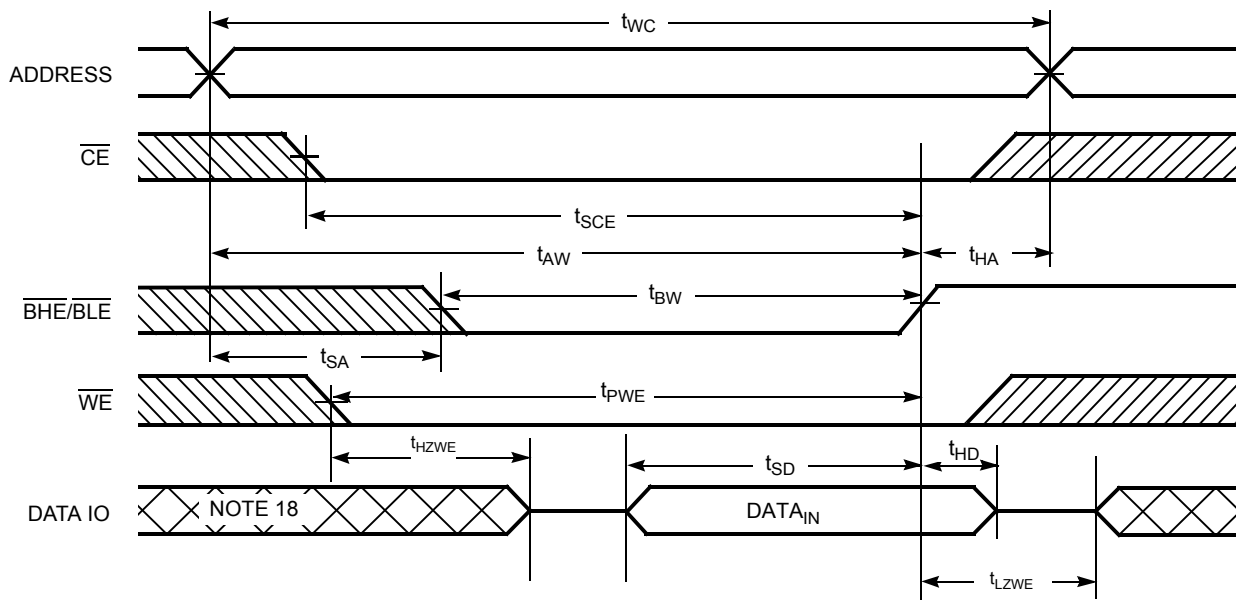


Figure 9. Write Cycle 4:  $\overline{BHE/BLE}$  Controlled,  $\overline{OE}$  LOW <sup>[17]</sup>



**Truth Table**

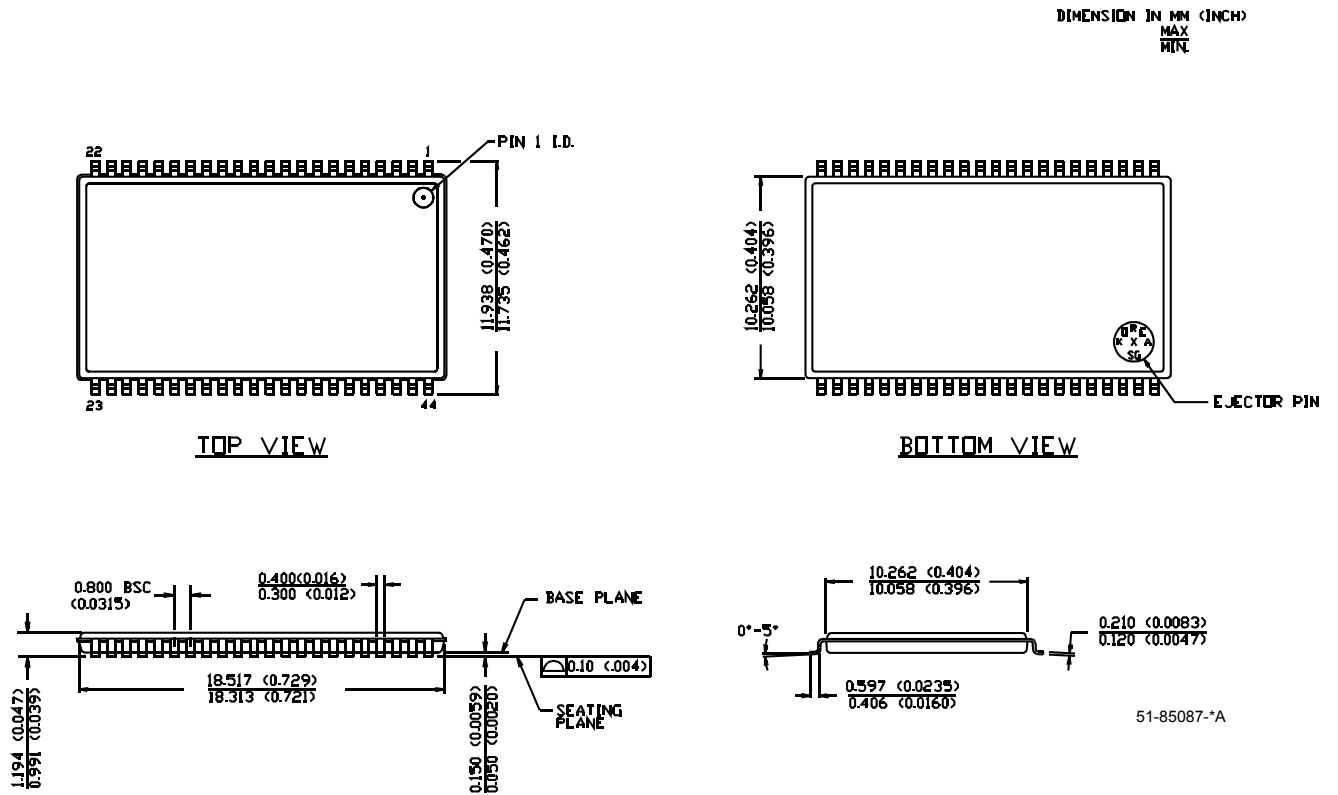
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/Power Down	Standby ( $I_{SB}$ )
L	X	X	H	H	High-Z	Output Disabled	Active ( $I_{CC}$ )
L	H	L	L	L	Data Out ( $IO_0$ – $IO_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	L	H	L	Data Out ( $IO_0$ – $IO_7$ ); $IO_8$ – $IO_{15}$ in High-Z	Read	Active ( $I_{CC}$ )
L	H	L	L	H	Data Out ( $IO_8$ – $IO_{15}$ ); $IO_0$ – $IO_7$ in High-Z	Read	Active ( $I_{CC}$ )
L	H	H	L	L	High-Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	High-Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	L	H	High-Z	Output Disabled	Active ( $I_{CC}$ )
L	L	X	L	L	Data In ( $IO_0$ – $IO_{15}$ )	Write	Active ( $I_{CC}$ )
L	L	X	H	L	Data In ( $IO_0$ – $IO_7$ ); $IO_8$ – $IO_{15}$ in High-Z	Write	Active ( $I_{CC}$ )
L	L	X	L	H	Data In ( $IO_8$ – $IO_{15}$ ); $IO_0$ – $IO_7$ in High-Z	Write	Active ( $I_{CC}$ )

**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62136ESL-45ZSXI	51-85087	44-Pin Thin Small Outline Package Type II (Pb-Free)	Industrial

Package Diagram

Figure 10. 44-Pin TSOP II, 51-85087



## Document History Page

Document Title: CY62136ESL MoBL® 2 Mbit (128K x 16) Static RAM Document Number: 001-48147				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	2615537	VKN/PYRS	12/03/08	New Data Sheet
*A	2718906	VKN	06/15/2009	Post to external web

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