Murata Power Solutions

DAC-330
10-Bit, Multiplying D/A Converter

PRODUCT DATA SHEET

OBSOLETE PRODUCT

Contact Factory for Replacement Model

FEATURES

- 10-Bit resolution
- 160 MHz conversion rate
- Multiplying — 14 MHz bandwidth
- ECL compatible
- Single (−5V) supply
- Low-power
- Low-glitch

APPLICATIONS

- Graphic displays
- High definition video displays
- Ultra high-speed signal processing
- Digital VTR
- Digital attenuators
- High-speed function generators

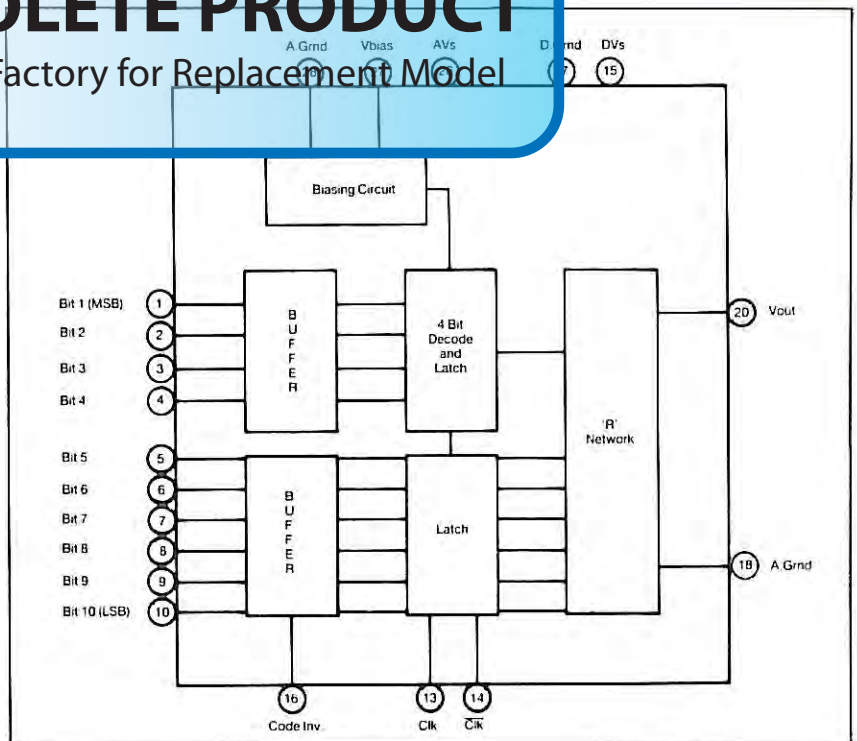
GENERAL DESCRIPTION

The monolithic DAC-330 is an ultra high-speed, 10-bit digital-to-analog converter. This ECL-compatible device has a 160 MHz update rate and a 14 MHz multiplying bandwidth capability.

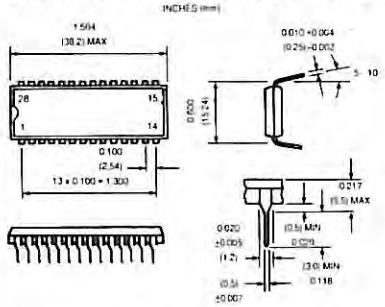
The DAC-330 develops an output voltage of 0 to −1.0V and can directly drive a 75Ω impedance load. Settling time is 5.2 nSec. while glitch energy is a low 15 picovolt/second. Other features of this D/A are integral linearity of 0.1% FS, and a differential linearity of ±1/2 LSB maximum.

Input coding of the DAC-330 can be programmed for straight binary or complementary binary through use of the COMP BIN control input line.

The DAC-330 is a low-power device requiring only a single −5.2V supply with a maximum current draw of 100 mA. The DAC-330 is packaged in a 28-pin plastic DIP and has an operating temperature range of −20°C to +75°C.



MECHANICAL DIMENSIONS



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	28	ANALOG GROUND
2	BIT 2	27	VBIAS
3	BIT 3	26	ANALOG SUPPLY (−5.0V)
4	BIT 4	25	N/C
5	BIT 5	24	N/C
6	BIT 6	23	N/C
7	BIT 7	22	N/C
8	BIT 8	21	N/C
9	BIT 6	20	ANALOG OUTPUT
10	BIT 10 (LSB)	19	N/C
11	N/C	18	ANALOG GROUND (R−2R)
12	N/C	17	DIGITAL GROUND
13	CLOCK INPUT (CLK)	16	CODE INVERSE INPUT
14	CLOCK INPUT ($\overline{CLK}$)	15	DIGITAL SUPPLY (−5.0V)

ORDERING INFORMATION

MODEL	OPERATING TEMPERATURE RANGE
DAC-330	−20°C to +75°C

ABSOLUTE MAXIMUM RATINGS (1)
(T_a = +25°C unless otherwise specified.

Power Supply Voltage, (Vs), (pins 15 + 26)	−7.0V dc
Digital Input Voltages	−Vs to +0.3V dc
Analog Output Current	20 mA
Operating Temperature Range	−20°C to +75°C
Storage Temperature Range	−65°C to +150°C
Reference Input Voltage	Vs to +0.3V
Allowable Power Dissipation	1.43 W

FUNCTIONAL SPECIFICATIONS
Typical at +25°C, ANA Vs = −5.2V dc, DIG Vs = −5.2V dc unless otherwise noted.

DIGITAL INPUTS	MIN.	TYP.	MAX.	UNITS
Resolution	10	—	—	bits
Coding (using Pin 16)				
Comp Bin = 0V		Straight Binary		
Comp Bin = −5.2V		Complementary Binary		
Data and Clock Inputs				
Logic "1" voltage	−0.74	−0.89	−1.04	V dc
Logic "0" voltage	−1.60	−1.75	−1.90	V dc
4 MSB's Data				
Logic "1" current	0.1	1.5	6.0	µA
Logic "0" current	0.1	1.5	6.0	µA
6 LSB's Data				
Logic "1" current	0.1	0.75	3.0	µA
Logic "0" current	0.1	0.75	3.0	µA
Clock				
Logic "1"current	2.0	23	70	µA
Comp Bin				
Logic "1" current	0.1	1.5	6.0	µA
Data				
Set Up Time (Tsu)	—	—	5.0	nSec.
Hold Time (Thd)	—	—	1.0	nSec.
REFERENCE				
Reference Input Voltage	−3.8	−4.2	−4.7	V dc
Reference Input Current	−0.1	−0.4	−3.0	µA
ANALOG OUTPUTS				
Output Resistance	.52	65	78	Ω
Output Voltage F.S.				
R ≥ 10K	−0.8	−1.0	−1.6	V dc
R = 75	−0.8	−1.0	−1.2	VDC
PERFORMANCE				
Conversion Rate (2)	160	—	—	MHz
Linearity Error	—	—	±0.1	% FS
Differential Linearity	—	—	±1/2	LSB
Gain Tempco				
R ≥ 10 kΩ	—	−140	−280	ppm/°C
R = 75Ω	—	−580	−1200	ppm/°C
Zero Offset	—	−7	−21	mV
Zero Offset Tempco (3)	6	16	22	µV/°C
Propagation Delay (Tpd) (2)	—	3.8	—	nSec.
Settling Time (Tset)	—	4.7	—	nSec.
Rise Time (Tr) (2)	—	1.5	—	nSec.
Fall Time (Tf) (2)	—	1.5	—	nSec.
Glitch Energy	—	15	—	pV/Sec.
Multiplying Bandwidth −3 dB, (2)	10	14	—	MHz
POWER SUPPLY REQUIREMENTS				
Supply Voltage Range	−4.75	−5.2	−5.45	V
Supply Current	−65	−85	−100	mA
PHYSICAL-ENVIRONMENTAL				
Operating Temp Range	−20°C to +75°C (ambient)			
Storage Temperature Range	−55°C to +150°C			
Package Type	28-pin plastic DIP			

(1)Absolute maximum ratings are limiting values, which when exceeded will yield derated performance of the device and may cause damage to the device.
(2)R = 75 Ω, −3 dB
(3)R ≥ 10 KΩ

TABLE 1. INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	28	ANA GND
2	BIT 2	27	V REF
3	BIT 3	26	ANA VS (−5.2V)
4	BIT 4	25	N/C
5	BIT 5	24	N/C
6	BIT 6	23	N/C
7	BIT 7	22	N/C
8	BIT 8	21	N/C
9	BIT 9	20	ANA OUT
10	BIT 10 (LSB)	19	N/C
11	N/C	18	ANA GND
12	N/C	17	DIG GND
13	CLK	16	COMP. BIN.
14	CLK	15	DIG VS (−5.2V)

TABLE 2. INPUT/OUTPUT CODING

RANGE	DIGITAL INPUT CODE	ANALOG OUTPUT VOLTAGE Comp. Bin = 0V (Pin 16 to DIG GND) STRAIGHT BINARY		ANALOG OUTPUT VOLTAGE Comp. Bin. = −5.2V (Pin 16 to −5.2V) COMP. BINARY	
−FS + 1 LSB	1111 1111 11	−999.02	mV	−0.9766	mV
−15/16 FS	1111 0000 00	−937.5	mV	−62.5	mV
−7/8 FS	1110 0000 00	−865	mV	−124	mV
−3/4 FS	1100 0000 00	−750	mV	−250	mV
−1/2 FS	1000 0000 00	−500	mV	−500	mV
−1/4 FS	0100 0000 00	−250	mV	−750	mV
−1/8 FS	0010 0000 00	−125	mV	−875	mV
−1/16 FS	0001 0000 00	−62.5	mV	−937.5	mV
−1 LSB	0000 0000 01	−0.9766	mV	−999.02	mV
0	0000 0000 00	0.0000	mV	−1.0000	VS

TECHNICAL NOTES

1. **Data Input Coding**
The relation between the binary input code and the analog output voltage is programmed by the COMP BIN control line (pin 16). When COMP BIN is connected to DIG GND (Pin 17) the input coding is straight binary, if COMP BIN is connected to DIG Vs (Pin 15) the input coding is complementary binary.

2. **Clock Inputs**
Input data to the DAC-330 is latched on the rising edge (0 to 1) of CLK (pin 14). The clock inputs $\overline{\text{CLK}}$ and CLK (pins 13 and 14 respectively) must be at ECL levels. An alternative method is to drive the CLK (pin 14) and set pin 13 ($\overline{\text{CLK}}$) to the mid-point of an ECL level by an external source. Refer to Figure 4 for typical connections.

3. **Digital Input Considerations**
When the DAC-330 is operated at the maximum conversion rate (160 MHz), it is suggested that ECL-100K logic gates be used to drive the inputs of the DAC. The data and clock drivers, for maximum performance, must be terminated at the DAC inputs with the Thevenin equivalent resistance of 50Ω at a dc level of −2V. Further the termination resistors should be placed as close as possible to the digital input pins of the D/A. Refer to Figure 11 for typical connections.

4. **Reference Voltage**
The full-scale output voltage (ANA OUT) of the DAC is determined by the reference voltage (VREF) on pin 27. Also ANA OUT varies in proportion to the voltage difference between pin 27 (VREF) and pin 26 (ANA Vs). The range in which a linear relationship is established beatween ANA IN and VREF is:

0.50V to 1.5V

To reduce high-frequency noise on the analog output (ANA OUT, pin 20), install a 0.01 μF ceramic capacitor as close as possible between pin 26 (ANA IN) and pin 27 (VREF).

Two circuits for deriving the reference voltage (VREF) are shown in Figures 3 and 4. Figure 3 simply divides the power supply voltage with two resistors. However the analog output voltage of this circuit will vary with any deviation in the supply voltage. Figure 4 eliminates the influence of supply deviations by using a voltage regulator resulting in a more stable analog output voltage.

5. **Output Load Considerations:**
The DAC-330 is a device which uses a load resistance to develop an output voltage. A typical value of the load resistance is 75Ω. Both the full scale output voltage and the zero offset voltage temperature coefficients are dependent on the load resistance. Larger value load resistances result in a lower value temperature coefficient. Refer to output versus temperature chart in Figure 10.

6. **Multiplying Operation:**
To use the DAC-330 in the multiplying mode, apply an external modulation signal coupled by a .001 μF capacitor to pin 27 (VREF). Also remove the 0.01 μF ceramic capacitor connected between pins 26 and 27. Refer to the schematic in Figure 5.

To set up the DAC-330 for multiplying operation:

a. Set the digital inputs (all 1s for straight binary or all 0s for complementary binary for full scale output ANA OUT on Pin 20.

b. With no AC signal applied to pin 27, adjust the 1.5 KΩ potentiometer so that the analog output (pin 20) is −1.0V. The DC voltage at pin 27 is then defined as VREF.

c. Then apply the AC signal such that the amplitude of the signal at pin 27 becomes (VREF +5.2)/2

7. **Power Supply Considerations:**
The board layout should have a ground plane and Vs (supply voltage) plane (−5.2V) as large as possible to reduce parasitic reactance and resistance. The analog and digital grounds should be separated on the printed circuit board, as well as the analog and digital −5.2V (Vs) power lines. For the best system noise reduction, the only place the analog and digital power and ground lines should be interconnected is at the main system power supply.

Both the analog and digital supplies should be bypassed by a 47 μF Tantalum and a 100 pF ceramic capacitor installed as close as possible to the DAC-330.

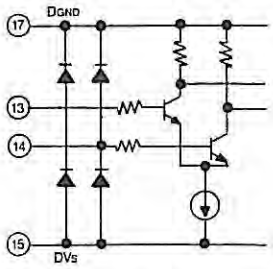


Figure 1. Clock Inputs

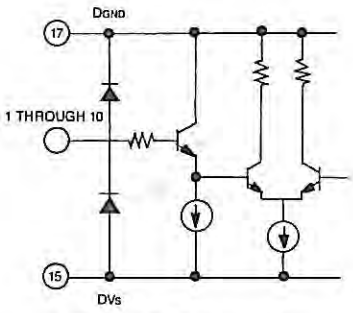


Figure 2. Data Inputs

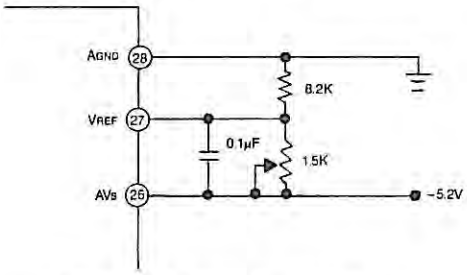


Figure 3. Voltage Reference

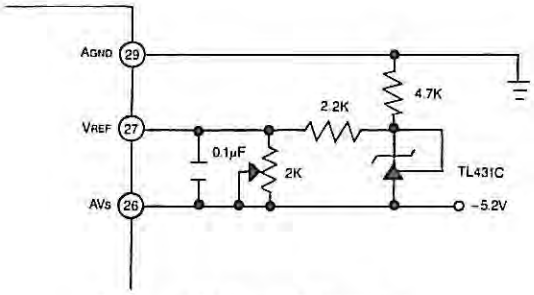


Figure 4. Voltage Reference

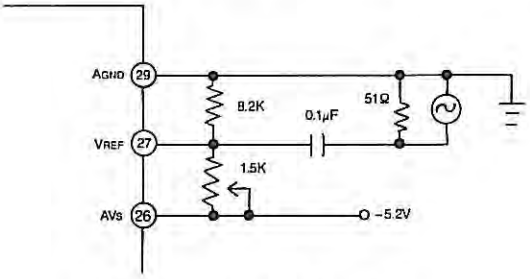


Figure 5. Multiple Circuits

TIMING NOTES

Data input update must be completed at least 5 nSec. before the positive transition of the clock (CLK).

$$T_S \geq 5 \text{ nSec.}$$

The input data is latched into the converter at the CLK and $\overline{CLK}$ crossover points. The data at the input must be held for at least 1 nSec. after this.

$$Thd \geq 1 \text{ nSec.}$$

The analog output will start to change to a new value after a propagation delay of typically 3.8 nSec.

$$Tpd = 3.8 \text{ nSec. (Typ.)}$$

Rise time (Tr) and fall time (Tf) for a full-scale change in analog output is typically 1.5 nSec.

$$Tr = Tf = 1.5 \text{ nSec. (Typ.)}$$

The settling time is calculated from the fall or rise time using the formula.

$$T \text{ (setting)} = 3.45 \times Tr \text{ (or } Tf) \text{ nSec.}$$
$$= 5.2 \text{ nSec.}$$

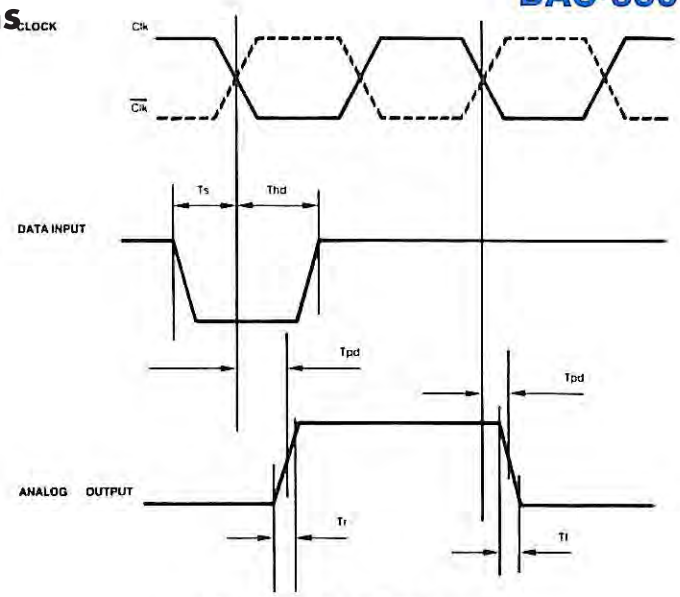


Figure 6. Timing Diagram

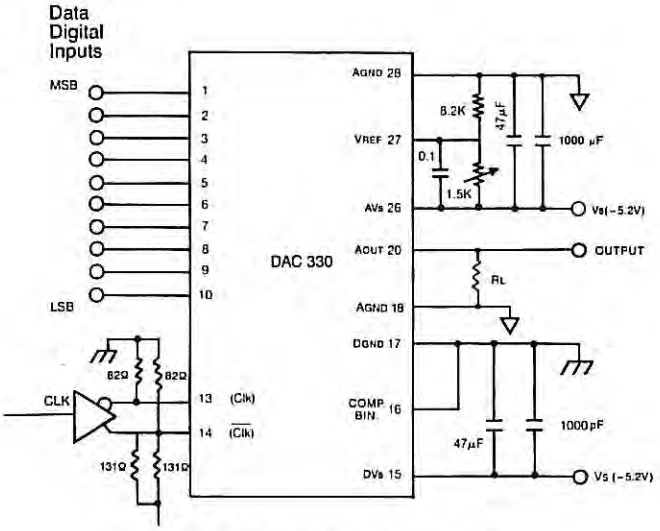


Figure 7. Connection Diagram

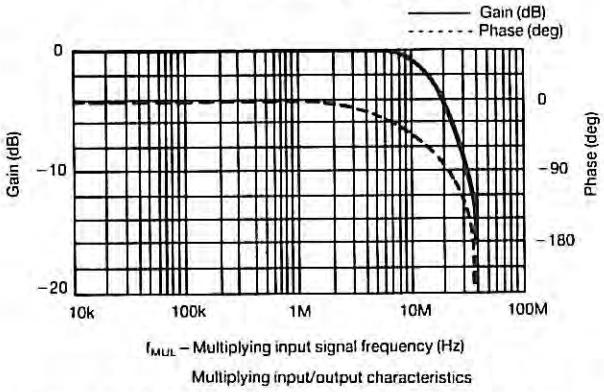


Figure 8. Multiplying Input/Output Characteristics

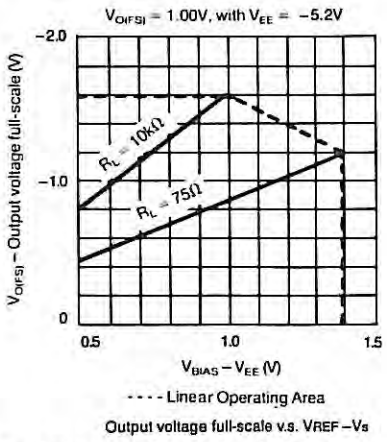


Figure 9. Output Voltage Full-Scale vs VREF –Vs

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