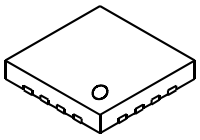
X-SP4T SWITCH GaAs MMIC

■ GENERAL DESCRIPTION

The NJG1663K44 is a X (Cross) -SP4T* switch GaAs MMIC, which is suitable for switching of balanced bandpass filters. The NJG1663K44 features very low phase error between on-state paths, low insertion loss, low control voltage and wide frequency coverage. The ESD protection circuits are integrated in the IC to achieve high ESD tolerance. The very small and very thin QFN16-44 package is adopted.

*) X-SP4T is a paired SP4T switch controlled synchronously. The X-SP4T includes two SP4T switches whose RF lines have crossings inside the MMIC.

■ PACKAGE OUTLINE



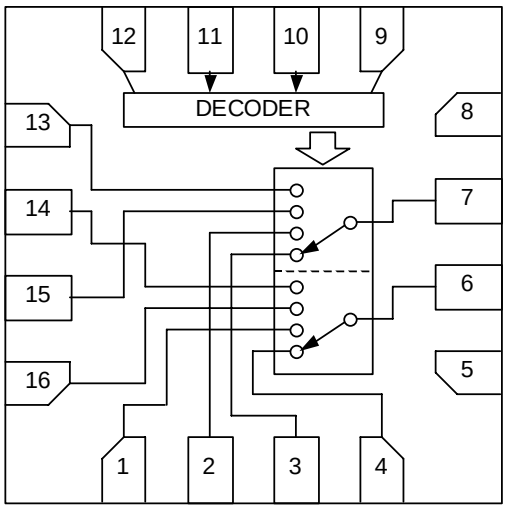
NJG1663K44

■ FEATURES

- Low phase error ±5 deg @f=2.0GHz
- Low operation voltage V_{DD}=+1.5~+4.5V
- Low control voltage $V_{CTL(H)}$=+1.3V min.
- Low insertion loss 0.45dB typ. @1.0GHz, 0.55dB typ. @2.0GHz
- High isolation 26dB typ. @1.0GHz, 20dB typ. @2.0GHz
- High ESD tolerance Integrated ESD protection circuit
- Small and thin package QFN16-44 (Package size: 2.3mm x 2.3mm x 0.45mm typ)
- Lead and halogen-free

■ PIN CONFIGURATION

(Top View)



Pin connection

1.	P2B	10.	CTL2
2.	P2A	11.	CTL1
3.	P1A	12.	GND
4.	P1B	13.	P4A
5.	GND	14.	P4B
6.	PCB	15.	P3A
7.	PCA	16.	P3B
8.	GND		
9.	VDD		

■ TRUTH TABLE

"H"=$V_{CTL(H)}$, "L"=$V_{CTL(L)}$

ON PATH	CTL1	CTL2
PCA-P1A, PCB-P1B	H	L
PCA-P2A, PCB-P2B	L	L
PCA-P3A, PCB-P3B	L	H
PCA-P4A, PCB-P4B	H	H

Note: The Information on this datasheet will be subject to change without notice.

■ ABSOLUTE MAXIMUM RATINGS

(T_a=+25°C, Z_s=Z_l=50Ω)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
RF Input Power	P_{IN}	V_{DD} =2.7V, V_{CTL}=0V/1.8V	28	dBm
Supply Voltage	V_{DD}	VDD terminal	5.0	V
Control Voltage	V_{CTL}	CTL1,CTL2 terminals	5.0	V
Power Dissipation	P_D	Four-layer FR4 PCB (50mmx50mm), T_j=150°C	1300	mW
Operating Temp.	T_{opr}		-40~+85	°C
Storage Temp.	T_{stg}		-55~+150	°C

■ ELECTRICAL CHARACTERISTICS

(General conditions: T_a=+25°C, Z_s=Z_l=50Ω, V_{DD}=2.7V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V, with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		1.5	2.7	4.5	V
Operating Current	I_{DD}	P_{IN}=0dBm	-	30	60	μA
Control Voltage (LOW)	$V_{CTL(L)}$		0	0	0.4	V
Control Voltage (HIGH)	$V_{CTL(H)}$		1.3	1.8	4.5	V
Control Current	I_{CTL}	f=1.0GHz, P_{IN}=0dBm	-	5	10	μA

■ ELECTRICAL CHARACTERISTICS

(General conditions: T_a=+25°C, Z_s=Z_l=50Ω, V_{DD}=2.7V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V, with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Loss 1	LOSS1	f=1.0GHz, P_{IN}=0dBm	-	0.45	0.65	dB
Insertion Loss 2	LOSS2	f=2.0GHz, P_{IN}=0dBm	-	0.55	0.75	dB
Insertion Loss 3	LOSS3	f=2.7GHz, P_{IN}=0dBm	-	0.80	1.00	dB
Isolation 1	ISL1	PCA-P1A, P2A, P3A, P4A PCB-P1B, P2B, P3B, P4B f=1.0GHz, P_{IN}=0dBm	24	26	-	dB
Isolation 2	ISL2	PCA-P1A, P2A, P3A, P4A PCB-P1B, P2B, P3B, P4B f=2.0GHz, P_{IN}=0dBm	17	20	-	dB
Isolation 3	ISL3	PCA-P1A, P2A, P3A, P4A PCB-P1B, P2B, P3B, P4B f=2.7GHz, P_{IN}=0dBm	15	17	-	dB
Isolation 4	ISL4	PCA-PCB port f=2.0GHz, P_{IN}=0dBm	18	20	-	dB
Phase error	PE	f=2.0GHz, between ON paths	-5	-	5	deg
Input power at 0.2dB Compression Point	$P_{-0.2dB}$	f=2.0GHz	20	23	-	dBm
VSWR	$VSWR_i$	f=2.0GHz, On port	-	1.2	1.4	-
Switching time	T_{SW}	50% V_{CTL} to 10/90% RF	-	2	5	μs

■ TERMINAL INFORMATION

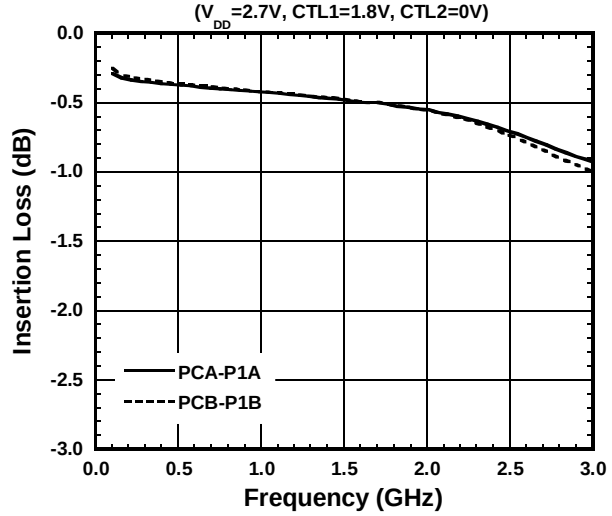
No.	SYMBOL	DESCRIPTION
1	P2B	The 2nd RF port of the 2nd switch. This port is connected with PCB port. PCA port is connected with P2A port at the same time. An external capacitor is required to block DC voltage.
2	P2A	The 2nd RF port of the 1st switch. This port is connected with PCA port. PCB port is connected with P2B port at the same time. An external capacitor is required to block DC voltage.
3	P1A	The 1st RF port of the 1st switch. This port is connected with PCA port. PCB port is connected with P1B port at the same time. An external capacitor is required to block DC voltage.
4	P1B	The 1st RF port of the 2nd switch. This port is connected with PCB port. PCA port is connected with P1A port at the same time. An external capacitor is required to block DC voltage.
5	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
6	PCB	Common RF port of the 2nd switch. This port is connected with either of P1B, P2B, P3B, and P4B port. An external capacitor is required to block DC voltage.
7	PCA	Common RF port of the 1st switch. This port is connected with either of P1A, P2A, P3A, and P4A port. An external capacitor is required to block DC voltage.
8	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
9	VDD	Positive voltage supply terminal. The positive voltage (+1.5~+4.5V) has to be supplied. Please connect a bypass capacitor with GND terminal for excellent RF performance.
10	CTL2	Control signal input terminal. This terminal is set to High-Level (+1.3V~4.5V) or Low-Level (0~+0.4V).
11	CTL1	Control signal input terminal. This terminal is set to High-Level (+1.3V~4.5V) or Low-Level (0~+0.4V).
12	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
13	P4A	The 4th RF port of the 1st switch. This port is connected with PCA port. PCB port is connected with P4B port at the same time. An external capacitor is required to block DC voltage.
14	P4B	The 4th RF port of the 2nd switch. This port is connected with PCB port. PCA port is connected with P4A port at the same time. An external capacitor is required to block DC voltage.
15	P3A	The 3rd RF port of the 1st switch. This port is connected with PCA port. PCB port is connected with P3B port at the same time. An external capacitor is required to block DC voltage.
16	P3B	The 3rd RF port of the 2nd switch. This port is connected with PCB port. PCA port is connected with P3A port at the same time. An external capacitor is required to block DC voltage.

■ ELECTRICAL CHARACTERISTICS

(General conditions: T_a=+25°C, Z_S=Z_I=50Ω, losses of external circuit are excluded, with application circuit)

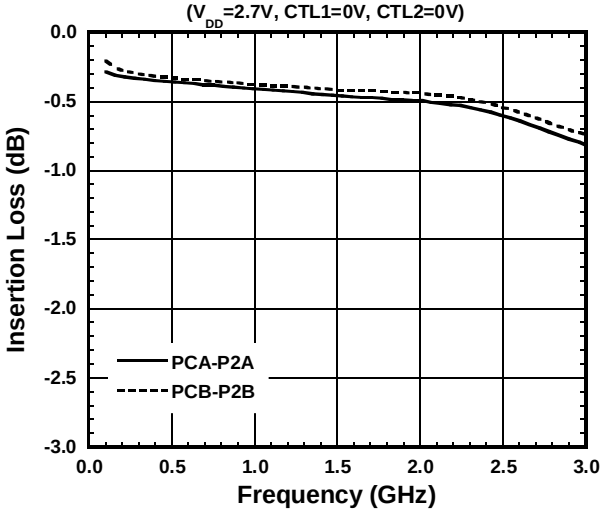
Insertion Loss vs. Frequency

(V_{DD}=2.7V, CTL1=1.8V, CTL2=0V)



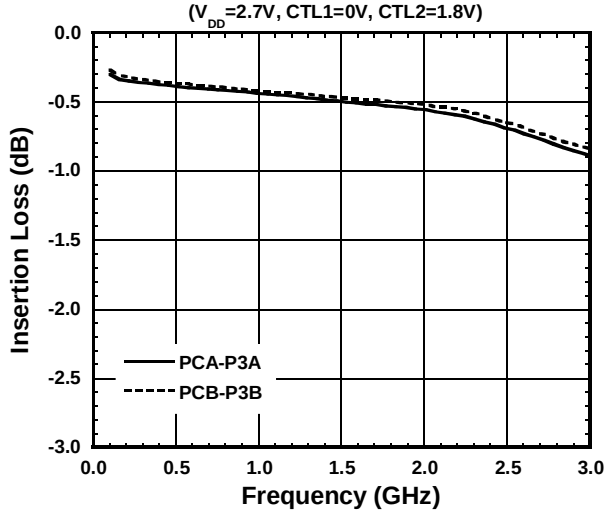
Insertion Loss vs. Frequency

(V_{DD}=2.7V, CTL1=0V, CTL2=0V)



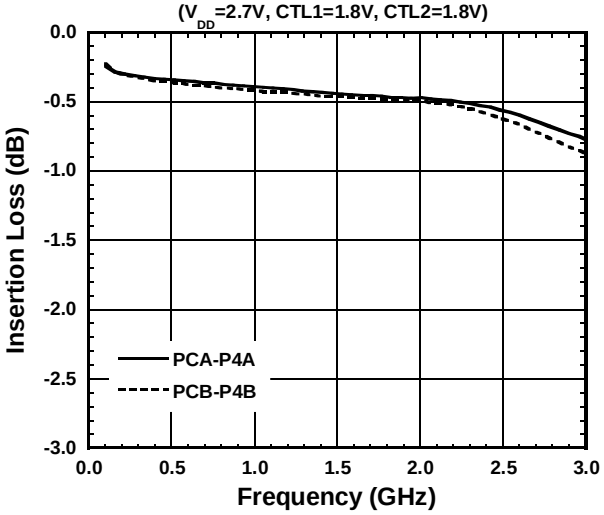
Insertion Loss vs. Frequency

(V_{DD}=2.7V, CTL1=0V, CTL2=1.8V)



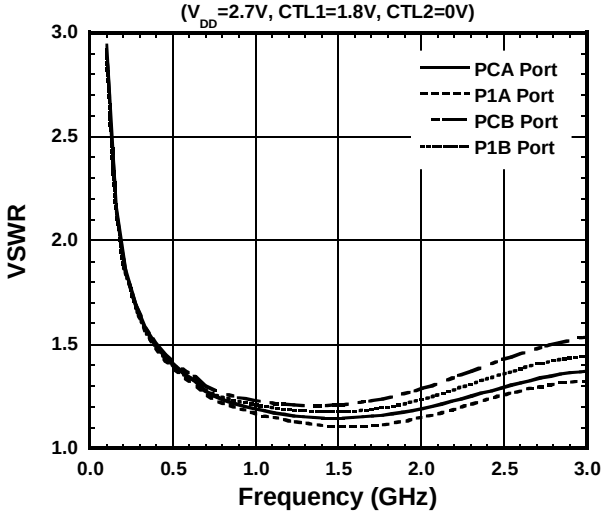
Insertion Loss vs. Frequency

(V_{DD}=2.7V, CTL1=1.8V, CTL2=1.8V)



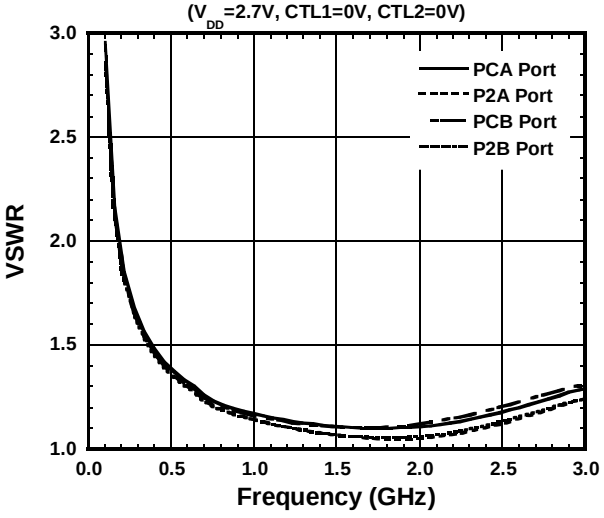
VSWR vs. Frequency

(V_{DD}=2.7V, CTL1=1.8V, CTL2=0V)



VSWR vs. Frequency

(V_{DD}=2.7V, CTL1=0V, CTL2=0V)

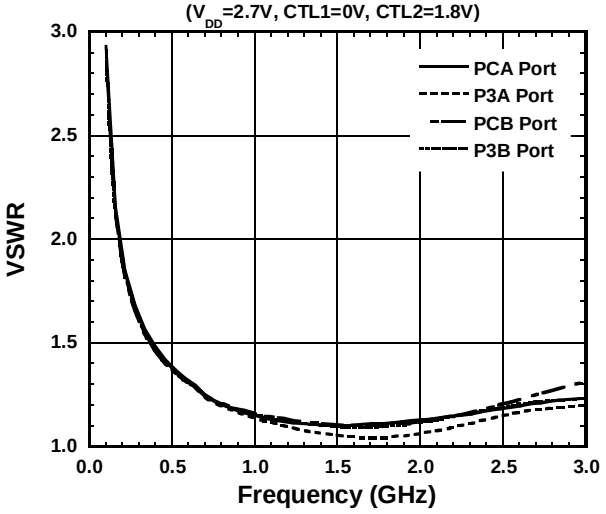


■ ELECTRICAL CHARACTERISTICS

(General conditions: T_a=+25°C, Z_S=Z_I=50Ω, losses of external circuit are excluded, with application circuit)

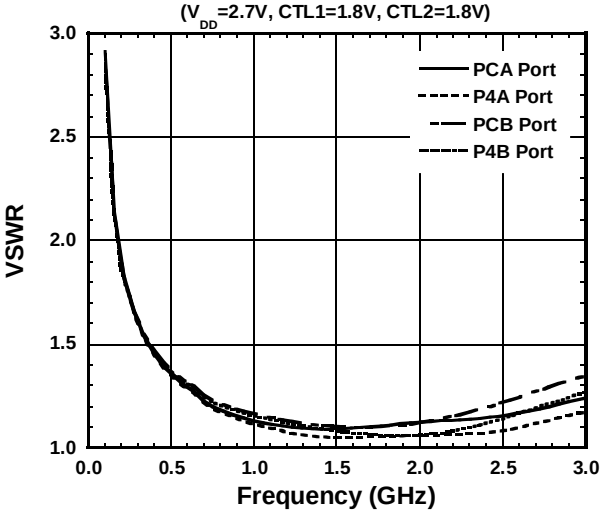
VSWR vs. Frequency

(V_{DD}=2.7V, CTL1=0V, CTL2=1.8V)



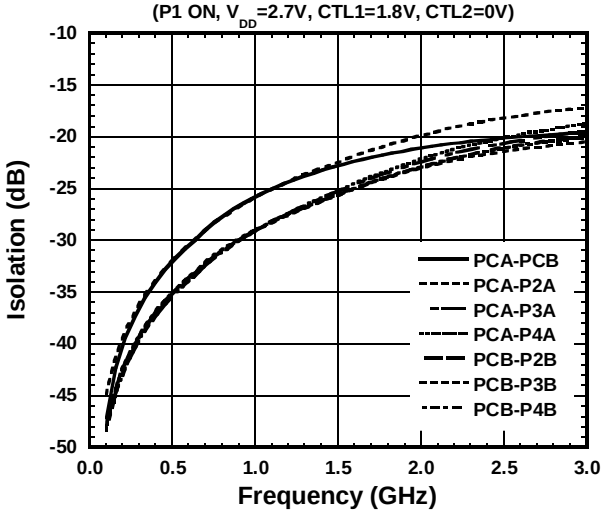
VSWR vs. Frequency

(V_{DD}=2.7V, CTL1=1.8V, CTL2=1.8V)



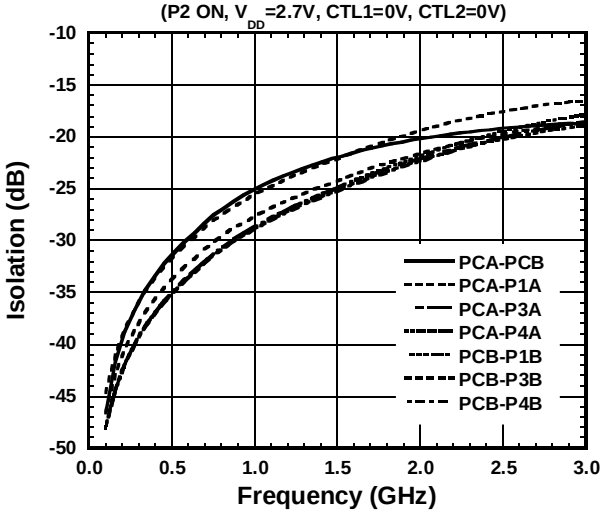
Isolation vs. Frequency

(P1 ON, V_{DD}=2.7V, CTL1=1.8V, CTL2=0V)



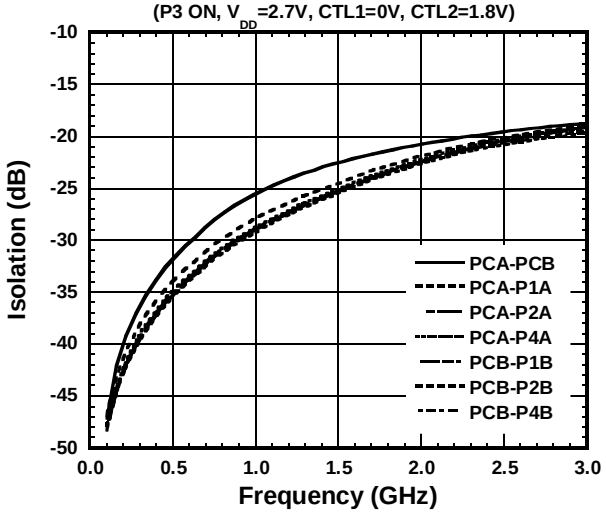
Isolation vs. Frequency

(P2 ON, V_{DD}=2.7V, CTL1=0V, CTL2=0V)



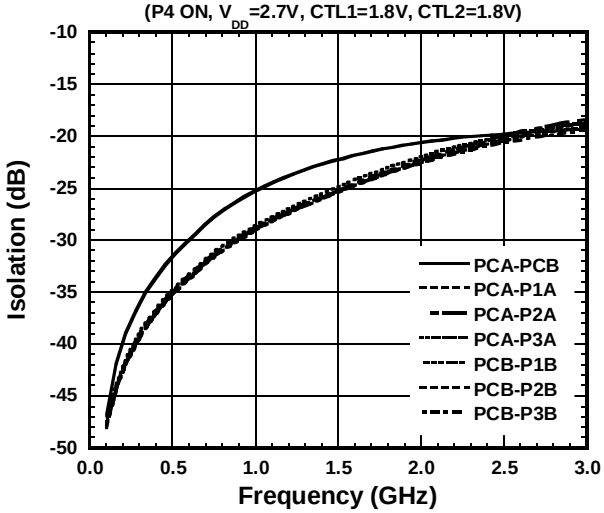
Isolation vs. Frequency

(P3 ON, V_{DD}=2.7V, CTL1=0V, CTL2=1.8V)



Isolation vs. Frequency

(P4 ON, V_{DD}=2.7V, CTL1=1.8V, CTL2=1.8V)

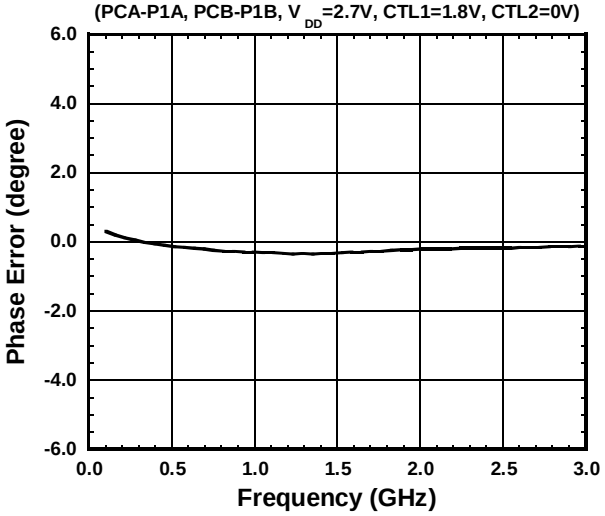


■ ELECTRICAL CHARACTERISTICS

(General conditions: T_a=+25°C, Z_S=Z_l=50Ω, losses of external circuit are excluded, with application circuit)

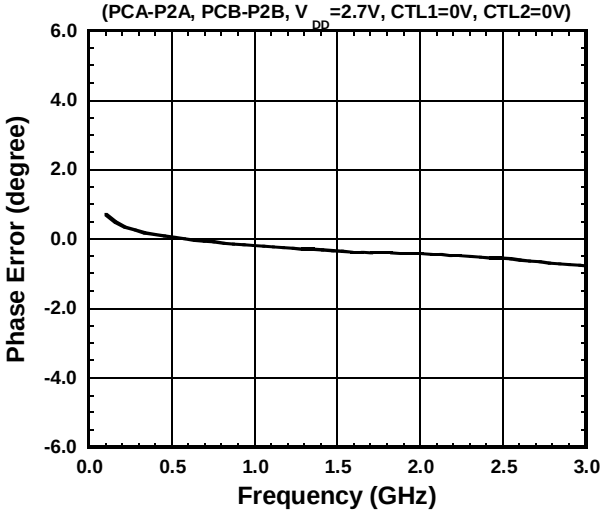
PC-P1 Phase Error vs. Frequency

(PCA-P1A, PCB-P1B, V_{DD}=2.7V, CTL1=1.8V, CTL2=0V)



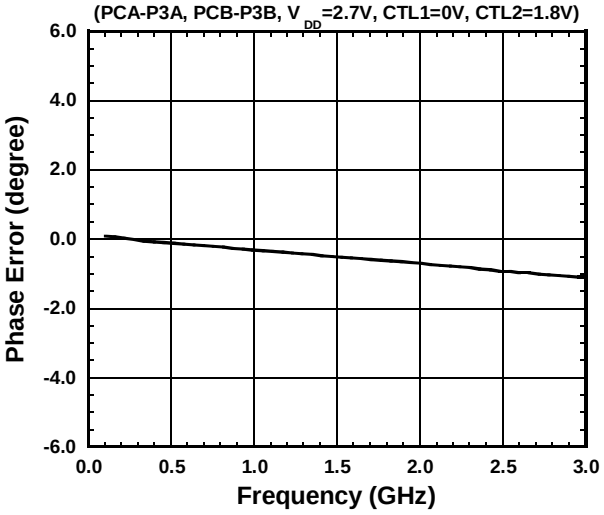
PC-P2 Phase Error vs. Frequency

(PCA-P2A, PCB-P2B, V_{DD}=2.7V, CTL1=0V, CTL2=0V)



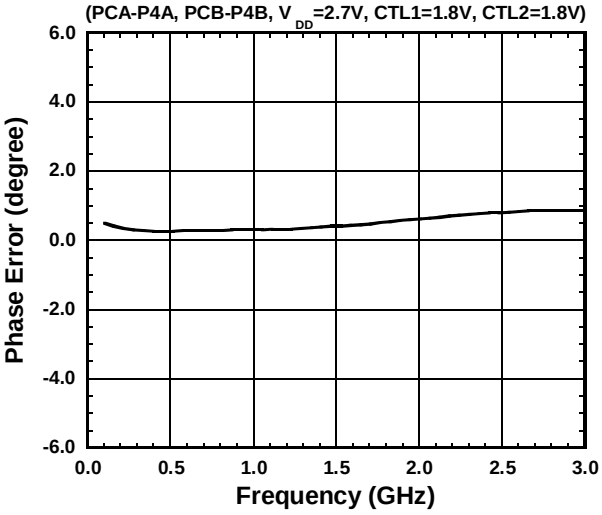
PC-P3 Phase Error vs. Frequency

(PCA-P3A, PCB-P3B, V_{DD}=2.7V, CTL1=0V, CTL2=1.8V)



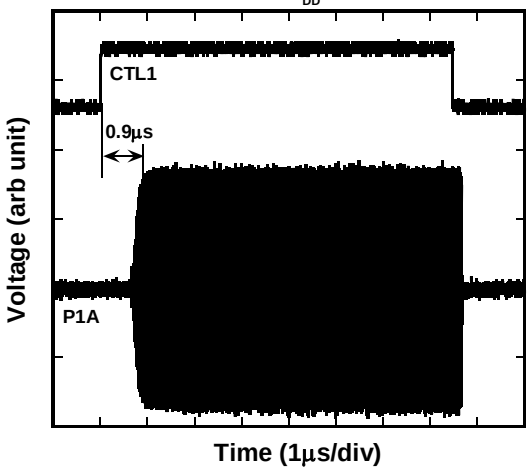
PC-P4 Phase Error vs. Frequency

(PCA-P4A, PCB-P4B, V_{DD}=2.7V, CTL1=1.8V, CTL2=1.8V)



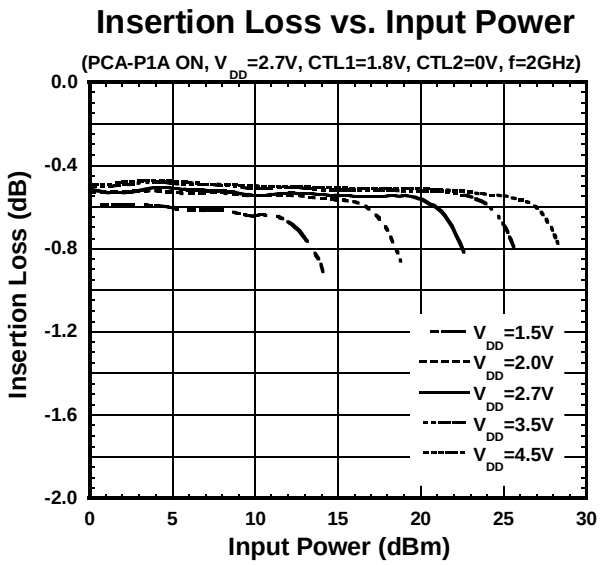
Switching Time

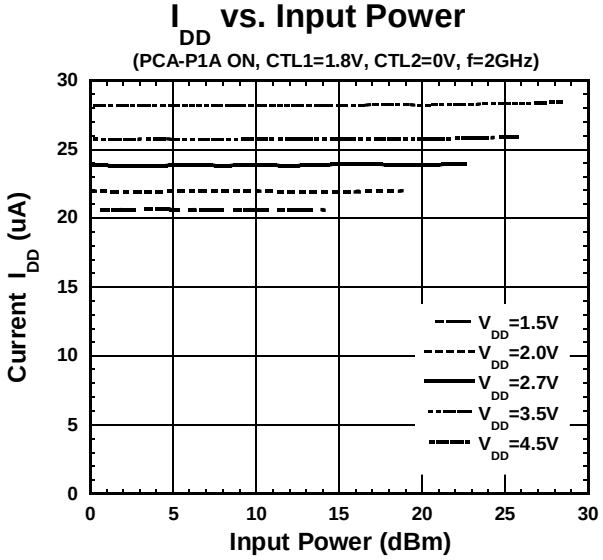
(PCA-P1A/P1B, V_{DD}=2.7V, CTL2=0V)



■ ELECTRICAL CHARACTERISTICS

(General conditions: T_a=+25°C, Z_S=Z_l=50Ω, losses of external circuit are excluded, with application circuit)

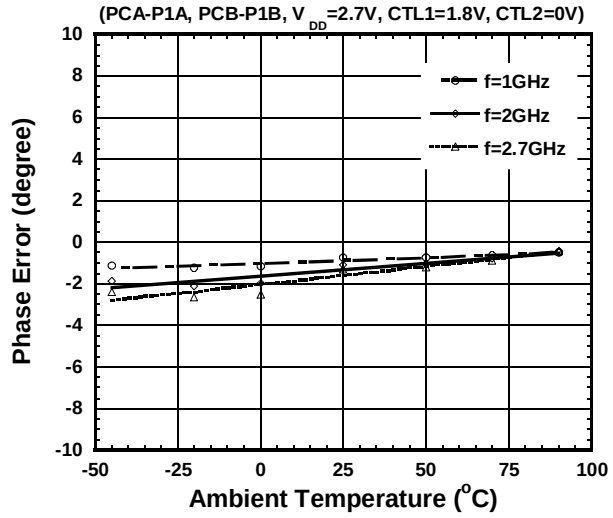




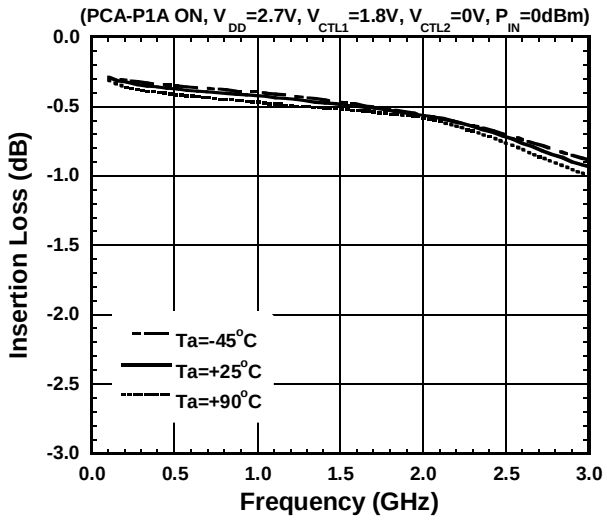
■ ELECTRICAL CHARACTERISTICS

(General conditions: Z_S=Z_I=50Ω, losses of external circuit are excluded, with application circuit)

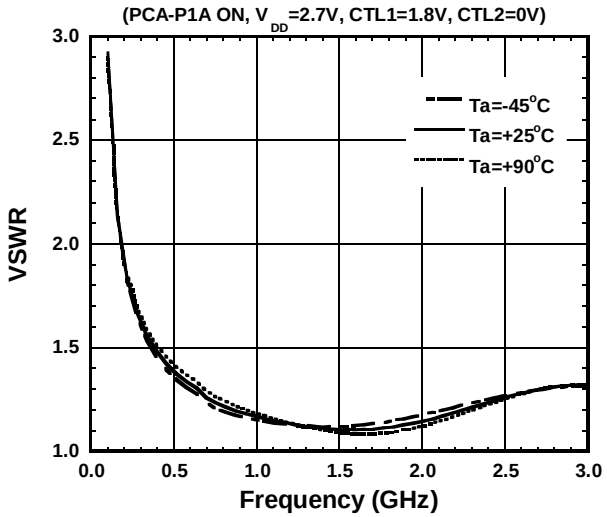
PC-P1 Phase Error vs. Ambient Temperature



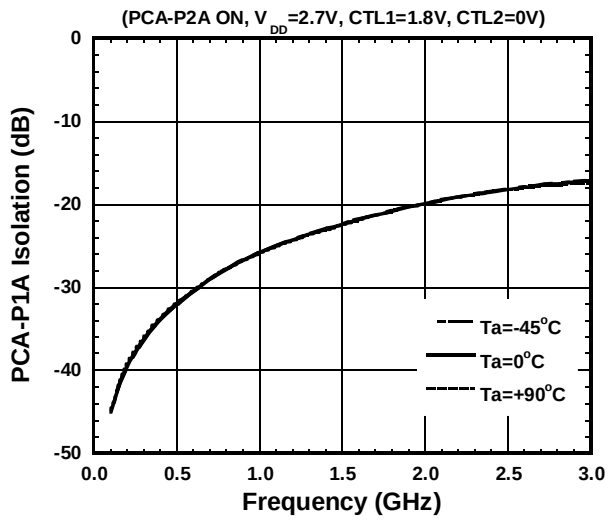
Insertion Loss vs. Frequency



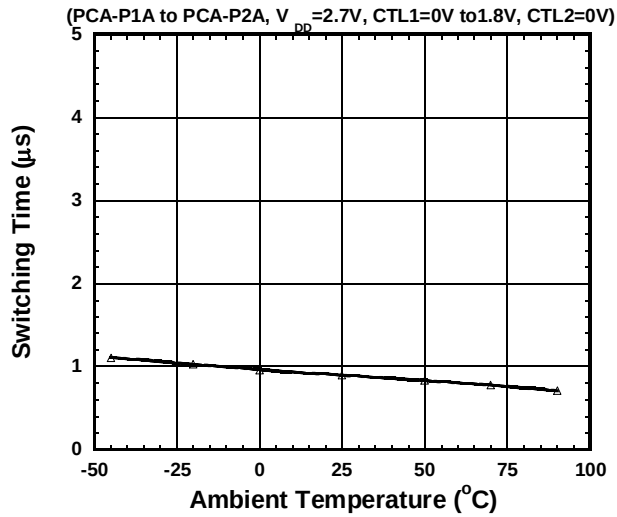
VSWR vs. Frequency



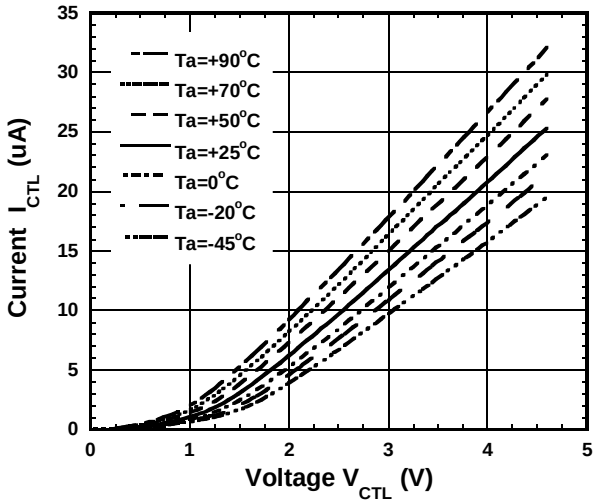
PCA-P1A Isolation vs. Frequency



Switching Time vs. Ambient Temperature

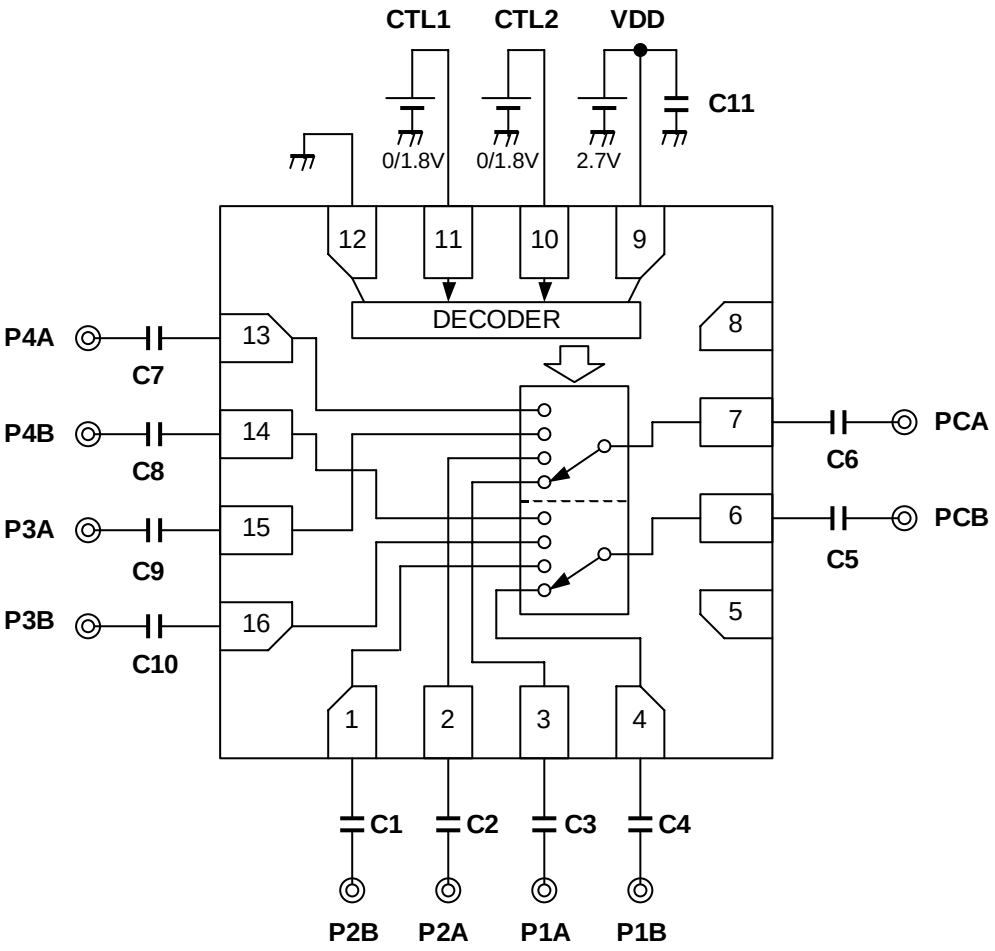


I_{CTL} vs. V_{CTL}



■ APPLICATION CIRCUIT

(Top View)

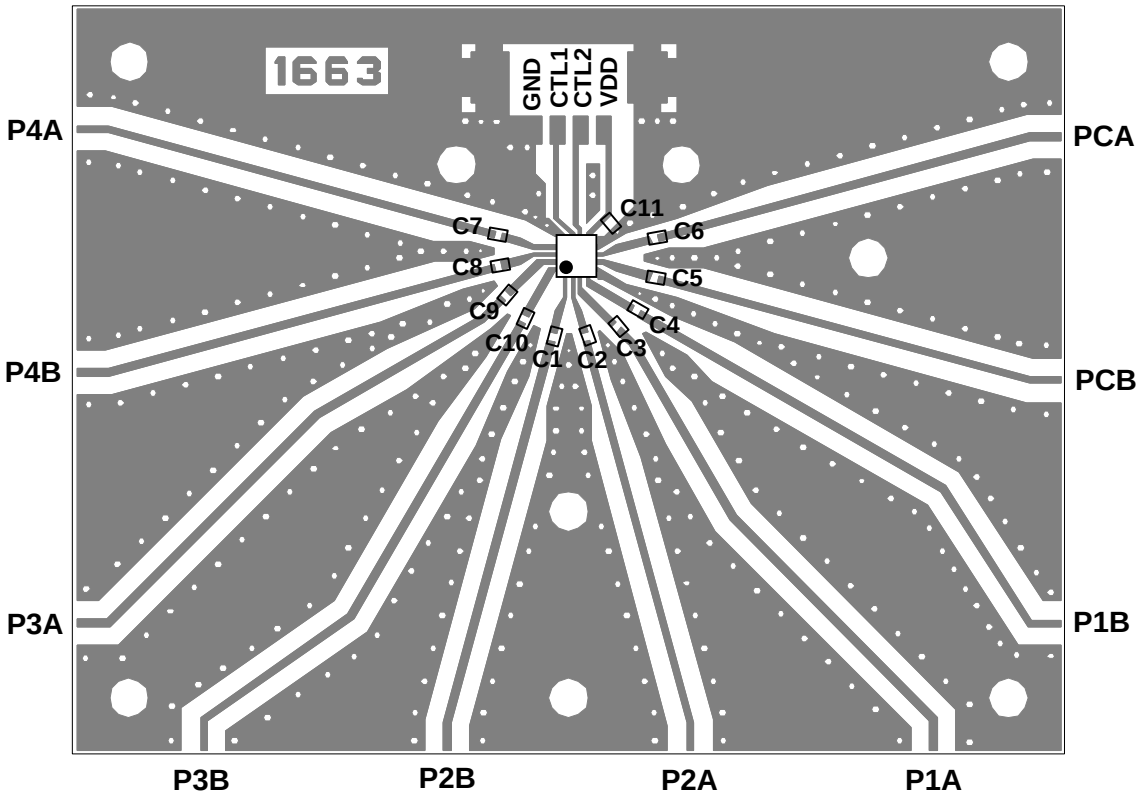


■ PARTS LIST

Part ID	Value	Notes
C1~C10	56pF	MURATA (GRM15)
C11	1000pF	

■ TEST PCB LAYOUT

(TOP VIEW)



PCB: FR-4, t=0.2mm
Capacitor Size: 1005
Strip Line Width: 0.4mm
PCB Size: 53 x 40mm

Losses of PCB, capacitors and connectors

Paths	Frequency (GHz)	Loss (dB)
PCA-P1A, PCB-P1B PCA-P3A, PCB-P3B	1.0	0.49
	2.0	0.79
	2.7	0.98
PCA-P2A, PCB-P2B PCA-P4A, PCB-P4B	1.0	0.45
	2.0	0.77
	2.7	0.95

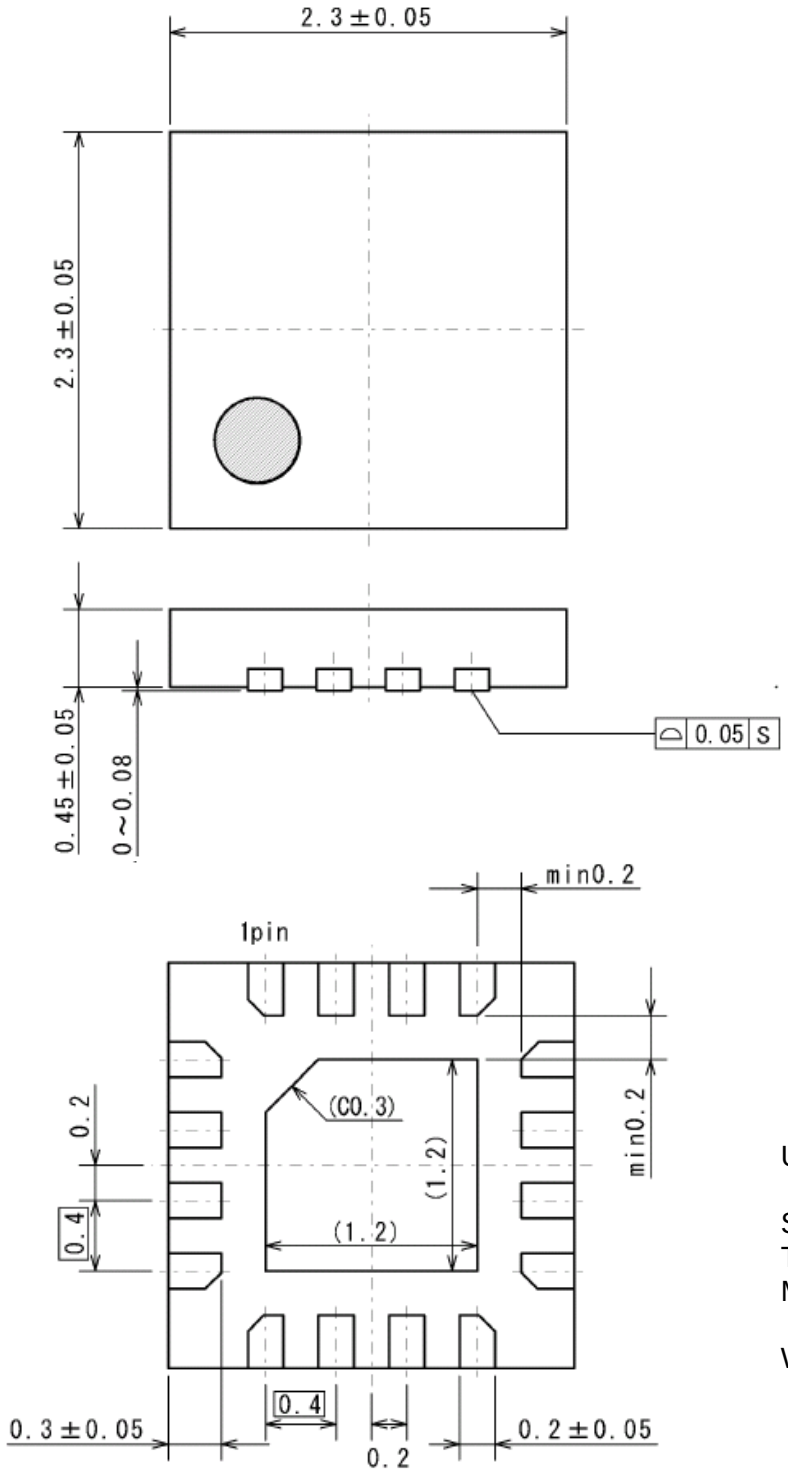
PRECAUTIONS

[1] The DC blocking capacitors (C1~C10) have to be placed at RF terminal of PCA, PCB, P1A, P2A, P3A, P4A, P1B, P2B, P3B, and P4B.

[2] To reduce strip line influence on RF characteristics, please locate bypass capacitor (C11) close to VDD terminal.

[3] For good isolation, the GND terminal must be connected to the ground plane of substrate, and through-holes for GND should be placed near by the pin connection.

■ PACKAGE OUTLINE (QFN16-44)



UNITS	: mm
SUBSTRATE MATERIAL	: Copper
TERMINAL FINISH	: Sn-Bi plating
MOLD MATERIAL	: Epoxy resin (Halogen-free)
WEIGHT	: 7.7mg

Cautions on using this product

This product contains Gallium-Arsenide (GaAs), which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle