

# COMLINEAR<sup>®</sup> CLC2059

## Dual, Low Noise, 4V to 36V Amplifier

### FEATURES

- Unity gain stable
- 110dB voltage gain
- $0.7\mu\text{V}_{\text{RMS}}$  (RIAA)
- 0.0005% THD
- 15MHz gain bandwidth product
- $7\text{V}/\mu\text{s}$  slew rate
- 110dB power supply rejection ratio
- 110dB common mode rejection ratio
- 4V to 36V single supply voltage range
- $\pm 2\text{V}$  to  $\pm 18\text{V}$  dual supply voltage range
- CLC2059: improved replacement for OP275
- CLC2059: Pb-free SOIC-8

### APPLICATIONS

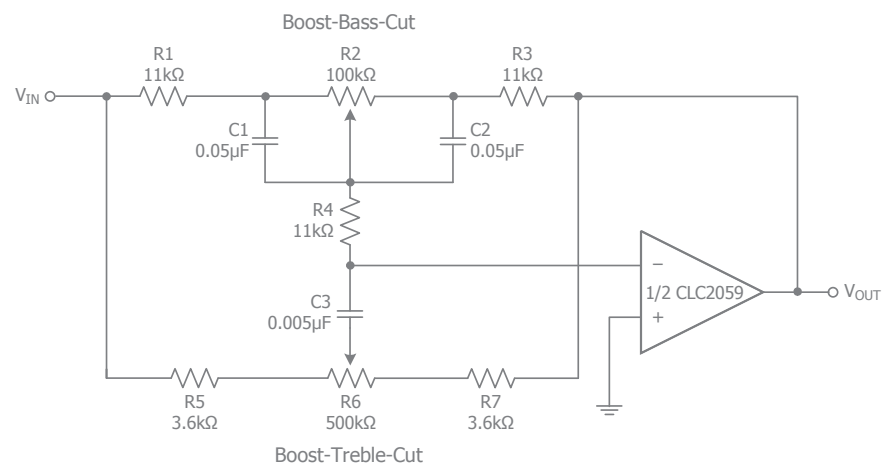
- Active Filters
- Audio Pre-Amplifiers
- Audio AC-3 Decoder Systems
- Headphone Amplifier
- General purpose dual amplifier

### General Description

The COMLINEAR CLC2059 is a low noise, dual voltage feedback amplifier that is internally frequency compensated to provide unity gain stability. The CLC2059 offers 13.7MHz of unity gain bandwidth and excellent (110dB) CMRR, PSRR, and open loop gain. The CLC2059 also features low input voltage noise ( $0.7\mu\text{V}_{\text{RMS}}$ ) and low distortion (0.0005%) making it well suited for audio applications to improve tone control. Other applications include industrial measurement tools, pre-amplifiers, and other circuits that require well-matched channels.

The COMLINEAR CLC2059 is designed to operate over a wide power supply voltage range,  $\pm 2\text{V}$  to  $\pm 18\text{V}$  (4V to 36V). It utilizes an industry standard dual amplifier pin-out and is available in a Pb-free, RoHS compliant SOIC-8 package.

### Typical Application - Audio Tone Control Circuit



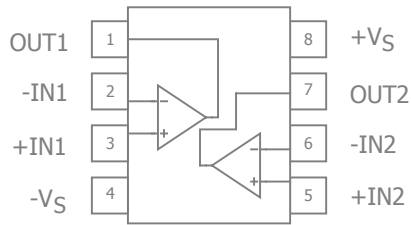
### Ordering Information

Part Number	Package	Pb-Free	RoHS Compliant	Operating Temperature Range	Packaging Method
CLC2059ISO8X	SOIC-8	Yes	Yes	-40°C to +85°C	Reel

Moisture sensitivity level for all parts is MSL-1.



## CLC2059 Pin Configuration



## CLC2059 Pin Description

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	-VS	Negative supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	+VS	Positive supply



## Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
Supply Voltage	0	40 ( $\pm 20$ )	V
Differential Input Voltage		60 ( $\pm 30$ )	V
Input Voltage		30 ( $\pm 15$ )	V
Power Dissipation ( $T_A = 25^\circ\text{C}$ ) - SOIC-8		500	mW

## Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			150	$^\circ\text{C}$
Storage Temperature Range	-65		150	$^\circ\text{C}$
Lead Temperature (Soldering, 10s)			260	$^\circ\text{C}$
Package Thermal Resistance				
SOIC-8		100		$^\circ\text{C}/\text{W}$

Notes:

Package thermal resistance ( $\theta_{JA}$ ), JEDEC standard, multi-layer test boards, still air.

## Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	$^\circ\text{C}$
Supply Voltage Range	4 ( $\pm 2$ )		36 ( $\pm 18$ )	V



## Electrical Characteristics

$T_A = 25^\circ\text{C}$ ,  $+V_S = +15\text{V}$ ,  $-V_S = -15\text{V}$ ,  $R_f = R_g = 2\text{k}\Omega$ ,  $R_L = 2\text{k}\Omega$  to  $V_S/2$ ,  $G = 2$ ; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
UGBW <sub>SS</sub>	Unity Gain Bandwidth	$G = +1$ , $V_{OUT} = 0.2V_{pp}$ , $V_S = 5\text{V}$ , $R_f = 0$		11.7		MHz
		$G = +1$ , $V_{OUT} = 0.2V_{pp}$ , $V_S = 30\text{V}$ , $R_f = 0$		13.7		MHz
BW <sub>SS</sub>	-3dB Bandwidth	$G = +2$ , $V_{OUT} = 0.2V_{pp}$ , $V_S = 5\text{V}$		6.3		MHz
		$G = +1$ , $V_{OUT} = 0.2V_{pp}$ , $V_S = 30\text{V}$		6.8		MHz
BW <sub>LS</sub>	Large Signal Bandwidth	$G = +2$ , $V_{OUT} = 1V_{pp}$ , $V_S = 5\text{V}$		2.8		MHz
		$G = +2$ , $V_{OUT} = 2V_{pp}$ , $V_S = 30\text{V}$		1.7		MHz
GBWP	Gain-Bandwidth Product			15		MHz
Time Domain Response						
$t_R$ , $t_F$	Rise and Fall Time	$V_{OUT} = 0.2\text{V}$ step; (10% to 90%), $V_S = 5\text{V}$		50		ns
		$V_{OUT} = 0.2\text{V}$ step; (10% to 90%), $V_S = 30\text{V}$		47		ns
OS	Overshoot	$V_{OUT} = 0.2\text{V}$ step		16		%
		$V_{OUT} = 2\text{V}$ step		5		%
SR	Slew Rate	2V step, $V_S = 5\text{V}$		6		V/ $\mu\text{s}$
		4V step, $V_S = 30\text{V}$		7		V/ $\mu\text{s}$
Distortion/Noise Response						
THD	Total Harmonic Distortion	$V_{OUT} = 5\text{V}$ , $f = 1\text{kHz}$ , $G = 20\text{dB}$		0.0005		%
$e_n$	Input Voltage Noise	> 1kHz		4		nV/ $\sqrt{\text{Hz}}$
		RIAA, 30kHz LPF, $R_S = 50\Omega$		0.7		$\mu\text{V}_{\text{RMS}}$
$X_{\text{TALK}}$	Crosstalk	Channel-to-channel, 500kHz, $V_S = 5\text{V}$ to 30V		67		dB
DC Performance						
$V_{IO}$	Input Offset Voltage <sup>(1)</sup>	$R_S \leq 10\text{k}\Omega$		0.5	3	mV
$I_b$	Input Bias Current <sup>(1)</sup>	$V_{CM} = 0\text{V}$		150	500	nA
$I_{OS}$	Input Offset Current <sup>(1)</sup>	$V_{CM} = 0\text{V}$		5	100	nA
PSRR	Power Supply Rejection Ratio <sup>(1)</sup>	$R_S \leq 10\text{k}\Omega$	80	110		dB
$A_{OL}$	Open-Loop Gain <sup>(1)</sup>	$R_L = \geq 2\text{k}\Omega$ , $V_{OUT} = \pm 10\text{V}$	90	110		dB
$I_S$	Supply Current <sup>(1)</sup>	Total, $R_L = \infty$		3	7	mA
Input Characteristics						
CMIR	Common Mode Input Range <sup>(1)</sup>	$+V_S = 15\text{V}$ , $-V_S = -15\text{V}$	$\pm 12$	$\pm 13.5$		V
CMRR	Common Mode Rejection Ratio <sup>(1)</sup>	DC, $V_{CM} = 0\text{V}$ to $+V_S - 1.5\text{V}$ , $R_S \leq 10\text{k}\Omega$	80	110		dB
Output Characteristics						
$V_{OUT}$	Output Voltage Swing	$R_L = 2\text{k}\Omega$		+13.8, -13.0		V
		$R_L = 10\text{k}\Omega$		$\pm 14.0$ , -13.3		V
$I_{\text{SOURCE}}$	Output Current, Sourcing	$V_{IN+} = 1\text{V}$ , $V_{IN-} = 0\text{V}$ , $V_{OUT} = 2\text{V}$		45		mA
$I_{\text{SINK}}$	Output Current, Sinking	$V_{IN+} = 0\text{V}$ , $V_{IN-} = 1\text{V}$ , $V_{OUT} = 2\text{V}$		80		mA

### Notes:

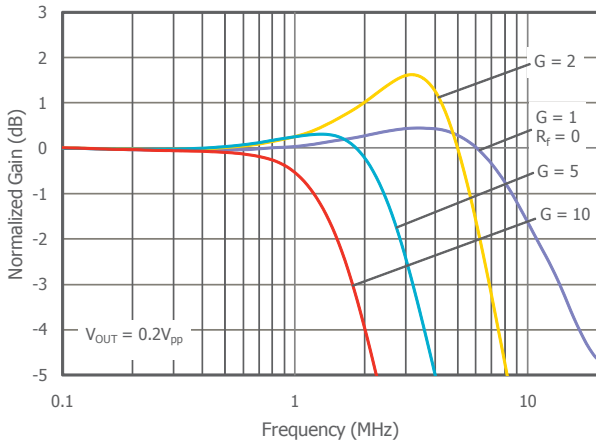
- 100% tested at  $25^\circ\text{C}$  at  $V_S = \pm 15\text{V}$ .



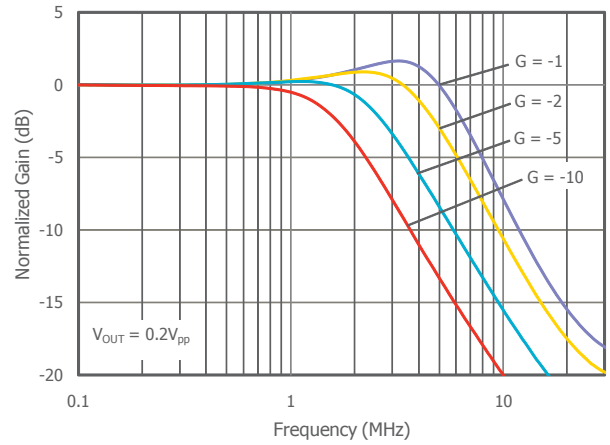
### Typical Performance Characteristics

$T_A = 25^\circ\text{C}$ ,  $+V_S = +15\text{V}$ ,  $-V_S = -15\text{V}$ ,  $R_f = R_g = 2\text{k}\Omega$ ,  $R_L = 2\text{k}\Omega$  to  $V_S/2$ ,  $G = 2$ ; unless otherwise noted.

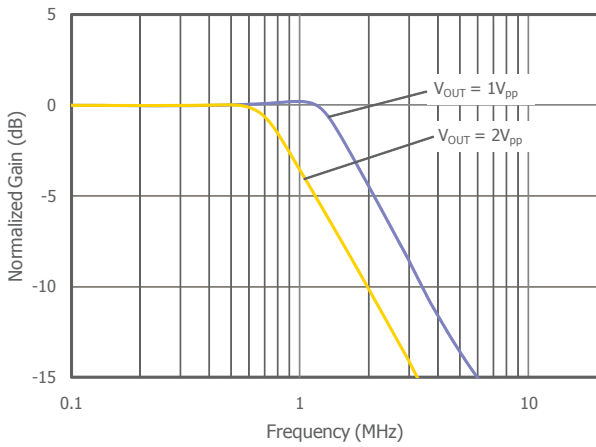
#### Non-Inverting Frequency Response



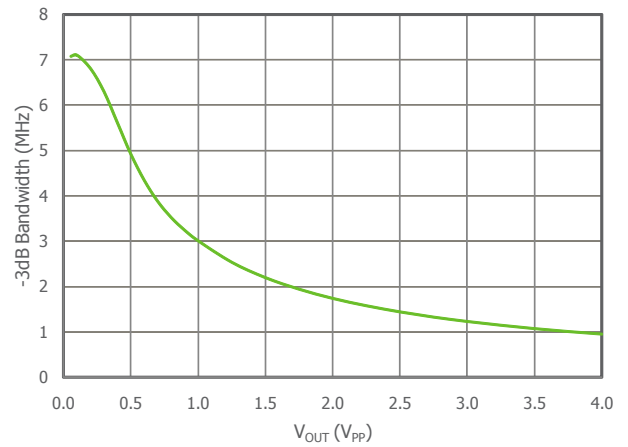
#### Inverting Frequency Response



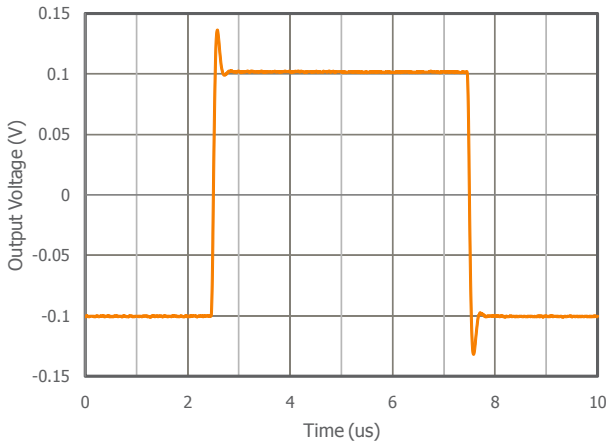
#### Large Signal Frequency Response



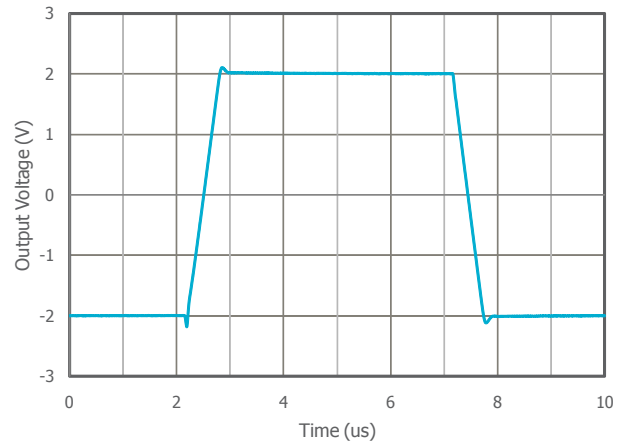
#### -3dB Bandwidth vs. $V_{OUT}$



#### Small Signal Pulse Response



#### Large Signal Pulse Response

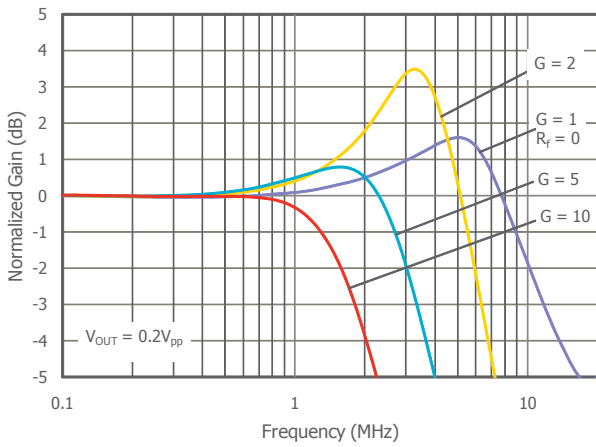




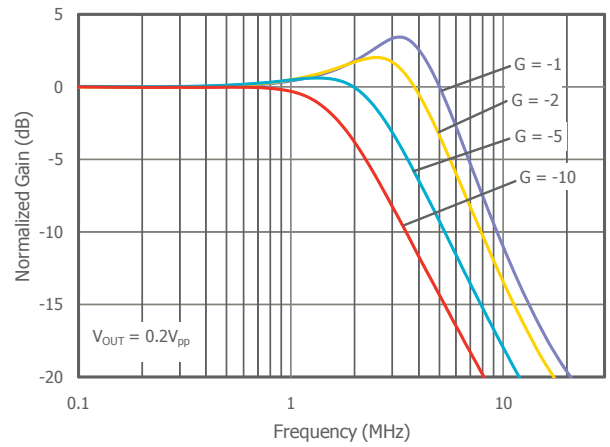
## Typical Performance Characteristics

$T_A = 25^\circ\text{C}$ ,  $+V_S = +5\text{V}$ ,  $-V_S = \text{GND}$ ,  $R_f = R_g = 2\text{k}\Omega$ ,  $R_L = 2\text{k}\Omega$  to  $V_S/2$ ,  $G = 2$ ; unless otherwise noted.

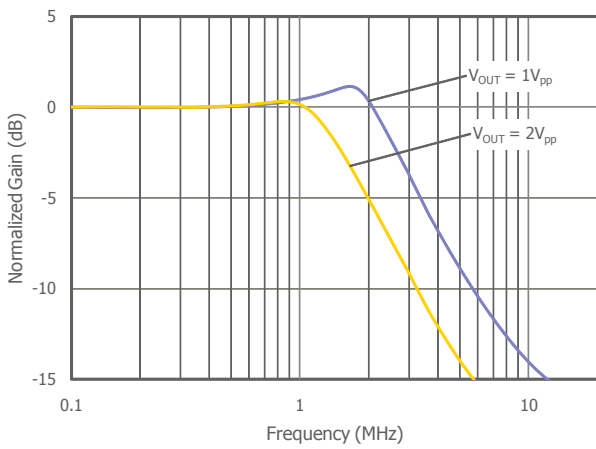
Non-Inverting Frequency Response



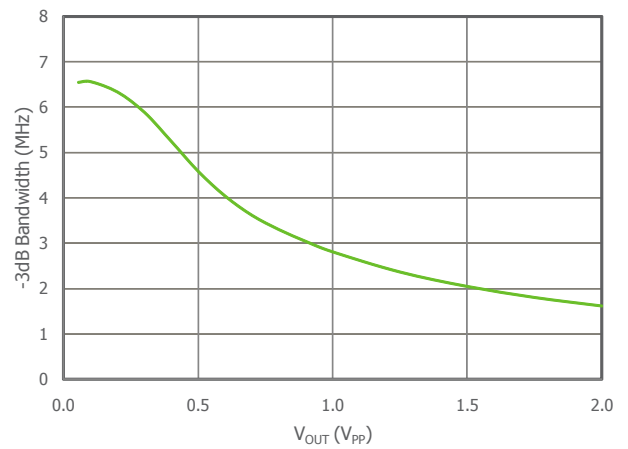
Inverting Frequency Response



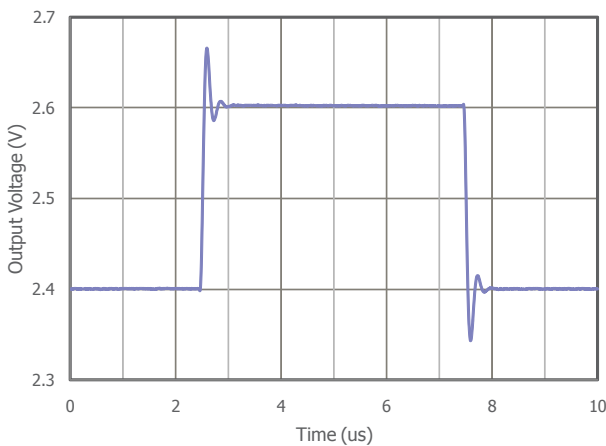
Large Signal Frequency Response



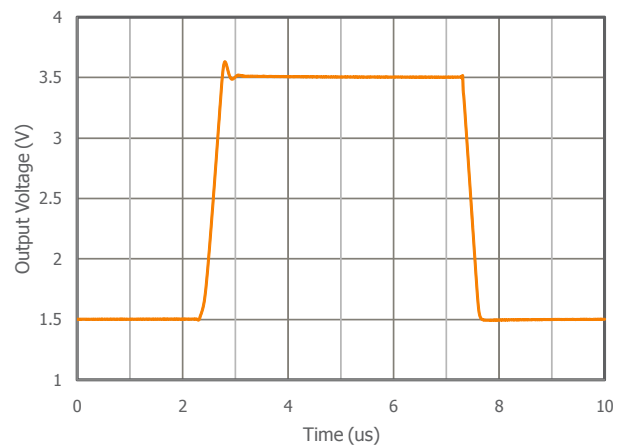
-3dB Bandwidth vs.  $V_{OUT}$



Small Signal Pulse Response



Large Signal Pulse Response

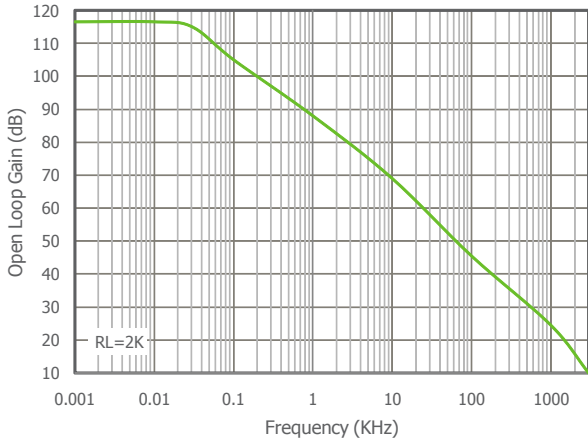




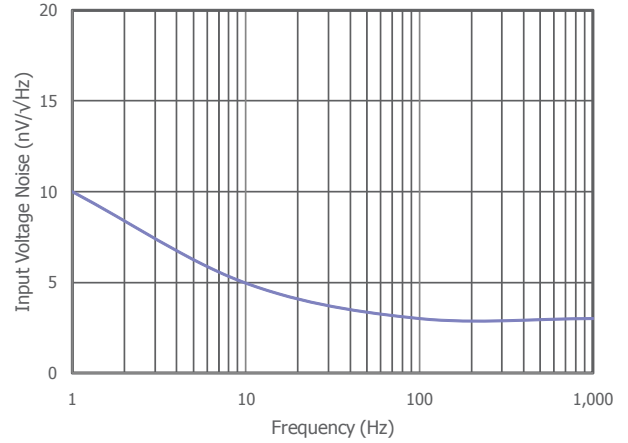
### Typical Performance Characteristics

$T_A = 25^\circ\text{C}$ ,  $+V_S = +15\text{V}$ ,  $-V_S = -15\text{V}$ ,  $R_f = R_g = 2\text{k}\Omega$ ,  $R_L = 2\text{k}\Omega$  to  $V_S/2$ ,  $G = 2$ ; unless otherwise noted.

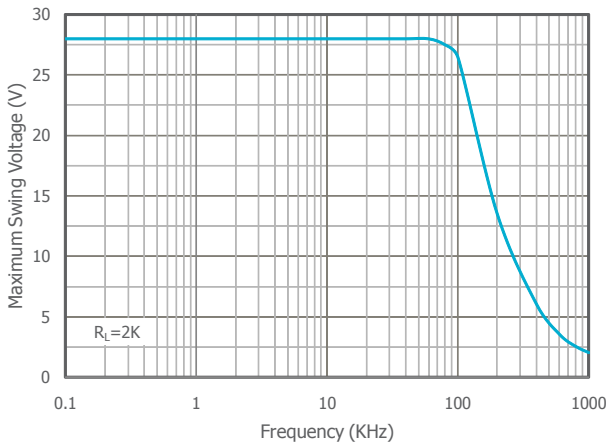
Open Loop Voltage Gain vs. Frequency



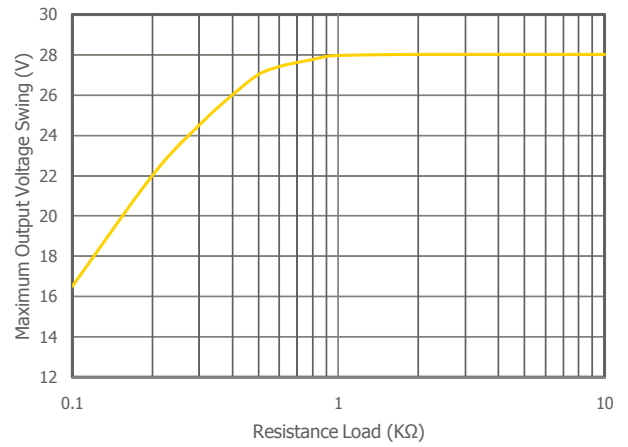
Input Voltage Noise vs. Frequency



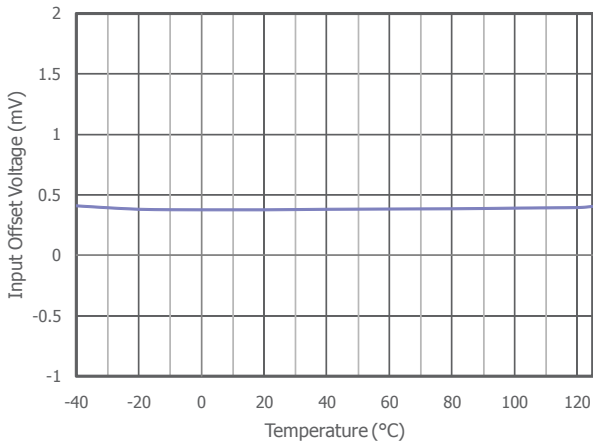
Maximum Output Voltage Swing vs. Frequency



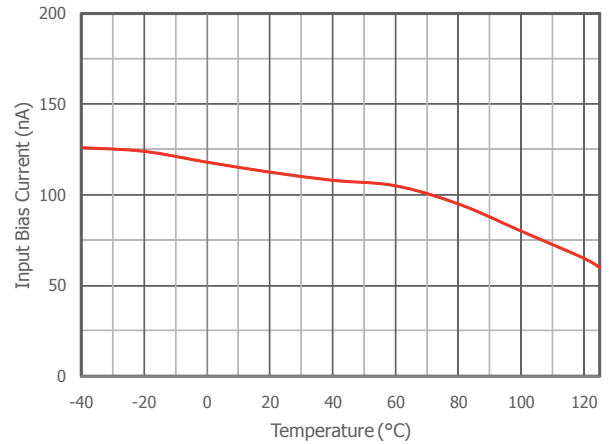
Maximum Output Voltage Swing vs.  $R_L$



Input Offset Voltage vs. Temperature



Input Bias Current vs. Temperature

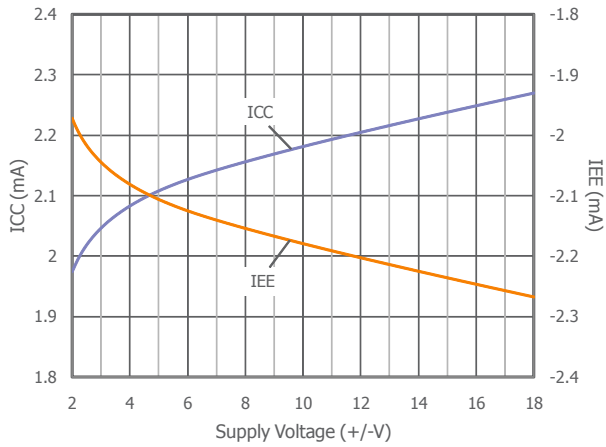




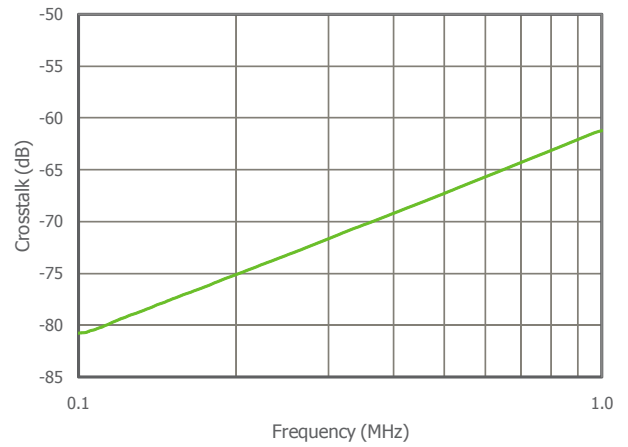
## Typical Performance Characteristics

$T_A = 25^\circ\text{C}$ ,  $+V_S = +15\text{V}$ ,  $-V_S = -15\text{V}$ ,  $R_f = R_g = 2\text{k}\Omega$ ,  $R_L = 2\text{k}\Omega$  to  $V_S/2$ ,  $G = 2$ ; unless otherwise noted.

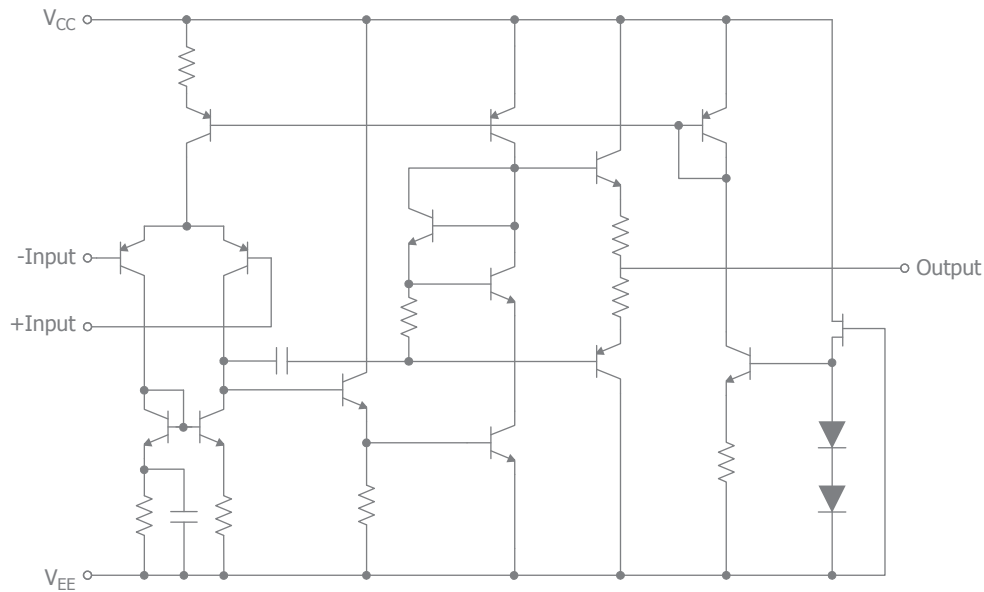
Supply Voltage vs. Supply Current



Crosstalk vs. Frequency



Functional Block Diagram







## Application Information

### Basic Operation

Figures 1 and 2 illustrate typical circuit configurations for non-inverting, inverting, and unity gain topologies for dual supply applications. They show the recommended bypass capacitor values and overall closed loop gain equations.

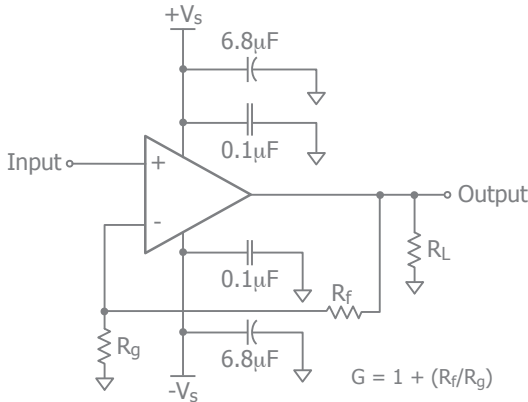


Figure 1. Typical Non-Inverting Gain Circuit

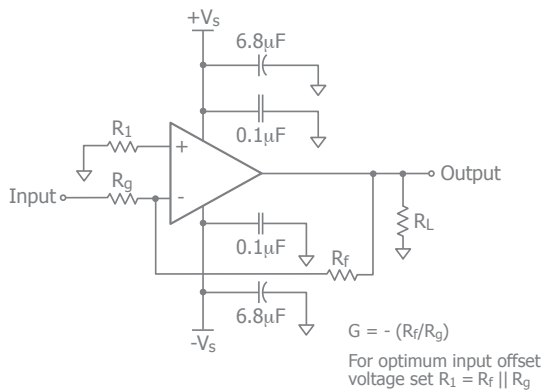


Figure 2. Typical Inverting Gain Circuit

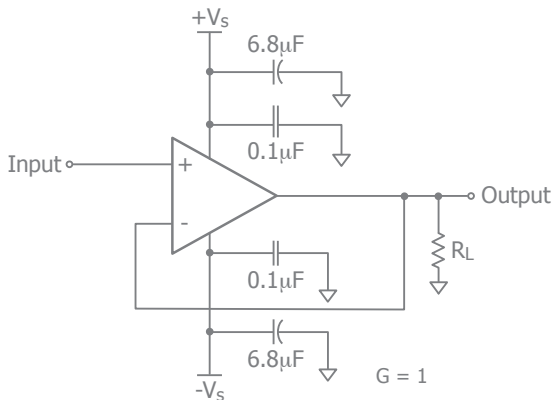


Figure 3. Unity Gain Circuit

### Power Dissipation

Power dissipation should not be a factor when operating under the stated 2k ohm load condition. However, applications with low impedance, DC coupled loads should be analyzed to ensure that maximum allowed junction temperature is not exceeded. Guidelines listed below can be used to verify that the particular application will not cause the device to operate beyond its intended operating range.

Maximum power levels are set by the absolute maximum junction rating of 150°C. To calculate the junction temperature, the package thermal resistance value  $\Theta_{JA}$  ( $\Theta_{JA}$ ) is used along with the total die power dissipation.

$$T_{\text{Junction}} = T_{\text{Ambient}} + (\Theta_{JA} \times P_D)$$

Where  $T_{\text{Ambient}}$  is the temperature of the working environment.

In order to determine  $P_D$ , the power dissipated in the load needs to be subtracted from the total power delivered by the supplies.

$$P_D = P_{\text{supply}} - P_{\text{load}}$$

Supply power is calculated by the standard power equation.

$$P_{\text{supply}} = V_{\text{supply}} \times I_{\text{RMS supply}}$$

$$V_{\text{supply}} = V_{S+} - V_{S-}$$

Power delivered to a purely resistive load is:

$$P_{\text{load}} = ((V_{\text{LOAD}})_{\text{RMS}}^2) / R_{\text{load eff}}$$

The effective load resistor ( $R_{\text{load eff}}$ ) will need to include the effect of the feedback network. For instance,

$R_{\text{load eff}}$  in figure 3 would be calculated as:

$$R_L \parallel (R_f + R_g)$$

These measurements are basic and are relatively easy to perform with standard lab equipment. For design purposes however, prior knowledge of actual signal levels and load impedance is needed to determine the dissipated power. Here,  $P_D$  can be found from

$$P_D = P_{\text{Quiescent}} + P_{\text{Dynamic}} - P_{\text{Load}}$$

Quiescent power can be derived from the specified  $I_S$  values along with known supply voltage,  $V_{\text{Supply}}$ . Load power



can be calculated as above with the desired signal amplitudes using:

$$(V_{LOAD})_{RMS} = V_{PEAK} / \sqrt{2}$$

$$(I_{LOAD})_{RMS} = (V_{LOAD})_{RMS} / R_{load_{eff}}$$

The dynamic power is focused primarily within the output stage driving the load. This value can be calculated as:

$$P_{DYNAMIC} = (V_{S+} - V_{LOAD})_{RMS} \times (I_{LOAD})_{RMS}$$

Assuming the load is referenced in the middle of the power rails or  $V_{supply}/2$ .

Figure 4 shows the maximum safe power dissipation in the package vs. the ambient temperature for the packages available.

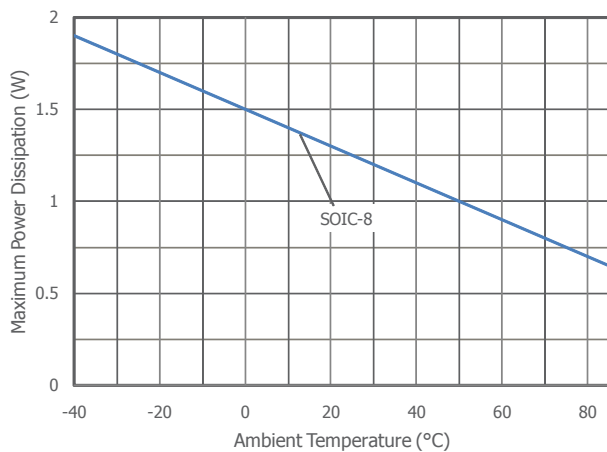


Figure 4. Maximum Power Derating

### Driving Capacitive Loads

Increased phase delay at the output due to capacitive loading can cause ringing, peaking in the frequency response, and possible unstable behavior. Use a series resistance,  $R_S$ , between the amplifier and the load to help improve stability and settling performance. Refer to Figure 5.

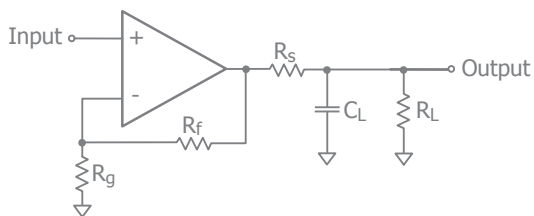


Figure 5. Addition of  $R_S$  for Driving Capacitive Loads

### Overdrive Recovery

An overdrive condition is defined as the point when either one of the inputs or the output exceed their specified voltage range. Overdrive recovery is the time needed for the amplifier to return to its normal or linear operating point. The recovery time varies, based on whether the input or output is overdriven and by how much the range is exceeded. The CLC2059 will typically recover in less than  $5\mu s$  from an overdrive condition. Figure 6 shows the CLC2059 in an overdriven condition.

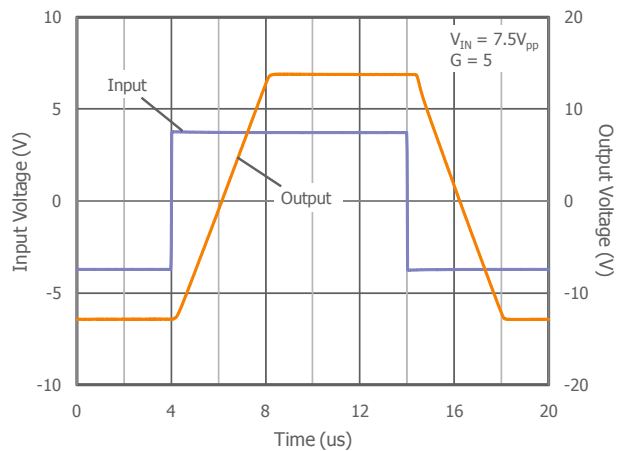


Figure 6. Overdrive Recovery

### Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. CADEKA has evaluation boards to use as a guide for high frequency layout and as an aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8 $\mu F$  and 0.1 $\mu F$  ceramic capacitors for power supply decoupling
- Place the 6.8 $\mu F$  capacitor within 0.75 inches of the power pin
- Place the 0.1 $\mu F$  capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.



### Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

Evaluation Board	Products
CEB006	CLC2059

### Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 7-9. These evaluation boards are built for dual-supply operation. Follow these steps to use the board in a single-supply application:

1. Short  $-V_s$  to ground.
2. Use C3 and C4, if the  $-V_s$  pin of the amplifier is not directly connected to the ground plane.

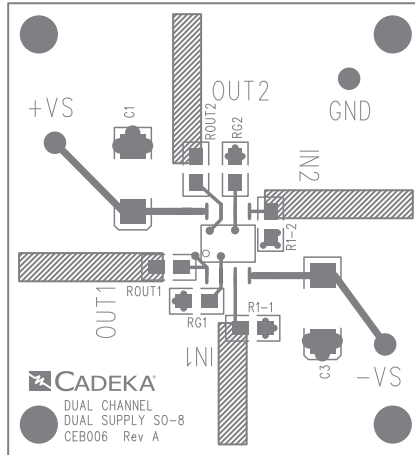


Figure 8. CEB006 Top View

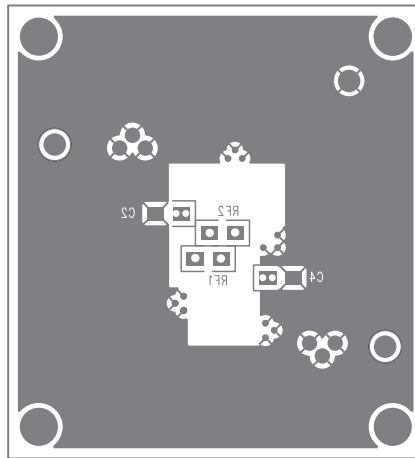


Figure 9. CEB006 Bottom View

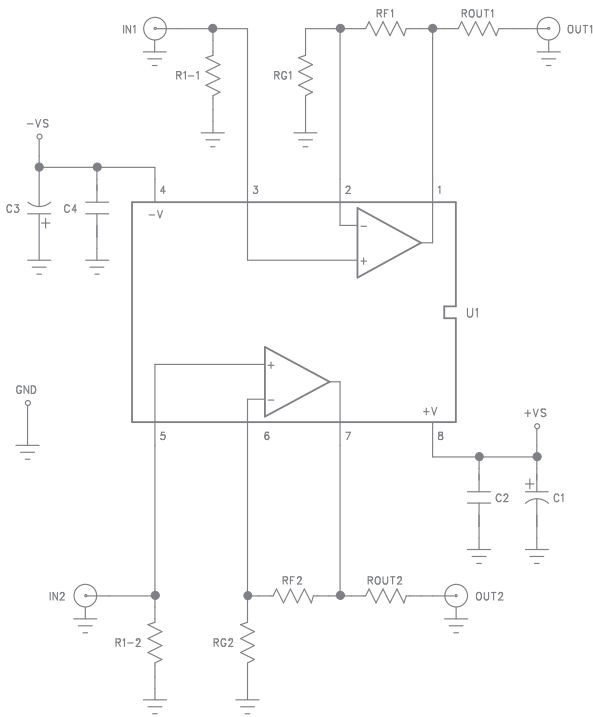


Figure 7. CEB006 Schematic



Typical Applications

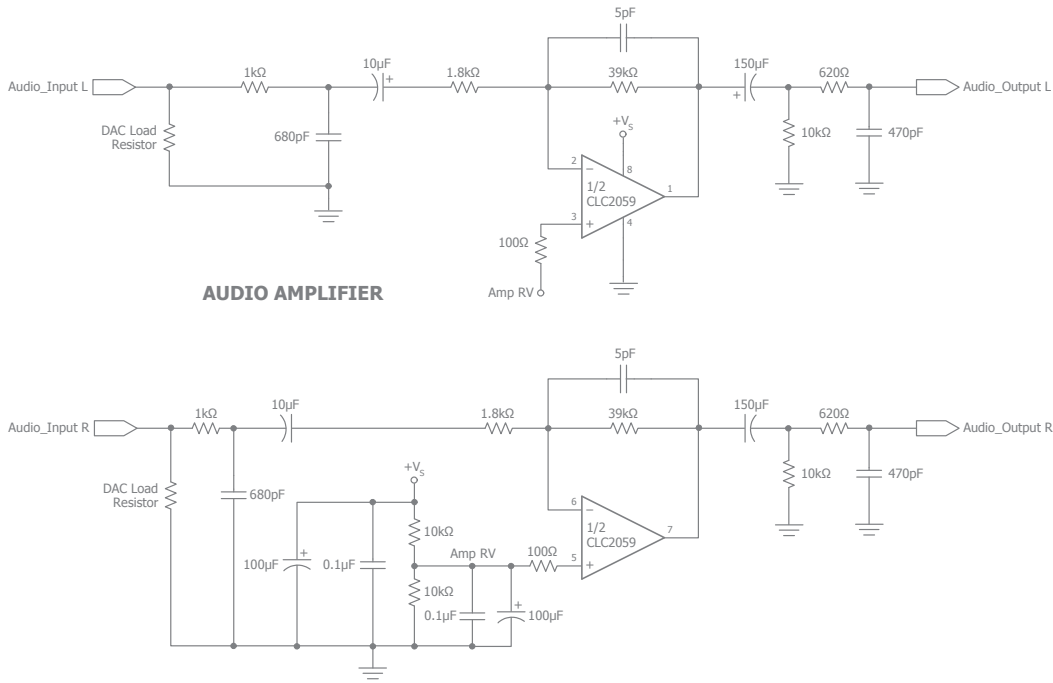


Figure 10: Typical Circuit for Filtering and Driving Audio in STB or DVD Player Applications

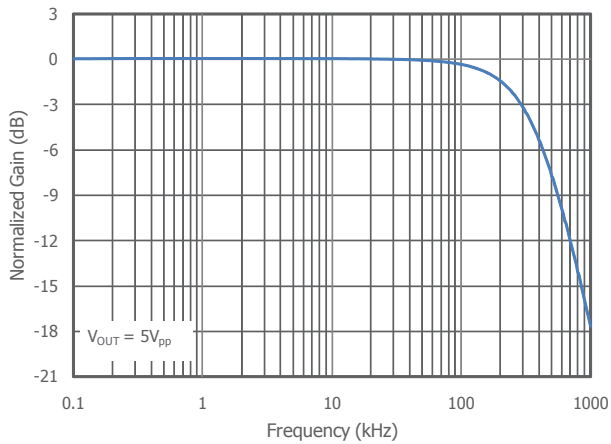


Figure 11: AC Reponse of Figure 10 ( $V_S=10V$ ,  $R_L=630\Omega$ )

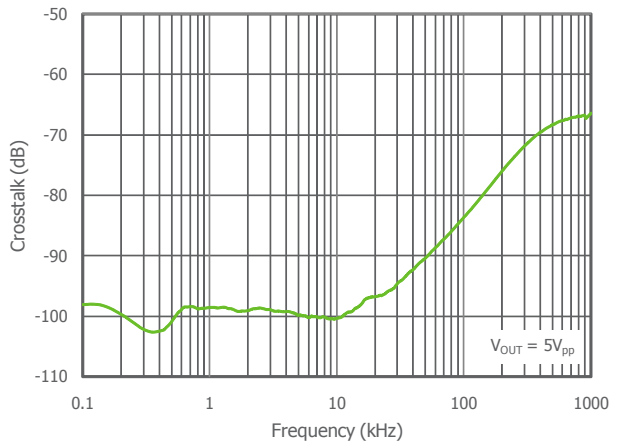
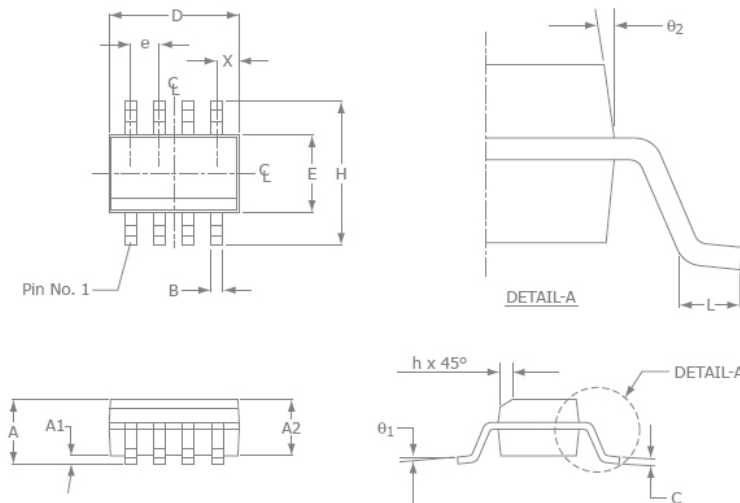


Figure 12: Cross-Talk Performance of Figure 10 ( $V_S=10V$ ,  $R_L=630\Omega$ )



## Mechanical Dimensions

### SOIC-8 Package



SOIC-8		
SYMBOL	MIN	MAX
A1	0.10	0.25
B	0.36	0.48
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.5
L	0.41	1.27
A	1.37	1.73
$\theta_1$	0°	8°
X	0.55 ref	
$\theta_2$	7° BSC	

#### NOTE:

1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.1mm (0.004") max.
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.1905mm from the lead tip.

For additional information regarding our products, please visit CADEKA at: [cadeka.com](http://cadeka.com)

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