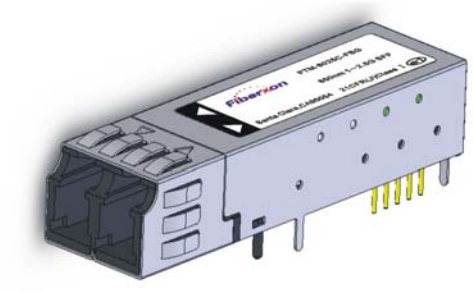
1~2.5Gbps 850nm SFF 2×5 Transceiver

(For 300m transmission at 2.125Gbps)

Members of Flexon™ Family



Features

- Multi-rate 1~2.5Gbps bi-directional data links
- Up to 300m transmission distance at 2.125Gbps
- Up to 550m transmission distance at 1.0625/1.25Gbps
- 850nm VCSEL transmitter
- SFF 2×5 package
- Duplex LC optical interface
- Low power dissipation
- Class I laser product
- Low EMI and excellent ESD protection
- Single +3.3V power supply
- Operating ambient temperature: 0 to +70°C

Applications

- 1.25Gbps 1000Base-SX Ethernet
- Dual Rate 1.0625/2.125Gbps Fibre Channel
- Mass storage system I/O
- Computer system I/O
- Host adapter I/O

Standard

- Compatible with SFF MSA 2000 version
- Compatible with ANSI specifications for Fibre Channel
- Compatible with IEEE 802.3
- Compatible with FCC 47 CFR Part 15, Class B
- Compatible with FDA 21 CFR 1040.10 and 1040.11, Class I
- Compliant with RoHS

Description

FTM-8025C-FBG is compatible with the specifications set forth in the SFF MSA. It is designed for use in Fibre Channel applications both at 1.0625Gbps and 2.125Gbps. The transceiver also meets the requirements of IEEE 802.3 Gigabit Ethernet (1000BASE-SX) standard.

FTM-8025C-FBG incorporates a highly reliable 850nm VCSEL laser in its transmitter section. And the receiver section consists of a PIN photodiode integrated with a trans-impedance preamplifier (TIA). All modules satisfy class I laser safety requirements.

FTM-8025C-FBG is Compliant with RoHS.

Regulatory Compliance

The transceivers have been tested according to American and European product safety and electromagnetic compatibility regulations (See Table 1). For further information regarding regulatory certification, please refer to Flexon™ regulatory specification and safety guidelines, or contact with Fiberxon, Inc. America sales office listed at the end of documentation.

Table 1 - Regulatory Compliance

Feature	Standard	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883E Method 3015.7	Class 1(>500 V)
Electrostatic Discharge (ESD) to the Duplex LC Receptacle	IEC 61000-4-2 GR-1089-CORE	Compatible with standards
Electromagnetic Interference (EMI)	FCC Part 15 Class B EN55022 Class B (CISPR 22B) VCCI Class B	Compatible with standards
Immunity	IEC 61000-4-3	Compatible with standards
Laser Eye Safety	FDA 21CFR 1040.10 and 1040.11 EN60950, EN (IEC) 60825-1,2	Compatible with Class I laser product.
Component Recognition	UL and CSA	Compatible with standards

Absolute Maximum Ratings

Stress in excess of the maximum absolute ratings can cause permanent damage to the module.

Table 2 - Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	+85	°C
Supply Voltage	V_{CC}	-0.5	3.6	V
Operating Relative Humidity	-	5	95	%

Recommended Operating Conditions

Table 3- Recommended Operating Conditions

Parameter		Symbol	Min.	Typical	Max.	Unit
Operating Ambient Temperature		T_A	0		+70	°C
Power Supply Voltage		V_{CC}	3.13		3.47	V
Power Supply Current		I_{CC}		130	240	mA
Data Rate			1.0625	2.125	2.5	Gbps
Fiber Length on 50/125μm MMF	1.0625/1.25Gbps	L			550	m
	2.125Gbps				300	

Fiber Length on 62.5/125μm MMF	1.0625/1.25Gbps	L			300	m
	2.125Gbps				150	

Optical and Electrical Characteristics

Table 4 - Optical and Electrical Characteristics

Parameter		Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter							
Centre Wavelength		λ_C	830	850	860	nm	
Spectral Width (RMS)		σ			0.85	nm	
Average Output Power		P_{0ut}	-9.5		-4	dBm	1
P_{0ut}@TX Disable Asserted		P_{0ut}			-40	dBm	1
Extinction Ratio		EX	9			dB	
Rise/Fall Time (20%～80%)	1.0625/1.25Gbps	t_r/t_f			260	ps	2
	2.125Gbps				150		
Total Jitter	1.0625Gbps	T_J			0.43	UI	3
	1.25Gbps				0.43		
	2.125Gbps				0.44		
Deterministic Jitter	1.0625Gbps	D_J			0.21	UI	3
	1.25Gbps				0.20		
	2.125Gbps				0.26		
Output Optical Eye		ANSI Fibre Channel and Gigabit Ethernet Compatible					
Data Input Swing Differential		V_{IN}	370		2000	mV	4
Input Differential Impedance		Z_{IN}	90	100	110	Ω	
TX Disable	Disable		2.0		Vcc	V	
	Enable		0		0.8	V	
Receiver							
Centre Wavelength		λ_C	770		860	nm	
Receiver Sensitivity	1.0625/1.25Gbps	P_{IN}			-18	dBm	5
	2.125Gbps				-17		
Receiver Overload		P_{IN}	0			dBm	5
Return Loss			12			dB	
SD Assert		SD_A			-18	dBm	
SD De-Assert		SD_D	-30			dBm	
SD Hysteresis			0.5		4	dB	
Total Jitter (pk-pk)	1.0625Gbps	T_J			0.61	UI	3
	1.25Gbps				0.749		
	2.125Gbps				0.64		
Deterministic Jitter (pk-pk)	1.0625Gbps	D_J			0.36	UI	3
	1.25Gbps				0.462		
	2.125Gbps				0.39		

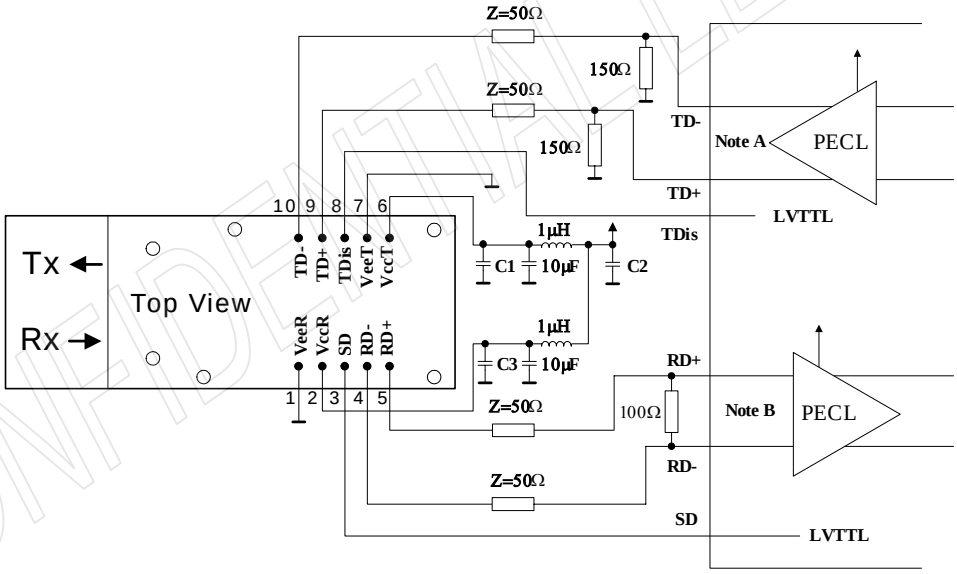
Data Output Swing Differential		V_{OUT}	370		2000	mV	4
SD	High		2.0		Vcc	V	
	Low		0		0.8	V	

Notes:

1. The optical power is launched into MMF.
2. Unfiltered, measured with a PRBS 2^7-1 test pattern
3. Measured with a PRBS 2^7-1 test pattern, meet the specified maximum output jitter requirements if the specified maximum input jitter is present.
4. PECL logic, internally AC coupled.
5. Measured with a PRBS 2^7-1 test pattern, worst-case extinction ratio, BER ≤1×10^{-12}.

Recommended Interface Circuit

Figure 1 shows the recommended interface circuit.



Note: C1=C2=C3=10nF or 100nF

Note A: Circuit assumes open emitter output

Note B: Circuit assumes high impedance internal bias @Vcc-1.3V

Figure 1, Recommended Interface Circuit

Pin Definitions

Figure 2 below shows the pin numbering of SFF 2×5 electrical interface. The pin functions are described in Table 5 with some accompanying notes.

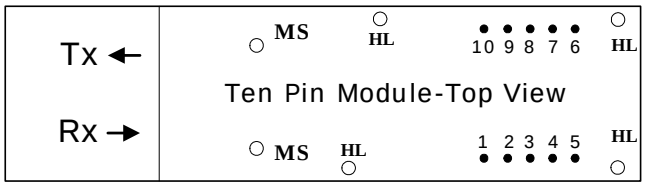


Figure 2, Pin View

Table 5– Pin Function Definitions

Pin No.	Name	Function	Notes
	MS	Mounting Studs	Note 5
	HL	Housing Leads	Note 6
1	V_{eer}	Receiver Signal Ground	
2	V_{ccr}	Receiver Power Supply	
3	SD	Signal Detect	Note 1
4	RD-	Received Data Out Bar	Note 2
5	RD+	Received Data Out	Note 2
6	V_{cct}	Transmitter Power Supply	
7	V_{eet}	Transmitter Signal Ground	
8	TDis	Transmitter Disable	Note 3
9	TD+	Transmitter Data In	Note 4
10	TD-	Transmitter Data In Bar	Note 4

Notes:

1. Normal operation: logic 1 output, V> 2.0V; fault condition: logic 0 output, V<0.8V.
2. PECL logic, internally AC coupled.
3. Transmitter output disable: (V_{cct} -1.3V)<V< $V_{cct;}$ transmitter output enable: V_{eet} <V<(V_{eet} +0.8V) or open circuit.
4. Internally AC coupled and 100Ω (differential) terminated input, PECL/CML compatible.
5. Mounting studs are provided for transceiver mechanical attachment to the circuit board. They also provide an optional connection of the transceiver to the equipment chassis ground. The holes in the circuit board must be tied to chassis ground.
6. Housing leads are provided for additional signal grounding. The holes in the circuit board must be included and tied to signal ground. Simultaneously there is a completed physical isolation between chassis ground and signal ground in the module.

Mechanical Design Diagram

The mechanical design diagram is shown in Figure 3.

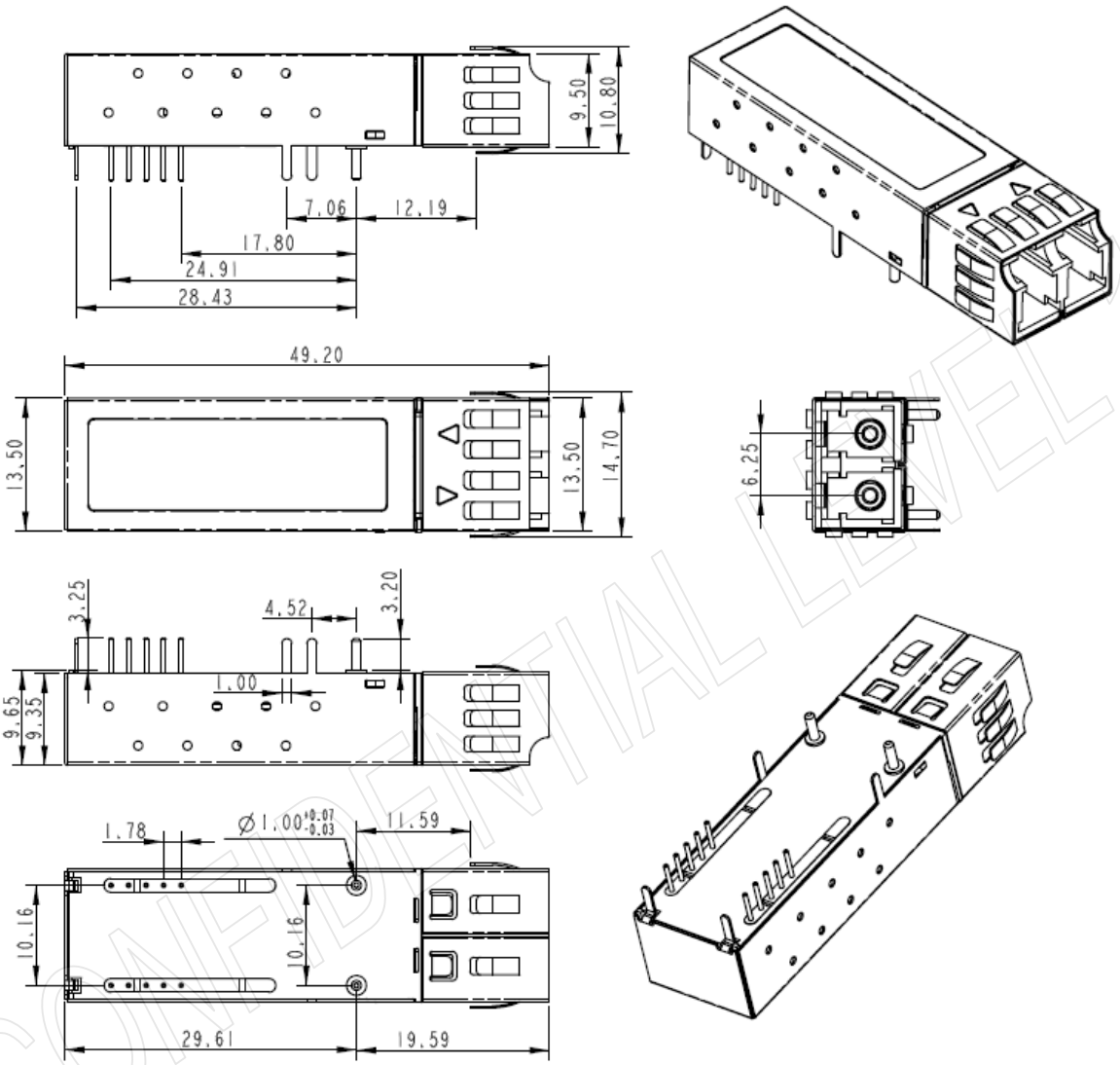
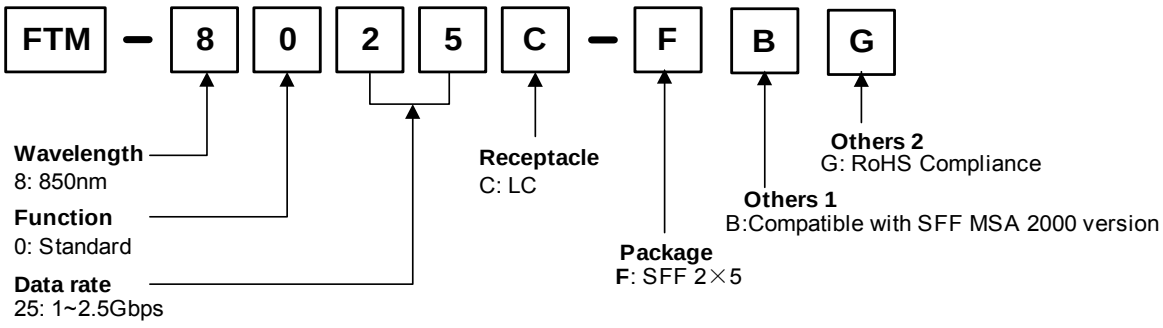


Figure 3, Mechanical Design Diagram of the SFF 2×5 (Dimension in mm)

Ordering information



Part No.	Product Description
FTM-8025C-FBG	850nm, 1~2.5Gbps, SFF 2×5, 0°C~+70°C，RoHS Compliance

Related Documents

For further information, please refer to the following documents:

- *Fiberxon SFF Transceiver Installation Guide*
- *Fiberxon SFF Transceiver Application Notes*
- *SFF Transceiver Multi-Source Agreement (MSA)*

Obtaining Document

You can visit our website:
http://www.fiberxon.com
Or contact with Fiberxon, Inc. America Sales Office listed at the end of documentation to get the latest documents.

Revision History

Revision	Initiate	Review	Approve	Subject	Release Date
Rev. 1a	Solaris Zhu	Tripper.Huang	Walker Wei	Initial datasheet	Dec 12, 2005
Rev. 1b	Solaris Zhu	Tripper.Huang	Walker Wei	Differentiate description on MS and HL	Dec 27, 2005
Rev. 1c	Solaris Zhu	Tripper.Huang	Walker Wei	Change SD Hysteresis from 1~4dB to 0.5~4dB	Feb 23, 2006
Rev. 1d	Henry xiao	Tripper.Huang	Walker Wei	Update Mechanical Design Diagram	Nov 13, 2006

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