CY7C197B

256 Kb (256K x 1) Static RAM

Features

- **Fast access time: 12 ns and 25 ns**
- **Wide voltage range: 5.0V ± 10% (4.5V to 5.5V)**
- **CMOS for optimum speed/power**
- **TTL-compatible Inputs and Outputs**
- **Available in 24 DIP and 24 SOJ**

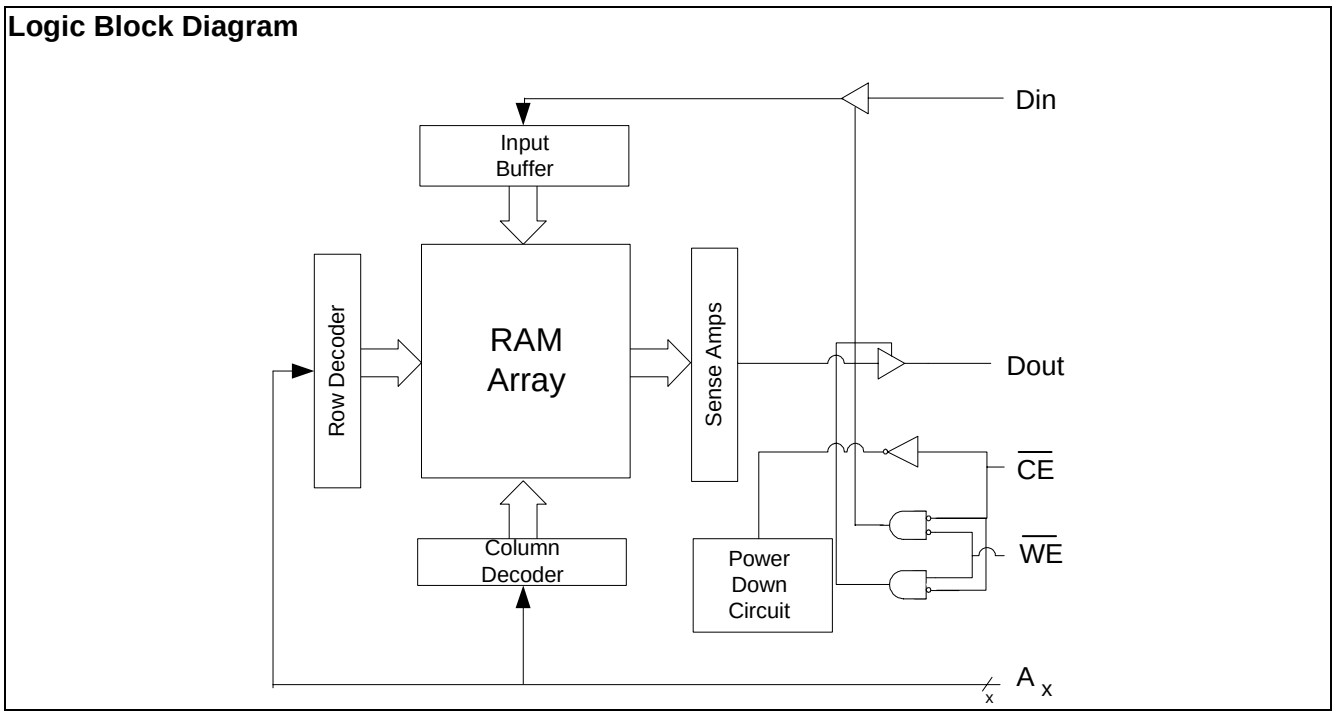
General Description[1]

The CY7C197B is a high-performance CMOS Asynchronous SRAM organized as 256K × 1 bits that supports an asynchronous memory interface. The device features an automatic power-down feature that significantly reduces power consumption when deselected.

See the Truth Table in this data sheet for a complete description of read and write modes.

The CY7C197B is available in 24 DIP and 24 SOJ package(s).

Logic Block Diagram



Product Portfolio

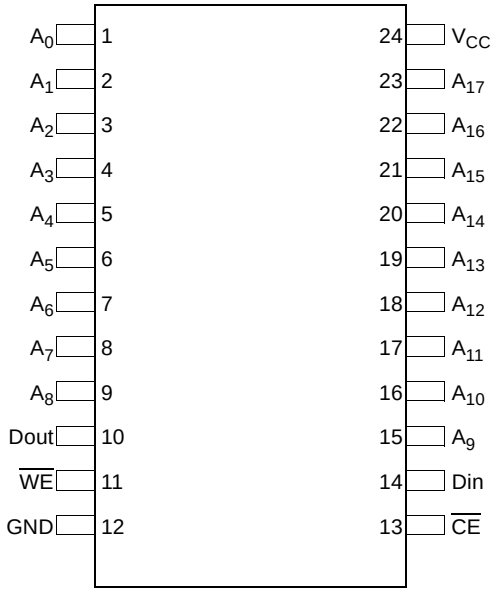
	12 ns	25 ns	Unit
Maximum Access Time	12	25	ns
Maximum Operating Current	150	95	mA
Maximum CMOS Standby Current	10	10	mA

Notes:

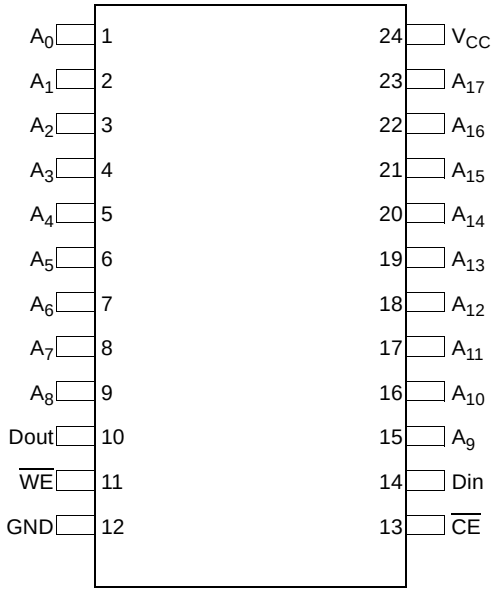
1. For best-practice recommendations, please refer to the Cypress application note *System Design Guidelines* at www.cypress.com.

Pin Layout and Specifications

24 DIP (6.6 × 31.8 × 3.5 mm) – P13



24 SOJ (8 × 15 × 3.5 mm) – V13



Pin Description

Pin	Type	Description	DIP	SOJ
A_X	Input	**Address Inputs**.	1, 2, 3, 4, 5, 6, 7, 8, 9, 15, 16, 17, 18, 19, 20, 21, 22, 23	1, 2, 3, 4, 5, 6, 7, 8, 9, 15, 16, 17, 18, 19, 20, 21, 22, 23
$\overline{CE}$	Control	**Chip Enable**.	13	13
Din	Input	**Data Input Pins**.	14	14
Dout	Output	**Data Output Pins**.	10	10
V_{CC}	Supply	**Power (5.0V)**.	24	24
$\overline{WE}$	Control	**Write Enable**.	11	11

Truth Table

$\overline{CE}$	$\overline{WE}$	Input/Output	Mode	Power
H	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	Data In	Write	Active (I_{CC})

Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested.)

Parameter	Description	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_{AMB}	Ambient Temperature with Power Applied (i.e., case temperature)	–55 to +125	°C
V_{CC}	Core Supply Voltage Relative to V_{SS}	–0.5 to +7.0	V
V_{IN}, V_{OUT}	DC Voltage Applied to any Pin Relative to V_{SS}	–0.5 to V_{CC} + 0.5	V
I_{OUT}	Output Short-Circuit Current	20	mA
V_{ESD}	Static Discharge Voltage (per MIL-STD-883, Method 3015)	> 2001	V
I_{LU}	Latch-up Current	> 200	mA

Operating Range

Range	Ambient Temperature (T_A)	Voltage Range (V_{CC})
Commercial	0°C to 70°C	5.0V ± 10%

DC Electrical Characteristics[2]

Parameter	Description	Condition	12 ns		25 ns		Unit
			Min	Max	Min	Max	
V_{IH}	Input HIGH Voltage	–	2.2	V_{CC}+0.3	2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.8	–0.3	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4	–	2.4	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., Iol = 8.0 mA	–	0.4	–	0.4	V
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = F_{MAX} = $1/t_{RC}$	–	150	–	95	mA
I_{SB1}	Automatic $\overline{CE}$ Power-down Current TTL Inputs	V_{CC} = Max., $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = F_{MAX}	–	30	–	30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-down Current CMOS Inputs	V_{CC} = Max., $\overline{CE} \geq V_{CC}$ – 0.3v, $V_{IN} \geq V_{CC}$ – 0.3v or V_{IN} < 0.3v, f = 0	–	10	–	10	mA
I_{OZ}	Output Leakage Current	GND ≤ Vi ≤ V_{CC}, Output Disabled	–5	+5	–5	+5	uA
I_{IX}	Input Load Current	GND ≤ Vi ≤ V_{CC}	–5	+5	–5	+5	uA

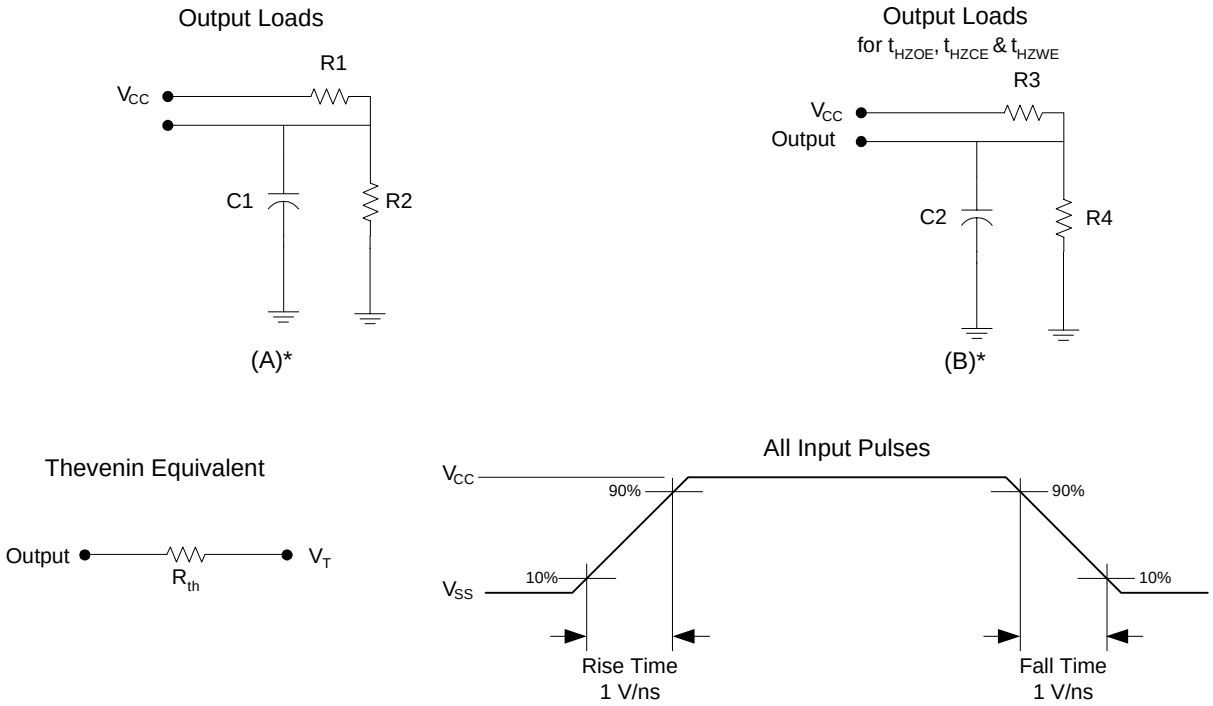
Capacitance[3]

Parameter	Description	Conditions	Max	Unit
			ALL – PACKAGES	
C_{IN}	Input Capacitance	T_A = 25C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	

Notes:

2. V_{IL} (min) = –2.0V for pulse durations of less than 20 ns.
3. Tested initially and after any design or process change that may affect these parameters.

AC Test Loads



* including scope and jig capacitance

AC Test Conditions

Parameter	Description	Nom.	Unit
C1	Capacitor 1	30	pF
C2	Capacitor 2	5	
R1	Resistor 1	480	Ω
R2	Resistor 2	255	
R3	Resistor 3	480	
R4	Resistor 4	255	
R_{TH}	Resistor Thevenin	167	
V_{TH}	Voltage Thevenin	1.73	V

Thermal Resistance[4]

Parameter	Description	Conditions	All – Packages	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 square inches, two-layer printed circuit board	TBD	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		TBD	

Notes:

4. Test conditions assume a transition time of 3 ns or less for –12 speed and 5 ns or less for –25 speed, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.

AC Electrical Characteristics[5, 6, 7]

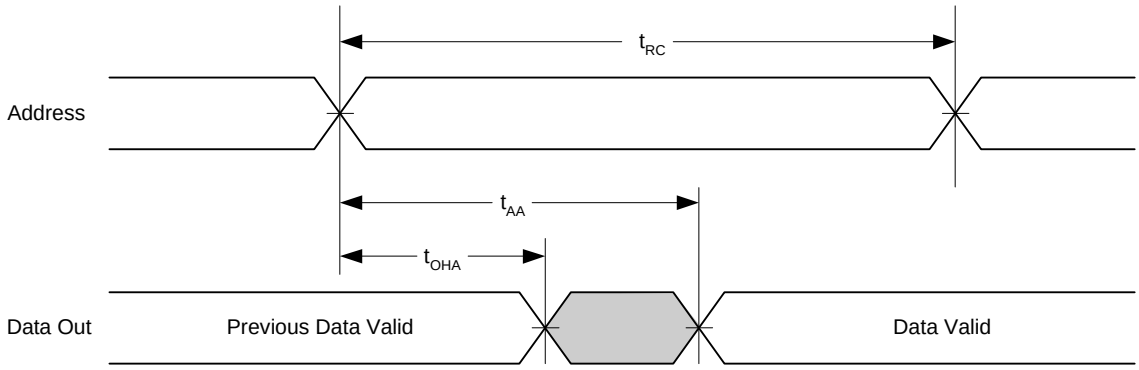
Parameter	Description	12 ns		25 ns		Unit
		Min	Max	Min	Max	
t_{RC}	Read Cycle Time	12	–	25	–	ns
t_{AA}	Address to Data Valid	–	12	–	25	ns
t_{OHA}	Data Hold from Address Change	3	–	3	–	ns
t_{ACE}	$\overline{CE}$ to Data Valid	–	12	–	25	ns
t_{LZCE}	$\overline{CE}$ to Low Z	3	–	3	–	ns
t_{HZCE}	$\overline{CE}$ to High Z	–	5	–	11	ns
t_{PU}	$\overline{CE}$ to Power-up	0	–	0	–	ns
t_{PD}	$\overline{CE}$ to Power-down	–	12	–	20	ns
t_{WC}	Write Cycle Time	12	–	25	–	ns
t_{SCE}	$\overline{CE}$ to Write End	9	–	20	–	ns
t_{AW}	Address Set-up to Write End	9	–	20	–	ns
t_{HA}	Address Hold from Write End	0	–	0	–	ns
t_{SA}	Address Set-up to Write Start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ Pulse Width	8	–	20	–	ns
t_{SD}	Data Set-up to Write End	8	–	15	–	ns
t_{HD}	Data Hold from Write End	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z	–	7	–	11	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	2	–	3	–	ns

Notes:

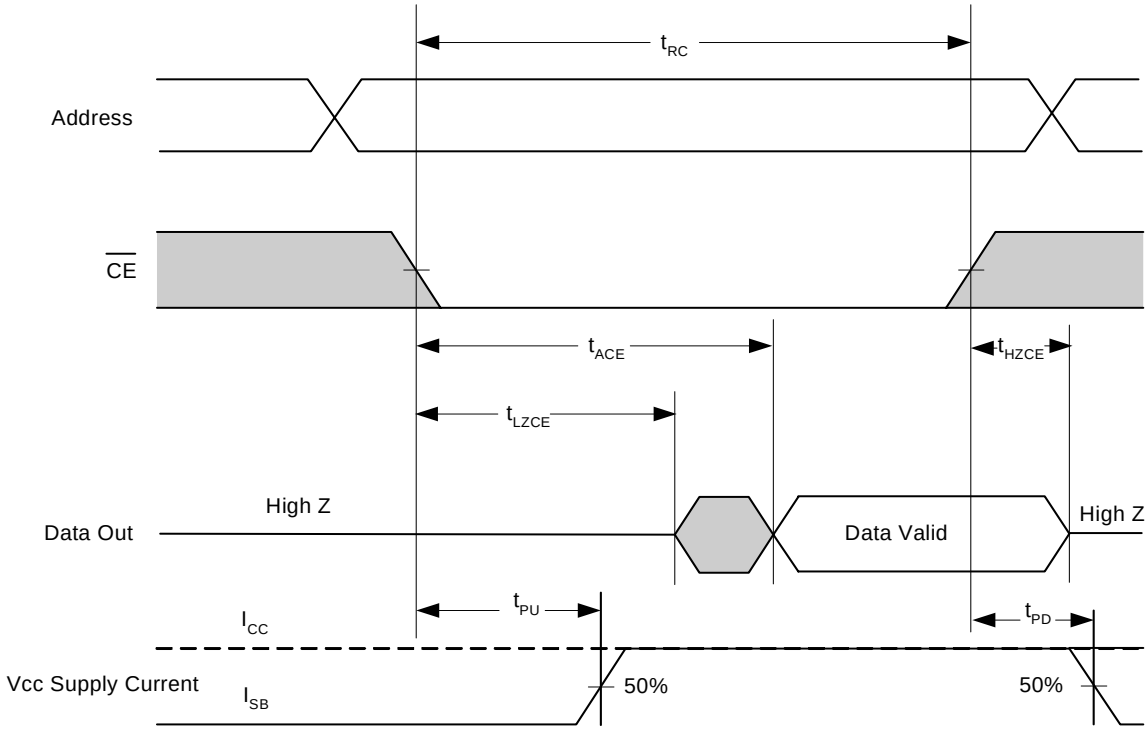
5. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
6. tHZCE and tLZCE are specified with CL = 5 pF as in part (B) in AC Test Loads and Waveforms. Transition is measured +/-500 mV from steady-state voltage.
7. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Timing Waveforms

Read Cycle No. 1 [8] [9]



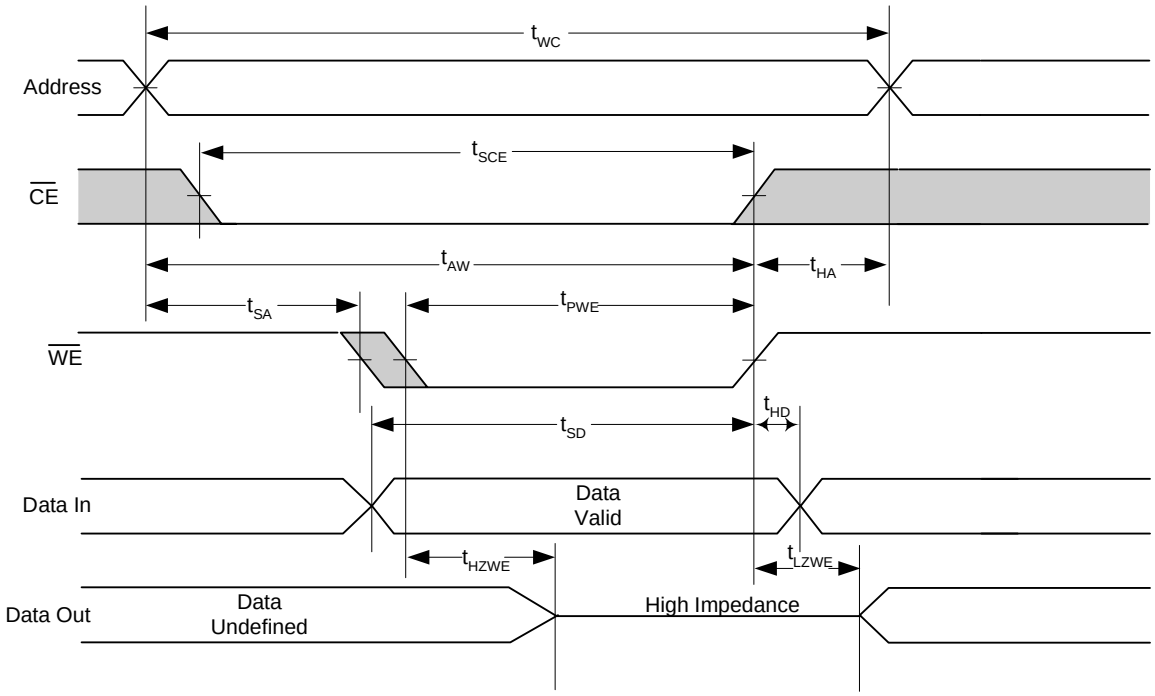
Read Cycle No. 2 [8]



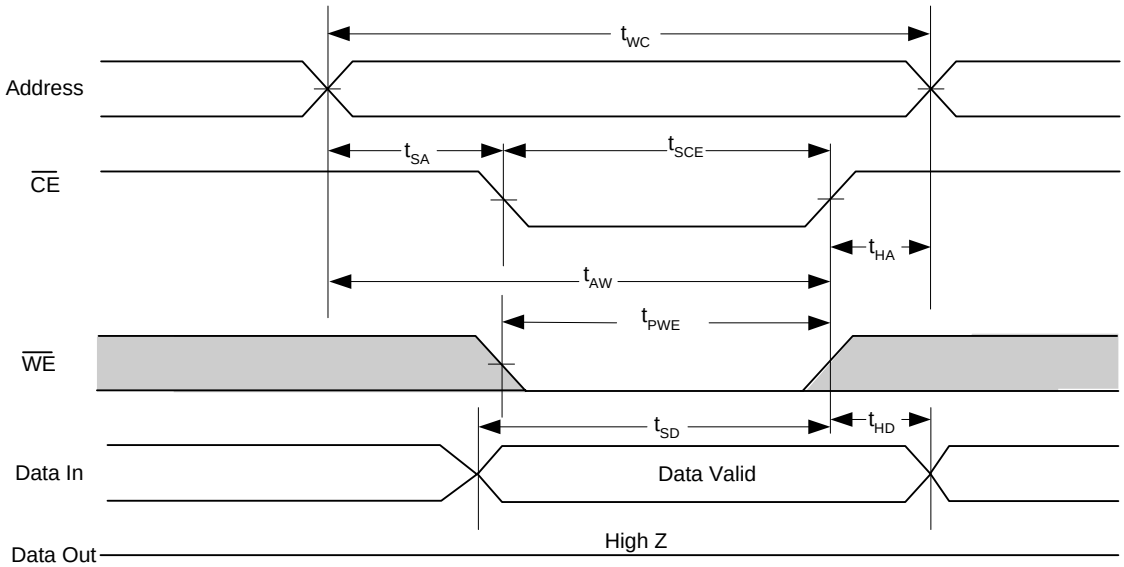
Notes:

8. $\overline{WE}$ is HIGH for ready cycle.
9. Device is continuously selected, $\overline{CE} = V_{IL}$.

Write Cycle No. 1 ($\overline{WE}$ Controlled)[7]



Write Cycle No. 2 ($\overline{CE}$ Controlled)[7,10]



Notes:

10. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high-impedance state.

Ordering Information

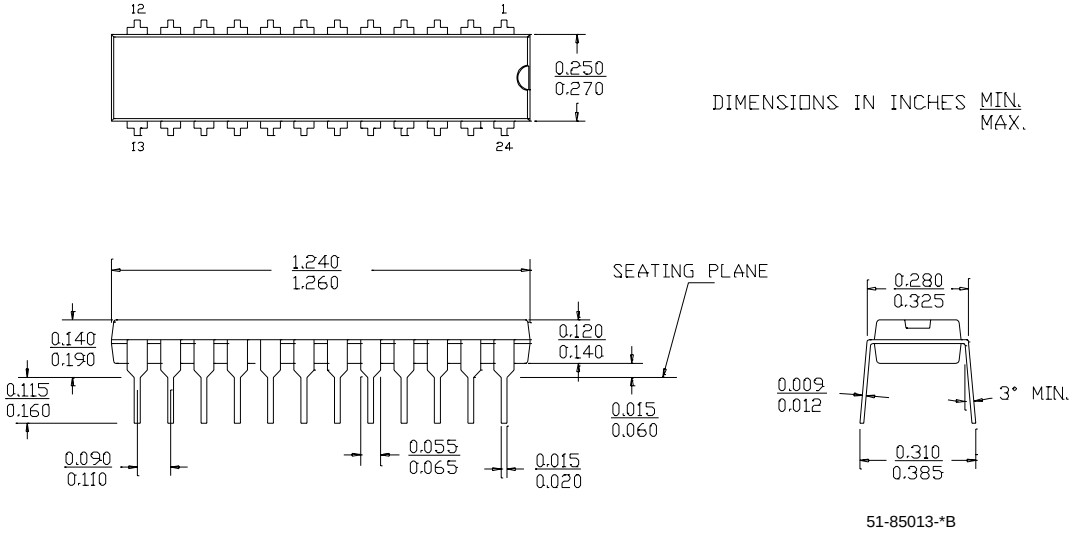
Speed	Ordering Code	Package Name	Package Type	Power Option	Operating Range
12 ns	CY7C197B-12VC	V13	24 SOJ (8 x 15 x 3.5 mm)	Standard	Commercial
25 ns	CY7C197B-25PC	P13	24 DIP (6.6 x 31.8 x 3.5 mm)	Standard	Commercial

Package Diagram

24-Lead (300-Mil) Molded SOJ V13

51-85030-*A

24-Lead (300-Mil) PDIP P13



51-85013-*B

Document History Page

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REV.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	129235	09/16/03	HGK	New Data Sheet