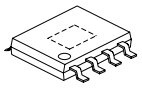
UR5516A

LINEAR INTEGRATED CIRCUIT

3A BUS TERMINATION REGULATOR



HSOP-8

*Pb-free plating product number: UR5516AL

■ DESCRIPTION

The UTC **UR5516A** is designed to provide a regulated voltage with bi-directional output current for DDR-SDRAM termination.

Current-limit work to limit the short-circuit current, on-chip thermal shutdown provides protection against any combination of overload that would create excessive junction temperature. The output voltage tracks the voltage at V_{REF} pin. A resistor divider connected to V_{IN}, GND and V_{REF} pins is used to provide a half voltage of V_{IN} to V_{REF} pin. In addition, an external ceramic capacitor and an open-drain transistor connected to V_{REF} pin provides soft-start and shutdown control respectively. Pulling and holding the V_{REF} to GND shuts off the output. The output of UTC **UR5516A** will be high impedance after being shut down by V_{REF} or thermal shutdown function.

■ FEATURES

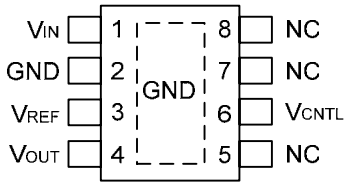
* Provide bi-direction current
  - Sourcing or sinking current up to 3A
* 1.25V/0.9V output for DDR I/II applications
* Fast transient response
* High output accuracy
  - ±20mv over load, V_{OUT} offset and temperature
* Adjustable output voltage by external resistors
* Current-limit protection
* On-chip thermal shutdown
* Shutdown for standby or suspend mode

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Normal	Lead Free Plating		
UR5516A-SH2-R	UR5516AL-SH2-R	HSOP-8	Tape Reel
UR5516A-SH2-T	UR5516AL-SH2-T	HSOP-8	Tube

U5516AL-SH2-R (1)Packing Type (2)Package Type (3)Lead Plating	(1) R: Tape Reel, T: Tube (2) SH2: HSOP-8 (3) L: Lead Free Plating, Blank: Pb/Sn

■ PIN CONFIGURATION

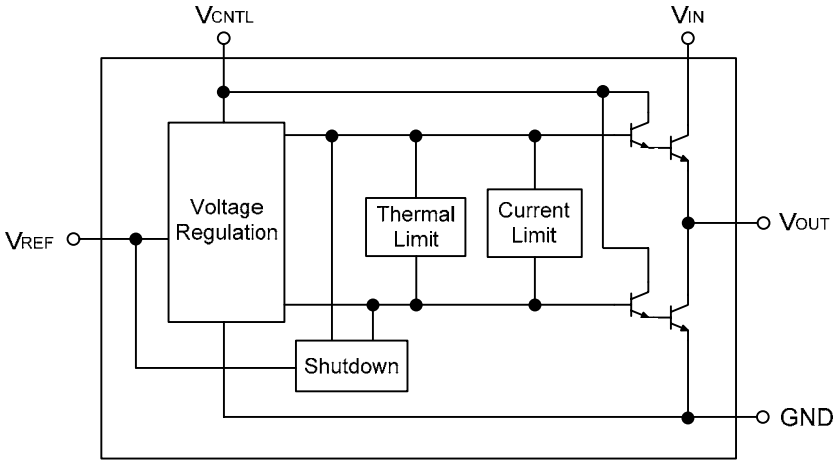


NC: No Connection

■ PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
V_{IN}	I	Main power input pin. Connect this pin to a voltage source and an input capacitor. The UTC **UR5516A** sources current to V_{OUT} pin by controlling the upper NPN pass transistor, providing a current path from VIN pin.
GND	O	Power and signal ground. Connect this pin to system ground plane with shortest traces. The UTC **UR5516A** sinks current from V_{OUT} pin by controlling the lower NPN pass transistor, providing a current path to GND pin. This pin is also the ground path for internal control circuitry.
V_{CNTL}	I	Power input pin for internal control circuitry. Connect this pin to a voltage source, providing a bias for the internal control circuitry. A bypass capacitor is usually connected near this pin.
V_{REF}	I	Reference voltage input and active-low shutdown control pin. Apply a voltage to this pin as a reference voltage for the UTC **UR5516A**. Connect this pin to a resistor divider, between V_{IN} and GND, and a capacitor for soft-start and filtering noise purposes. Applying and holding this pin low by an open-drain transistor to shut down the output.
V_{OUT}	O	Output pin of the regulator. Connect this pin to load. Output capacitors connected this pin improves stability and transient response. The output voltage tracks the reference voltage and is capable of sourcing or sinking current up to 3A.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
V_{CNTL} Supply Voltage, V_{CNTL} to GND	V_{CNTL}	-0.2 ~ 7	V
V_{IN} Supply Voltage, V_{IN} to GND	V_{IN}	-0.2 ~ 3.9	V
Power Dissipation	P_D	Internally Limited	W
Junction Temperature	T_J	+150	°C
Storage Temperature	T_{STG}	-40 ~ +150	°C

Note Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RANGES	UNIT
V_{CNTL} Supply Voltage (Note 1)	V_{CNTL}	3.1 ~ 6	V
V_{IN} Supply Voltage (Note 2)	V_{IN}	1.2 ~ 3.5	V
V_{REF} Input Voltage	V_{REF}	0.85 ~ 1.75	V
V_{OUT} Output Voltage (Note 3)	V_{OUT}	V_{REF} ± 0.02	V
V_{OUT} Output Current (Note 4,5)	I_{OUT}	-3 ~ +3	A
Junction Temperature	T_J	0 ~ +125	°C

Note: 1. Please always keep V_{CNTL}-V_{OUT}>1.9V for good regulation.

2. Please supply enough voltage to V_{IN} for sourcing desired maximum output current. Please refer to the V_{IN} Dropout Voltage vs. Output Current in the Typical Characteristics.
3. The V_{OUT} is regulated to the V_{REF} with additional voltage offset and load regulation except over-load conditions.
4. The symbol “+” means the V_{OUT} sources current to load; the symbol “-“ means the V_{OUT} sinks current to GND.
5. The max. I_{OUT} varies with the T_J and the voltages of V_{IN}-V_{OUT} and V_{OUT}. Please refer to the Typical Characteristics.

■ THERMAL DATA

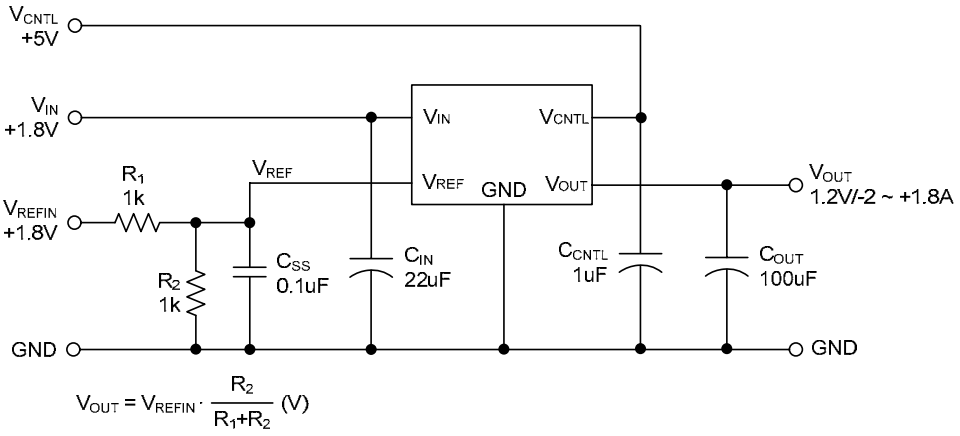
PARAMETER	SYMBOL	RATINGS	UNIT
Thermal Resistance	θ_{JA}	80	°C/W

■ ELECTRICAL CHARACTERISTICS(T_J=25°C,V_{CNTL}=3.3V,V_{IN}=2.5V/1.8V,V_{REF}=0.5V_{IN},unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output Voltage	V_{OUT}	I_{OUT}=0A			V_{REF}		V
System Accuracy		Over temperature, V_{OUT} offset, and load regulation		-20		20	mV
Offset Voltage (V_{OUT}–V_{REF})	$V_{O(OFF)}$	I_{OUT}=+10mA		-20			mV
		I_{OUT}=-10mA				20	
Load Regulation	ΔV_{OUT}	I_{OUT}=+10mA ~ +3A				2	%
		I_{OUT}= -10mA ~ -3A				2	
Current Limit	I_{LIMIT}	Sourcing Current (V_{IN}=2.5V)	T_J=25°C	+3	+3.6		A
			T_J=125°C		+3.1		
		Sinking Current (V_{IN}=2.5V)	T_J=25°C	-3	-3.6		
			T_J=125°C		-3.1		
		Sourcing Current (V_{IN}=1.8V)	T_J=25°C	+2.9	+3.2		
			T_J=125°C		+2.6		
		Sinking Current (V_{IN}=1.8V)	T_J=25°C	-2.9	-3.2		
			T_J=125°C		-2.6		
Thermal Shutdown Temperature	T_{SHDN}	Rising T_J			183		°C
Thermal Shutdown Hysteresis	T_{HYS}				42		°C
V_{CNTL} Supply Current	I_{CNTL}	I_{OUT}=0A		1	2	3	mA
		I_{OUT}=±3A (Normal Operation)			50	110	
		V_{REF}=GND (Shutdown)			2.0		
V_{REF} Bias Current (The current flows out of V_{REF})	I_{BIAS}	V_{REF}=1.25V/0.9V (Normal Operation)			200	500	nA
		V_{REF}=GND (Shutdown)			20	40	μA
Shutdown Threshold Voltage	V_{SHDN}			0.2	0.35	0.65	V

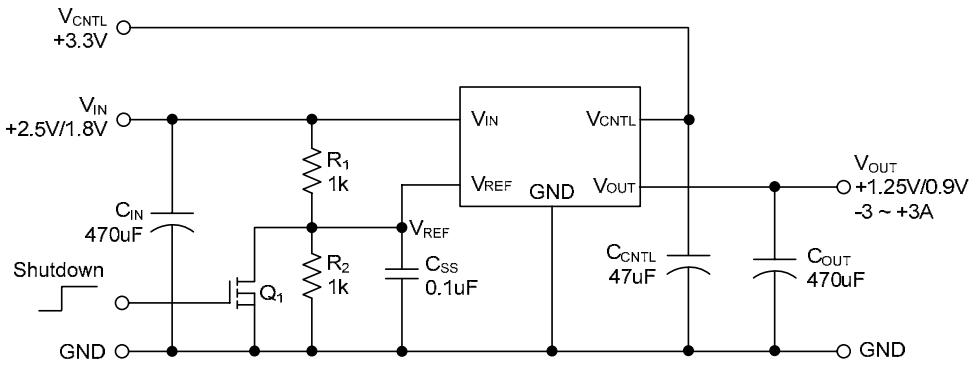
■ APPLICATIONS CIRCUIT

1. General Application



$$V_{OUT} = V_{REFIN} \cdot \frac{R_2}{R_1+R_2} \text{ (V)}$$

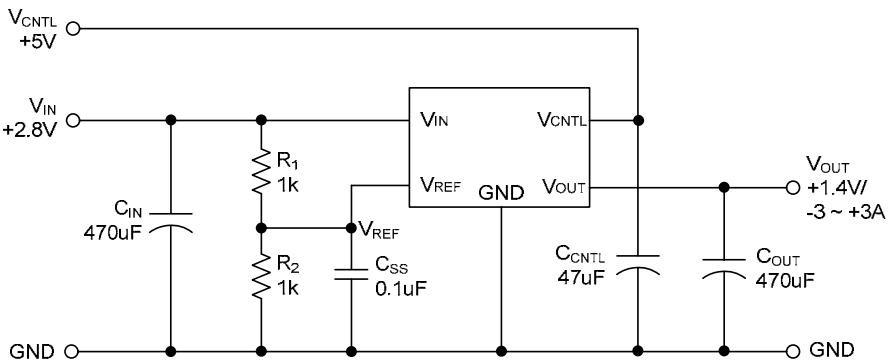
2. For V_{OUT}=1.25V/0.9V



C_{OUT} : 470μF, ESR=25mΩ
R_1, R_2 : 1kΩ, 1%
Q1 : APM2300 AC

Note : Since R1 and R2 are very small, the voltage offset caused by the bias current of V_{REF} can be ignore.

3. For V_{OUT}=1.4V

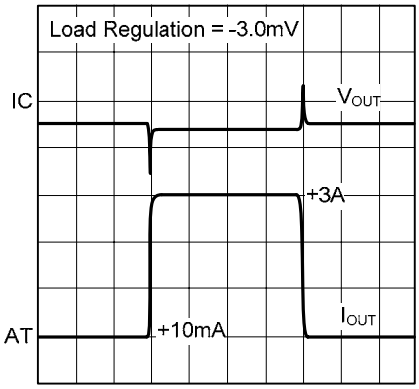


■ OPERATING WAVEFORMS

1. Load Transient Response: I_{OUT} = +10mA -> +3A -> +10mA

- V_{IN} = 2.5V, V_{CNTL} = 3.3V
- V_{REF} is 1.250V supplied by a regulator
- C_{OUT} = 470μF/10V, ESR = 30mΩ
- I_{OUT} slew rate = ±3A/μS

I_{OUT} = +10mA -> +3A -> +10mA

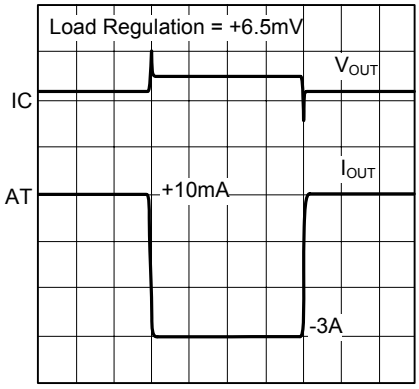


Ch1 : V_{OUT}, 20mV/Div, DC,
Offset = 1.250V
Ax1 : I_{OUT}, 1A/Div
Time : 20μS/Div

2. Load Transient Response: I_{OUT} = -10mA -> -3A -> -10mA

- V_{IN} = 2.5V, V_{CNTL} = 3.3V
- V_{REF} is 1.250V supplied by a regulator
- C_{OUT} = 470μF/10V, ESR = 30mΩ
- I_{OUT} slew rate = ±3A/μS

I_{OUT} = -10mA -> -3A -> -10mA



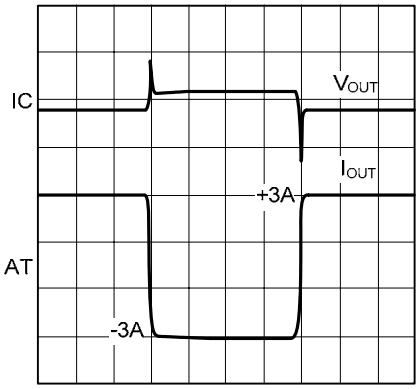
Ch1 : V_{OUT}, 20mV/Div, DC,
Offset = 1.250V
Ax1 : I_{OUT}, 1A/Div
Time : 20μS/Div

■ OPERATNG WAVEFORMS(Cont.)

3. Load Transient Response: I_{OUT} = +3A -> -3A -> +3A

- V_{IN} = 2.5V, V_{CNTL} = 3.3V
- V_{REF} is 1.250V supplied by a regulator
- C_{OUT} = 470μF/10V, ESR = 30mΩ
- I_{OUT} slew rate = ±3A/μS

I_{OUT} = +3A -> -3A -> +3A

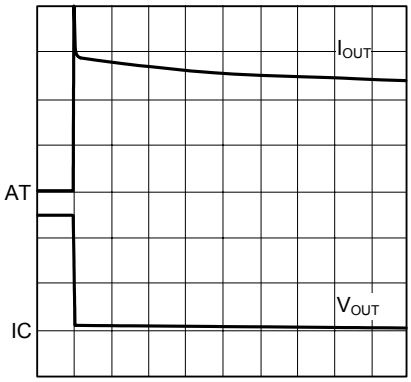


Ch1 : V_{OUT}, 50mV/Div, DC,
Offset = 1.250V
Ax1 : I_{OUT}, 2A/Div
Time : 20μS/Div

4. Short-Circuit Test

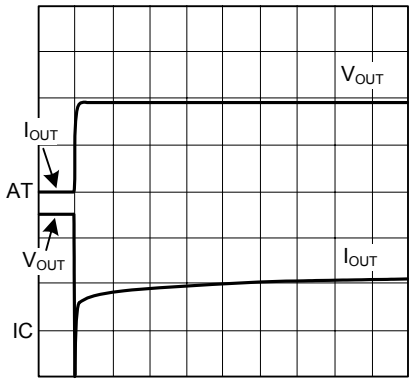
- V_{IN} = 2.5V, V_{CNTL} = 3.3V

V_{OUT} is Shorted to GND



Ch1 : V_{OUT}, 500mV/Div, DC,
Offset = 1.250V
Ax1 : I_{OUT}, 2A/Div
Time : 5mS/Div

V_{OUT} is Shorted to V_{IN} (2.5V)



Ch1 : V_{OUT}, 500mV/Div, DC,
Offset = 1.250V
Ax1 : I_{OUT}, 2A/Div
Time : 5mS/Div

■ TYPICAL CHARACTERISTICS