## Features

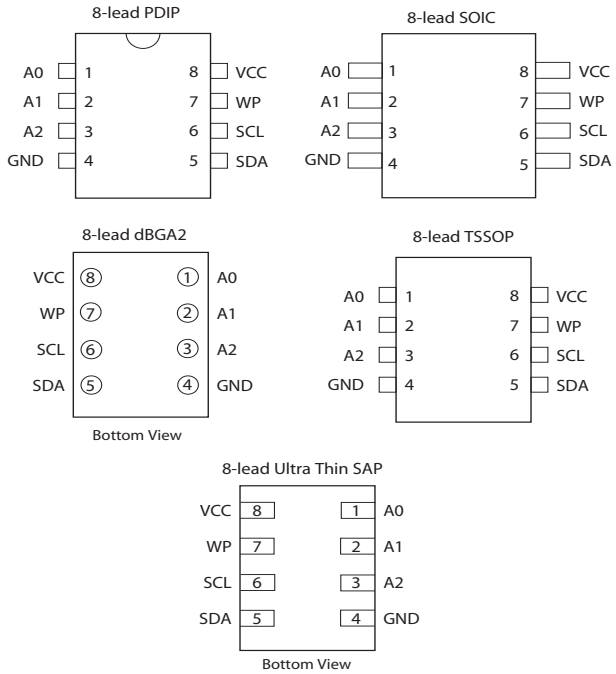
- Low-voltage and Standard-voltage Operation
  - 1.8 ($V_{CC}$ = 1.8V to 5.5V)
- Internally Organized as 32,768 x 8
- Two-wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 1 MHz (5.0V, 2.7V, 2.5V), and 400 kHz (1.8V) Compatibility
- Write Protect Pin for Hardware and Software Data Protection
- 64-byte Page Write Mode (Partial Page Writes Allowed)
- Self-timed Write Cycle (5 ms Max)
- High Reliability
  - Endurance: One Million Write Cycles
  - Data Retention: 40 Years
- Lead-free/Halogen-free Devices Available
- 8-lead JEDEC PDIP, 8-lead JEDEC SOIC, EIAJ SOIC, 8-lead Ultra Thin Small Array Package (SAP), 8-lead TSSOP, and 8-ball dBGA2 Packages
- Die Sales: Wafer Form, Waffle Pack and Bumped Wafers

## Description

The AT24C256B provides 262,144 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 32,768 words of 8 bits each. The device's cascadable feature allows up to eight devices to share a common two-wire bus. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The devices are available in space-saving 8-lead JEDEC PDIP, 8-lead JEDEC SOIC, 8-lead Ultra Thin SAP, 8-lead TSSOP, and 8-ball dBGA2 packages. In addition, the entire family is available in a 1.8V (1.8V to 5.5V) version.

## Pin Configurations

| Pin Name | Function |
|---|---|
| A0–A2 | Address Inputs |
| SDA | Serial Data |
| SCL | Serial Clock Input |
| WP | Write Protect |
| GND | Ground |




# Two-wire Serial EEPROM

**256K (32,768 x 8)**

# AT24C256B

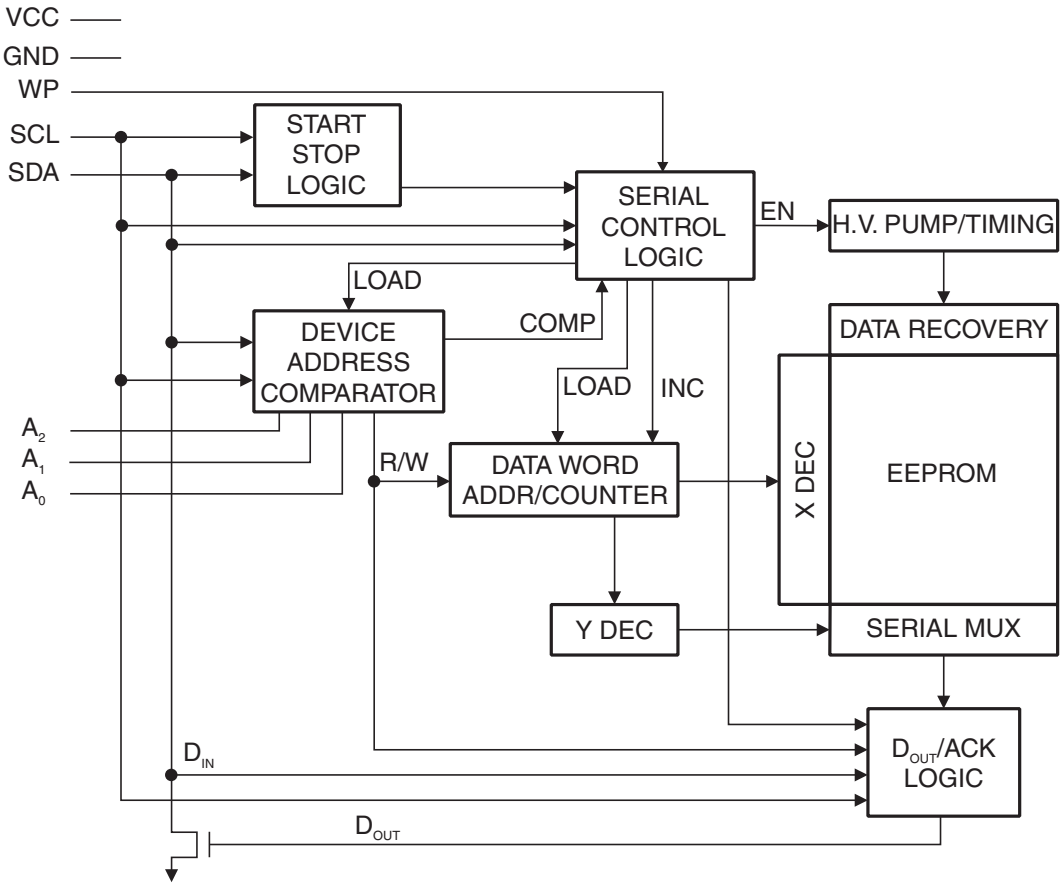
Rev. 5279C–SEEPR–3/09

# 1. Absolute Maximum Ratings*

| | |
|---|---|
| Operating Temperature | – 55°C to +125°C |
| Storage Temperature | – 65°C to +150°C |
| Voltage on Any Pin with Respect to Ground | – 1.0V to +7.0V |
| Maximum Operating Voltage | 6.25V |
| DC Output Current | 5.0 mA |

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Figure 1-1.** Block Diagram



## 2. Pin Description

**SERIAL CLOCK (SCL):** The SCL input is used to positive-edge clock data into each EEPROM device and negative-edge clock data out of each device.

**SERIAL DATA (SDA):** The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1, and A0 pins are device address inputs that are hardwired (directly to GND or to Vcc) for compatibility with other AT24Cxx devices. When the pins are hardwired, as many as eight 256K devices may be addressed on a single bus system. (Device addressing is discussed in detail under “Device Addressing,” page 9.) A device is selected when a corresponding hardware and software match is true. If these pins are left floating, the A2, A1, and A0 pins will be internally pulled down to GND. However, due to capacitive coupling that may appear during customer applications, Atmel recommends always connecting the address pins to a known state. When using a pull-up resistor, Atmel recommends using 10kΩ or less.

**WRITE PROTECT (WP):** The write protect input, when connected to GND, allows normal write operations. When WP is connected directly to Vcc, all write operations to the memory are inhibited. If the pin is left floating, the WP pin will be internally pulled down to GND. However, due to capacitive coupling that may appear during customer applications, Atmel recommends always connecting the WP pins to a known state. When using a pull-up resistor, Atmel recommends using 10kΩ or less.

## 3. Memory Organization

**AT24C256B, 256K SERIAL EEPROM:** The 256K is internally organized as 512 pages of 64 bytes each. Random word addressing requires a 15-bit data word address.

**Table 3-1.** Pin Capacitance[1]

Applicable over recommended operating range from $T_A$ = 25°C, f = 1.0 MHz, $V_{CC}$ = +1.8V

| Symbol | Test Condition | Max | Units | Conditions |
|---|---|---|---|---|
| $C_{I/O}$ | Input/Output Capacitance (SDA) | 8 | pF | $V_{I/O}$ = 0V |
| $C_{IN}$ | Input Capacitance ($A_0$, $A_1$, SCL) | 6 | pF | $V_{IN}$ = 0V |

Note: 1. This parameter is characterized and is not 100% tested.

**Table 3-2.** DC Characteristics

Applicable over recommended operating range from: $T_{AI}$ = – 40°C to +85°C, $V_{CC}$ = +1.8V to +5.5V (unless otherwise noted)

| Symbol | Parameter | Test Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{CC1}$ | Supply Voltage | | | 1.8 | | 5.5 | V |
| $I_{CC1}$ | Supply Current | $V_{CC}$ = 5.0V | READ at 400 kHz | | 1.0 | 2.0 | mA |
| $I_{CC2}$ | Supply Current | $V_{CC}$ = 5.0V | WRITE at 400 kHz | | 2.0 | 3.0 | mA |
| $I_{SB1}$ | Standby Current (1.8V option) | $V_{CC}$ = 1.8V | $V_{IN}$ = $V_{CC}$ or $V_{SS}$ | | | 1.0 | µA |
| | | $V_{CC}$ = 5.5V | | | | 6.0 | µA |
| $I_{LI}$ | Input Leakage Current $V_{CC}$ = 5.0V | $V_{IN}$ = $V_{CC}$ or $V_{SS}$ | | | 0.10 | 3.0 | µA |
| $I_{LO}$ | Output Leakage Current $V_{CC}$ = 5.0V | $V_{OUT}$ = $V_{CC}$ or $V_{SS}$ | | | 0.05 | 3.0 | µA |
| $V_{IL}$ | Input Low Level(1) | | | – 0.6 | | $V_{CC}$ x 0.3 | V |
| $V_{IH}$ | Input High Level(1) | | | $V_{CC}$ x 0.7 | | $V_{CC}$ + 0.5 | V |
| $V_{OL2}$ | Output Low Level | $V_{CC}$ = 3.0V | $I_{OL}$ = 2.1 mA | | | 0.4 | V |
| $V_{OL1}$ | Output Low Level | $V_{CC}$ = 1.8V | $I_{OL}$ = 0.15 mA | | | 0.2 | V |

Notes: 1. $V_{IL}$ min and $V_{IH}$ max are reference only and are not tested.

**Table 3-3.** AC Characteristics (Industrial Temperature)

Applicable over recommended operating range from $T_{AI}$ = – 40°C to +85°C, $V_{CC}$ = +1.8V to +5.5V, CL = 100 pF (unless otherwise noted). Test conditions are listed in Note 2.

| Symbol | Parameter | 1.8-volt | | 2.5, 5.0-volt | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $f_{SCL}$ | Clock Frequency, SCL | | 400 | | 1000 | kHz |
| $t_{LOW}$ | Clock Pulse Width Low | 1.3 | | 0.4 | | µs |
| $t_{HIGH}$ | Clock Pulse Width High | 0.6 | | 0.4 | | µs |
| $t_i$ | Noise Suppression Time(1) | | 100 | | 50 | ns |
| $t_{AA}$ | Clock Low to Data Out Valid | 0.05 | 0.9 | 0.05 | 0.55 | µs |
| $t_{BUF}$ | Time the bus must be free before a new transmission can start(1) | 1.3 | | 0.5 | | µs |
| $t_{HD.STA}$ | Start Hold Time | 0.6 | | 0.25 | | µs |
| $t_{SU.STA}$ | Start Set-up Time | 0.6 | | 0.25 | | µs |
| $t_{HD.DAT}$ | Data In Hold Time | 0 | | 0 | | µs |
| $t_{SU.DAT}$ | Data In Set-up Time | 100 | | 100 | | ns |
| $t_R$ | Inputs Rise Time(1) | | 0.3 | | 0.3 | µs |
| $t_F$ | Inputs Fall Time(1) | | 300 | | 100 | ns |
| $t_{SU.STO}$ | Stop Set-up Time | 0.6 | | 0.25 | | µs |
| $t_{DH}$ | Data Out Hold Time | 50 | | 50 | | ns |
| $t_{WR}$ | Write Cycle Time | | 5 | | 5 | ms |
| Endurance(1) | 25°C, Page Mode, 3.3V | 1,000,000 | | | | Write Cycles |

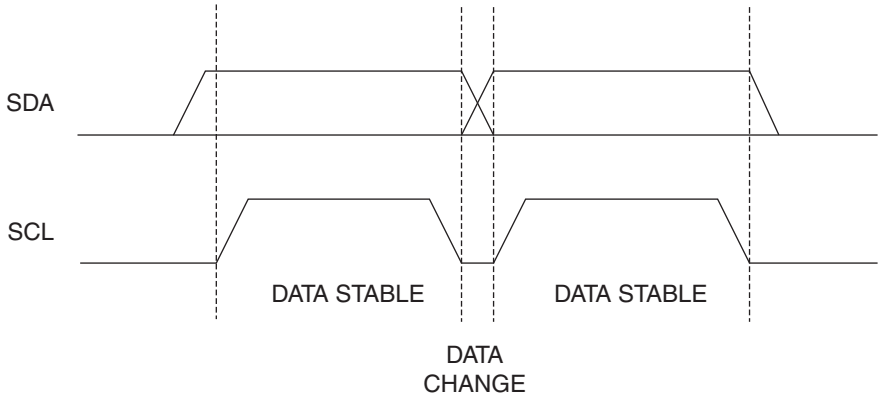
Notes: 1. This parameter is ensured by characterization and is not 100% tested.

2. AC measurement conditions:
   $R_L$ (connects to $V_{CC}$): 1.3 kΩ (2.5V, 5.5V), 10 kΩ (1.8V)
   Input pulse voltages: 0.3 $V_{CC}$ to 0.7 $V_{CC}$
   Input rise and fall times: ≤ 50 ns
   Input and output timing reference voltages: 0.5 $V_{CC}$

# 4. Device Operation

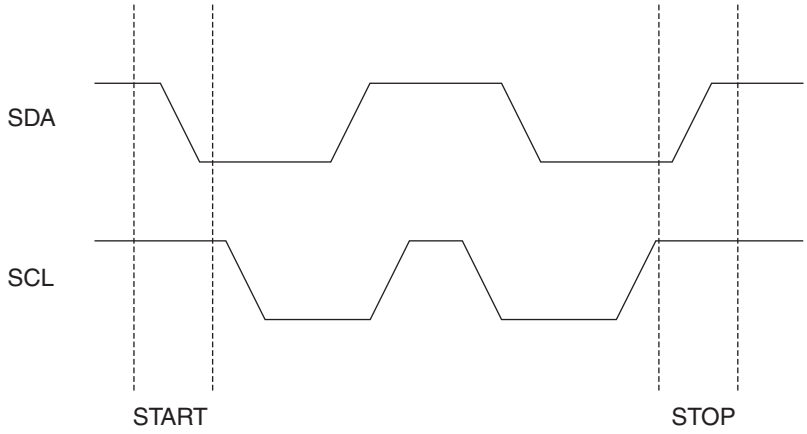
**CLOCK and DATA TRANSITIONS:** The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 4-1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

**Figure 4-1.** Data Validity




**START CONDITION:** A high-to-low transition of SDA with SCL high is a start condition that must precede any other command (see Figure 4-2).

**Figure 4-2.** Start and Stop Definition




**STOP CONDITION:** A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see Figure 4-2).

**ACKNOWLEDGE:** All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a “0” during the ninth clock cycle to acknowledge that it has received each word.

**STANDBY MODE:** The AT24C256B features a low-power standby mode that is enabled upon power-up and after the receipt of the stop bit and the completion of any internal operations.

**SOFTWARE RESET:** After an interruption in protocol, power loss or system reset, any 2-wire part can be protocol reset by following these steps: (a) Create a start bit condition, (b) clock 9 cycles, (c) create another start bit followed by stop bit condition as shown below. The device is ready for next communication after above steps have been completed.

**Figure 4-3.** Software Reset

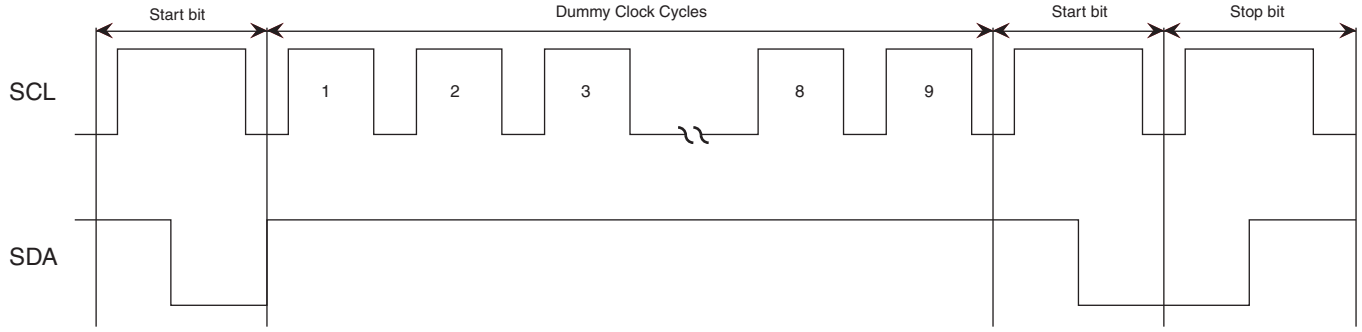



**Figure 4-4.** Bus Timing

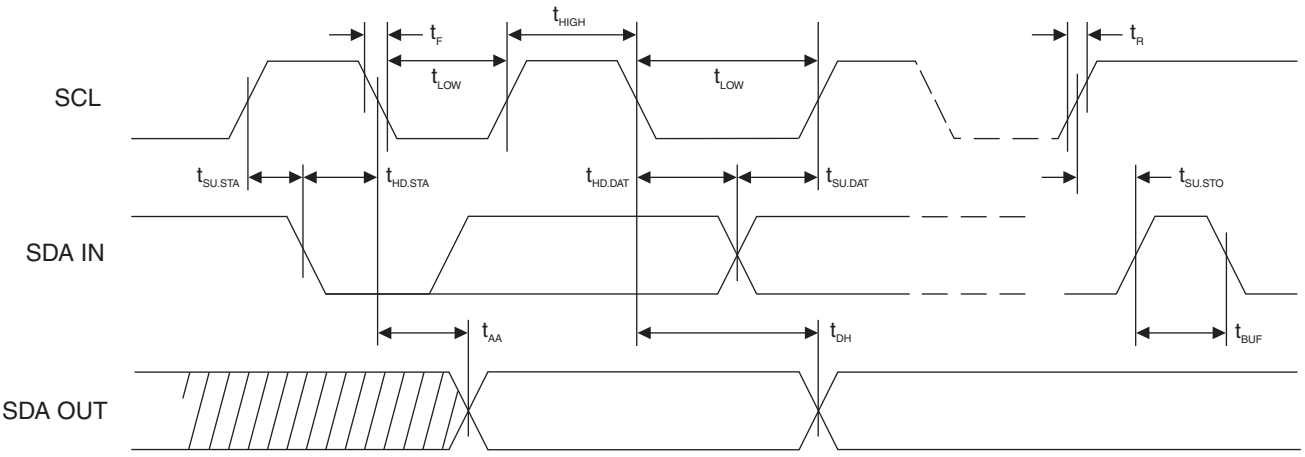
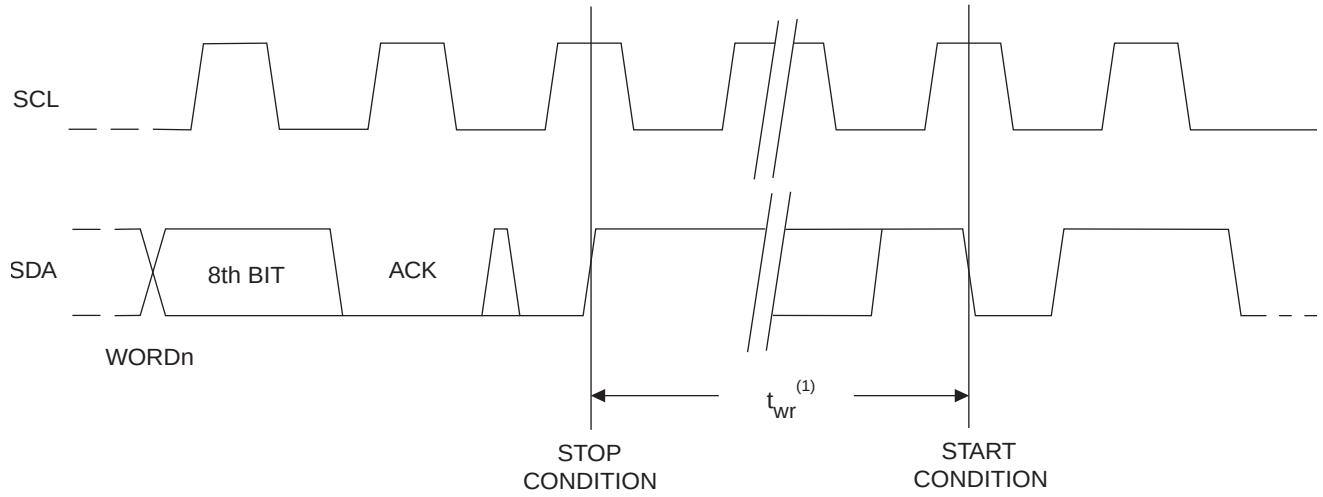
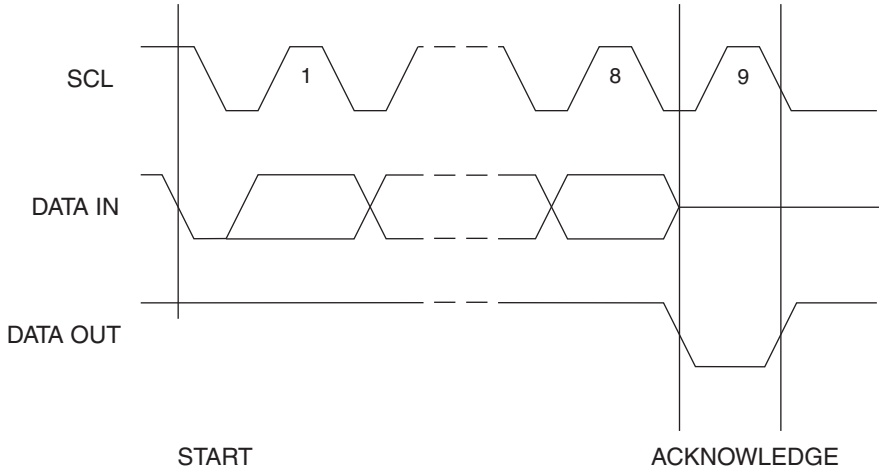



**Figure 4-5.** Write Cycle Timing




Note: 1. The write cycle time $t_{WR}$ is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

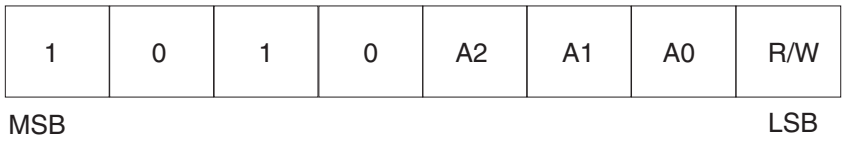
**Figure 4-6.** Output Acknowledge



## 5. Device Addressing

The 256K EEPROM requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Figure 5-1). The device address word consists of a mandatory “1”, “0” sequence for the first four most significant bits as shown. This is common to all two-wire EEPROM devices.

**Figure 5-1.** Device Address




The next three bits are the A2, A1, A0 device address bits to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins. The A2, A1, and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high, and a write operation is initiated if this bit is low.

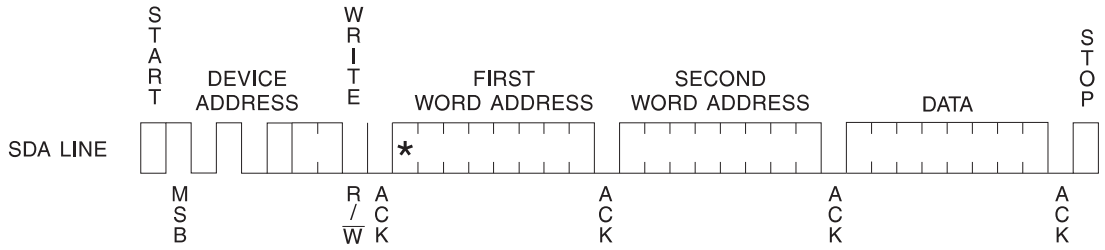
Upon a compare of the device address, the EEPROM will output a “0”. If a compare is not made, the device will return to a standby state.

**DATA SECURITY:** The AT24C256B has a hardware data protection scheme that allows the user to write protect the whole memory when the WP pin is at $V_{CC}$.

# 6. Write Operations

**BYTE WRITE:** A write operation requires two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a “0” and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a “0”. The addressing device, such as a microcontroller, must then terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, $t_{WR}$, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 6-1).

**Figure 6-1.** Byte Write

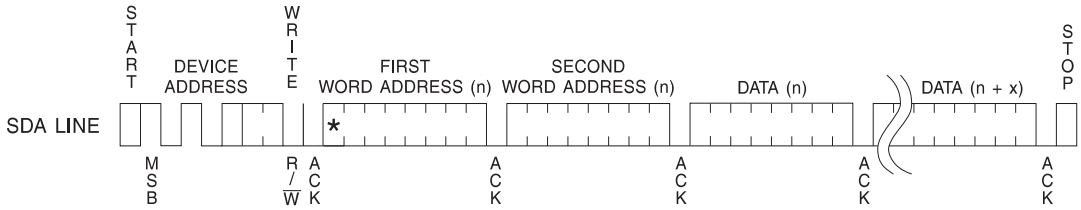



Note: * = DON’T CARE bit

**PAGE WRITE:** The 256K EEPROM is capable of 64-byte page writes.

A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 63 more data words. The EEPROM will respond with a “0” after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 6-2).

**Figure 6-2.** Page Write




Note: * = DON’T CARE bit

The data word address lower six bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 64 data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten. The address “roll over” during write is from the last byte of the current page to the first byte of the same page.

**ACKNOWLEDGE POLLING:** Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a “0”, allowing the read or write sequence to continue.

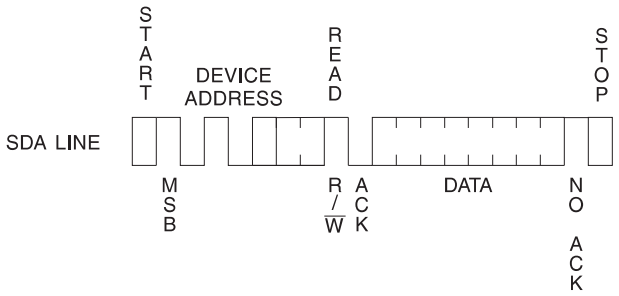
## 7. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to “1”. There are three read operations: current address read, random address read, and sequential read.

**CURRENT ADDRESS READ:** The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address “roll over” during read is from the last byte of the last memory page, to the first byte of the first page.

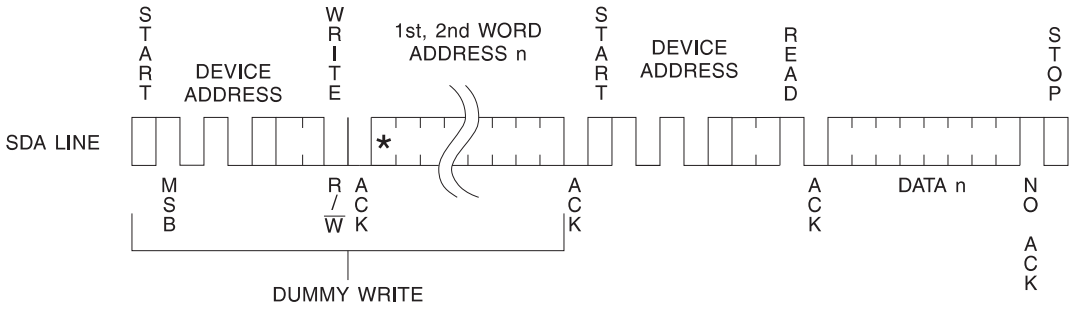
Once the device address with the read/write select bit set to “1” is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input “0” but does generate a following stop condition (see Figure 7-1).

**Figure 7-1.** Current Address Read




**RANDOM READ:** A random read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 7-2).

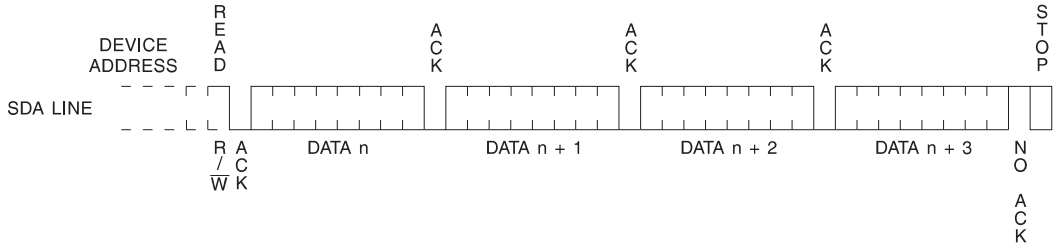
**Figure 7-2.** Random Read




Note: * = DON’T CARE bit

**SEQUENTIAL READ:** Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “roll over” and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 7-3).

**Figure 7-3.** Sequential Read



## 8. AT24C256B Ordering Codes

| Ordering Code | Voltage | Package | Operation Range |
|---|---|---|---|
| AT24C256B-PU (Bulk Form Only) | 1.8 | 8P3 | Lead-free/Halogen-free Industrial Temperature (–40°C to 85°C) |
| AT24C256BN-SH-B[1] (NiPdAu Lead Finish) | 1.8 | 8S1 | |
| AT24C256BN-SH-T[2] (NiPdAu Lead Finish) | 1.8 | 8S1 | |
| AT24C256BW-SH-B[1] (NiPdAu Lead Finish) | 1.8 | 8S2 | |
| AT24C256BW-SH-T[2] (NiPdAu Lead Finish) | 1.8 | 8S2 | |
| AT24C256B-TH-B[1] (NiPdAu Lead Finish) | 1.8 | 8A2 | |
| AT24C256B-TH-T[2] (NiPdAu Lead Finish) | 1.8 | 8A2 | |
| AT24C256BY7-YH-T[2] (NiPdAu Lead Finish) | 1.8 | 8Y7 | |
| AT24C256BU2-UU-T[2] | 1.8 | 8U2-1 | |
| AT24C256B-W-11 | 1.8 | Die Sale | Industrial Temperature (–40°C to 85°C) |

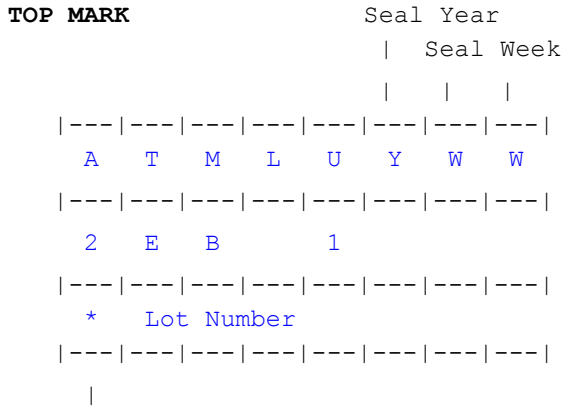
Notes:
1. "-B" denotes bulk.
2. "-T" denotes tape and reel. SOIC = 4K per reel. TSSOP and dBGA2 = 5K per reel. SAP = 3K per reel. EIAJ = 2K per reel.
3. Available in tape & reel and wafer form; order as SL788 for inkless wafer form. Bumped die available upon request. Please contact Serial Interface Marketing.

| Package Type | |
|---|---|
| **8P3** | 8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| **8S1** | 8-lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC) |
| **8S2** | 8-lead, 0.200" Wide, Plastic Gull Wing Small Outline Package (EIAJ SOIC) |
| **8U2-1** | 8-ball, die Ball Grid Array Package (dBGA2) |
| **8A2** | 8-lead, 4.40 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP) |
| **8Y7** | 8-lead, 6.00 mm x 4.90 mm Body, Ultra Thin, Dual Footprint, Non-leaded, Small Array Package (SAP) |
| **Options** | |
| **–1.8** | Low-voltage (1.8V to 5.5V) |

# 9. Part Marking Scheme

## 8-PDIP

**TOP MARK**




Y = SEAL YEAR

| | |
|---|---|
| 6: 2006 | 0: 2010 |
| 7: 2007 | 1: 2011 |
| 8: 2008 | 2: 2012 |
| 9: 2009 | 3: 2013 |

WW = SEAL WEEK

02 = Week 2
04 = Week 4
:: : :::: :
:: : :::: ::
50 = Week 50
52 = Week 52

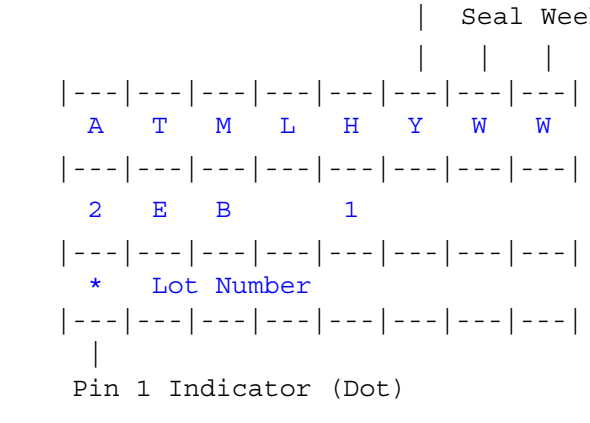
Lot Number to Use ALL Characters in Marking

**BOTTOM MARK**

No Bottom Mark

## 8-SOIC

**TOP MARK**




Y = SEAL YEAR

| | |
|---|---|
| 6: 2006 | 0: 2010 |
| 7: 2007 | 1: 2011 |
| 8: 2008 | 2: 2012 |
| 9: 2009 | 3: 2013 |

WW = SEAL WEEK

02 = Week 2
04 = Week 4
:: : :::: :
:: : :::: ::
50 = Week 50
52 = Week 52

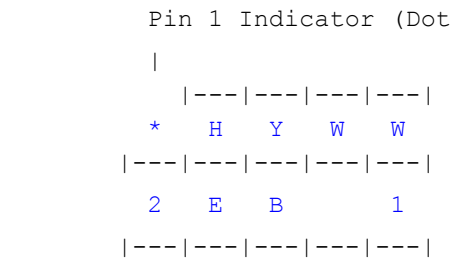
Lot Number to Use ALL Characters in Marking

**BOTTOM MARK**

No Bottom Mark

## 8-TSSOP

**TOP MARK**




Y = SEAL YEAR

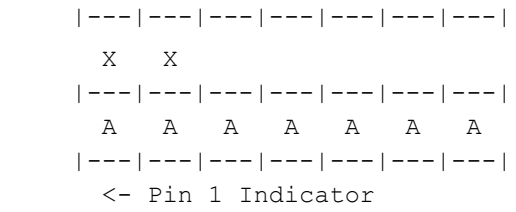
| | |
|---|---|
| 6: 2006 | 0: 2010 |
| 7: 2007 | 1: 2011 |
| 8: 2008 | 2: 2012 |
| 9: 2009 | 3: 2013 |

WW = SEAL WEEK

02 = Week 2
04 = Week 4
:: : :::: :
:: : :::: ::
50 = Week 50
52 = Week 52

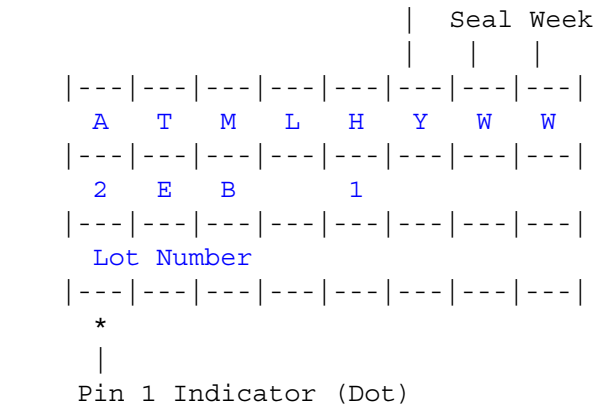
**BOTTOM MARK**

XX = Country of Origin




## 8-Ultra Thin SAP

TOP MARK




Y = SEAL YEAR

| | |
|---|---|
| 6: 2006 | 0: 2010 |
| 7: 2007 | 1: 2011 |
| 8: 2008 | 2: 2012 |
| 9: 2009 | 3: 2013 |

WW = SEAL WEEK

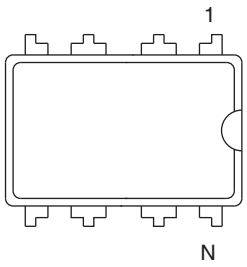
02 = Week 2
04 = Week 4
:: : :::: :
:: : :::: ::
50 = Week 50
52 = Week 52

## dBGA2

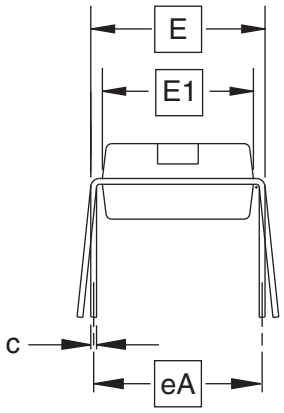
```
TOP MARK

LINE 1------->     2EBU
LINE 2------->     YMTC
                  |<--  Pin 1 This Corner


 Y = ONE DIGIT YEAR CODE
4: 2004   7: 2007
5: 2005   8: 2008
6: 2006   9: 2009

M = SEAL MONTH (USE ALPHA DESIGNATOR A-L)
  A = JANUARY
  B = FEBRUARY
  " " """""""
  J = OCTOBER
  K = NOVEMBER
  L = DECEMBER


    TC = TRACE CODE
```

## 10. Packaging Information

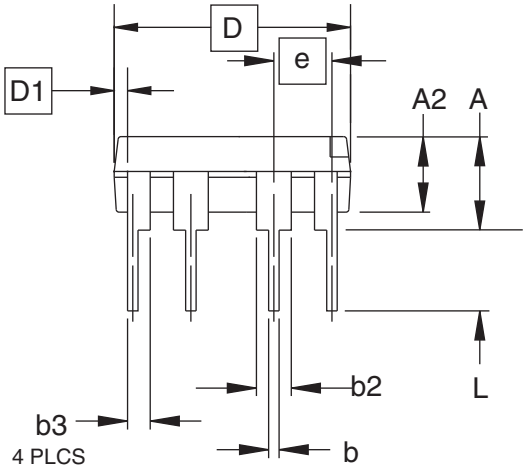
### 8P3 – PDIP




Top View




End View




Side View

**COMMON DIMENSIONS**
(Unit of Measure = inches)

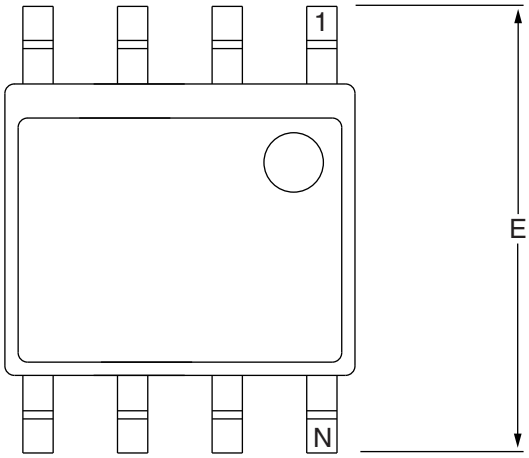
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | – | – | 0.210 | 2 |
| A2 | 0.115 | 0.130 | 0.195 | |
| b | 0.014 | 0.018 | 0.022 | 5 |
| b2 | 0.045 | 0.060 | 0.070 | 6 |
| b3 | 0.030 | 0.039 | 0.045 | 6 |
| c | 0.008 | 0.010 | 0.014 | |
| D | 0.355 | 0.365 | 0.400 | 3 |
| D1 | 0.005 | – | – | 3 |
| E | 0.300 | 0.310 | 0.325 | 4 |
| E1 | 0.240 | 0.250 | 0.280 | 3 |
| e | 0.100 BSC | | | |
| eA | 0.300 BSC | | | 4 |
| L | 0.115 | 0.130 | 0.150 | 2 |

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA, for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

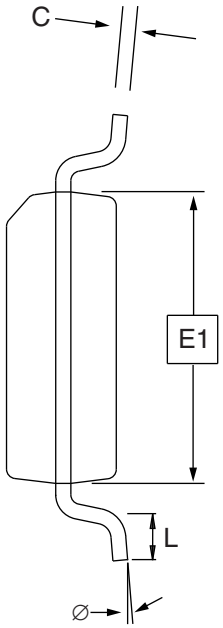
01/09/02

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **8P3**, 8-lead, 0.300" Wide Body, Plastic Dual In-line Package (PDIP) | 8P3 | B |

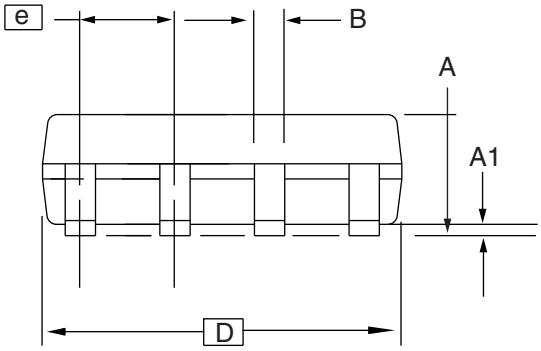
## 8S1 – JEDEC SOIC




Top View




End View




Side View

**COMMON DIMENSIONS**
(Unit of Measure = mm)

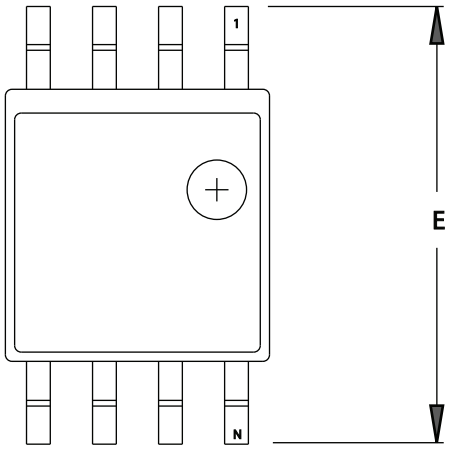
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 1.35 | – | 1.75 | |
| A1 | 0.10 | – | 0.25 | |
| b | 0.31 | – | 0.51 | |
| C | 0.17 | – | 0.25 | |
| D | 4.80 | – | 5.00 | |
| E1 | 3.81 | – | 3.99 | |
| E | 5.79 | – | 6.20 | |
| e | 1.27 BSC | | | |
| L | 0.40 | – | 1.27 | |
| ∅ | 0° | – | 8° | |

Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

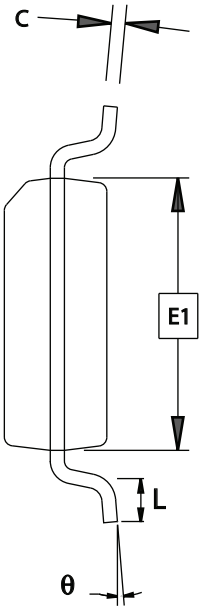
10/7/03

| | | | |
|---|---|---|---|
| 1150 E. Cheyenne Mtn. Blvd.<br>Colorado Springs, CO 80906 | **TITLE**<br>**8S1**, 8-lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC) | **DRAWING NO.**<br>8S1 | **REV.**<br>B |

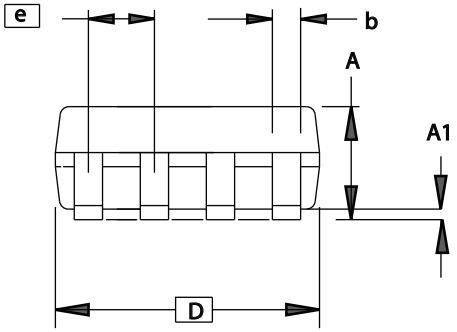
## 8S2 - EIAJ SOIC




TOP VIEW




END VIEW




SIDE VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

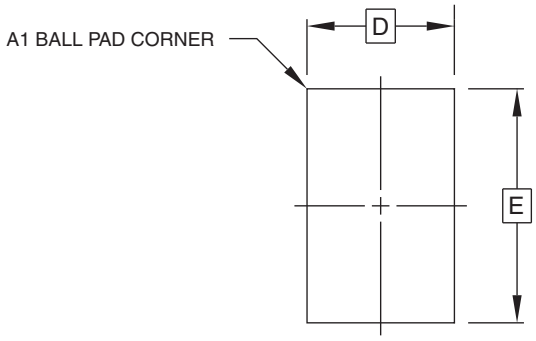
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 1.70 | | 2.16 | |
| A1 | 0.05 | | 0.25 | |
| b | 0.35 | | 0.48 | 5 |
| C | 0.15 | | 0.35 | 5 |
| D | 5.13 | | 5.35 | |
| E1 | 5.18 | | 5.40 | 2, 3 |
| E | 7.70 | | 8.26 | |
| L | 0.51 | | 0.85 | |
| θ | 0° | | 8° | |
| e | 1.27 BSC | | | 4 |

Notes:
1. This drawing is for general information only; refer to EIAJ Drawing EDR-7320 for additional information.
2. Mismatch of the upper and lower dies and resin burrs aren't included.
3. It is recommended that upper and lower cavities be equal. If they are different, the larger dimension shall be regarded.
4. Determines the true geometric position.
5. Values b,C apply to plated terminal. The standard thickness of the plating layer shall measure between 0.007 to .021 mm.

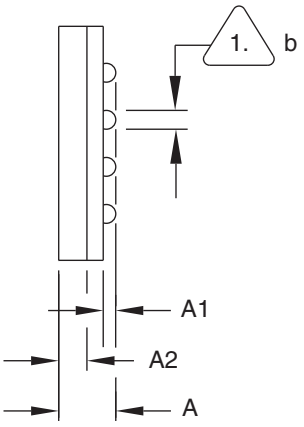
4/7/06

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | 8S2, 8-lead, 0.209" Body, Plastic Small Outline Package (EIAJ) | 8S2 | D |

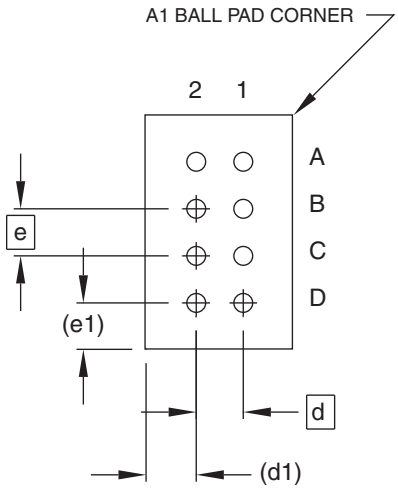
## 8U2-1 – dBGA2




Top View




Side View




Bottom View
8 Solder Balls

1. Dimension 'b' is measured at the maximum solder ball diameter.

This drawing is for general information only.

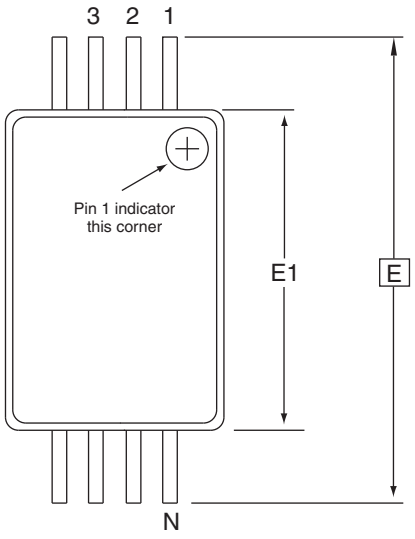
**COMMON DIMENSIONS**
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 0.81 | 0.91 | 1.00 | |
| A1 | 0.15 | 0.20 | 0.25 | |
| A2 | 0.40 | 0.45 | 0.50 | |
| b | 0.25 | 0.30 | 0.35 | 1 |
| D | | 2.35 BSC | | |
| E | | 3.73 BSC | | |
| e | | 0.75 BSC | | |
| e1 | | 0.74 REF | | |
| d | | 0.75 BSC | | |
| d1 | | 0.80 REF | | |

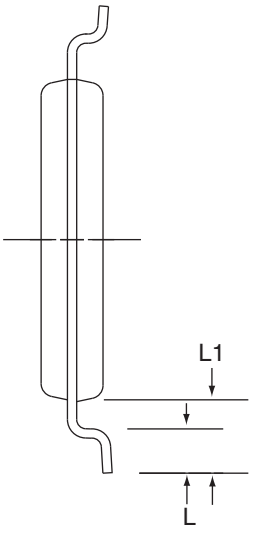
6/24/03

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 1150 E. Cheyenne Mtn. Blvd.<br>Colorado Springs, CO 80906 | **8U2-1,** 8-ball, 2.35 x 3.73 mm Body, 0.75 mm pitch,<br>Small Die Ball Grid Array Package (dBGA2) | PO8U2-1 | A |

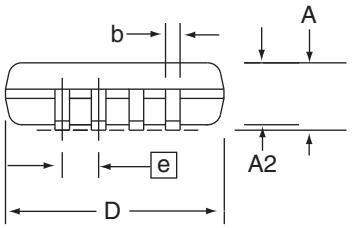
## 8A2 – TSSOP




Top View




End View




Side View

**COMMON DIMENSIONS**
(Unit of Measure = mm)

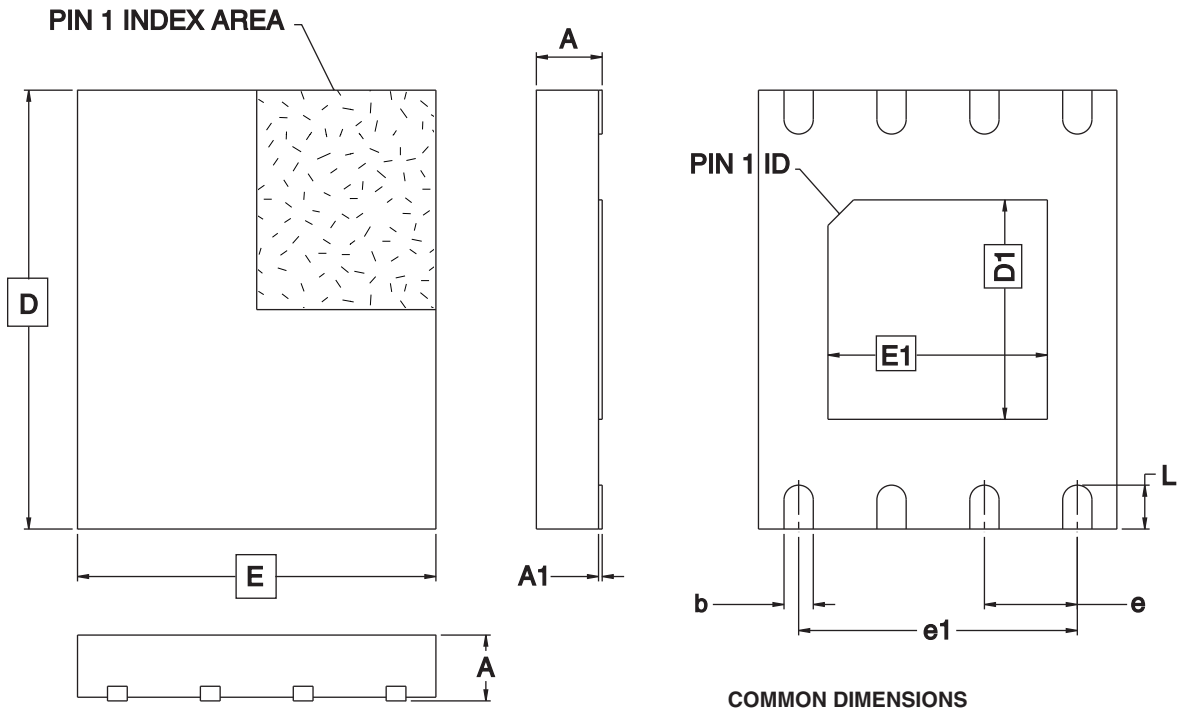
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| D | 2.90 | 3.00 | 3.10 | 2, 5 |
| E | | 6.40 BSC | | |
| E1 | 4.30 | 4.40 | 4.50 | 3, 5 |
| A | – | – | 1.20 | |
| A2 | 0.80 | 1.00 | 1.05 | |
| b | 0.19 | – | 0.30 | 4 |
| e | | 0.65 BSC | | |
| L | 0.45 | 0.60 | 0.75 | |
| L1 | | 1.00 REF | | |

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
5. Dimension D and E1 to be determined at Datum Plane H.

5/30/02

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **8A2**, 8-lead, 4.4 mm Body, Plastic<br>Thin Shrink Small Outline Package (TSSOP) | 8A2 | B |

## 8Y7 – SAP




**COMMON DIMENSIONS**
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | – | – | 0.60 | |
| A1 | 0.00 | – | 0.05 | |
| D | 5.80 | 6.00 | 6.20 | |
| E | 4.70 | 4.90 | 5.10 | |
| D1 | 3.30 | 3.40 | 3.50 | |
| E1 | 3.90 | 4.00 | 4.10 | |
| b | 0.35 | 0.40 | 0.45 | |
| e | 1.27 TYP | | | |
| e1 | 3.81 REF | | | |
| L | 0.50 | 0.60 | 0.70 | |

10/13/05

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 1150 E. Cheyenne Mtn. Blvd.<br>Colorado Springs, CO 80906 | **8Y7**, 8-lead (6.00 x 4.90 mm Body) Ultra-Thin SOIC Array Package (UTSAP) Y7 | 8Y7 | B |

## Revision History

| Doc. Rev. | Date | Comments |
|---|---|---|
| 5279C | 3/2009 | Changed the Vcc to 5.5V in the test condition for Isb1 |
| 5279B | 3/2008 | Format changes to document |
| 5279A | 1/2008 | AT24C256B product with date code 2008 work week 14 (814) or later supports 5Vcc operation<br>Initial document release |

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