Data Sheet | September 17, 2008 | FN6768.0

QFN Packaged, ±15kV ESD Protected, +2.7V to +3.6V, 250kbps, RS-232 Transmitters/Receivers with Separate Logic Supply Pin

The Intersil ISL324xE devices are 2.7V to 3.6V powered RS-232 transmitters/receivers which meet EIA/TIA-232 and V.28/V.24 specifications, even at V_{CC} = 3.0V. Additionally, they provide ±15kV ESD protection (IEC61000-4-2 Air Gap and Human Body Model) on transmitter outputs and receiver inputs (RS-232 pins). Targeted applications are POS systems, and notebook and laptop computers where the low operational, and even lower standby, power consumption is critical. Efficient on-chip charge pumps, coupled with manual and automatic power-down functions, reduce the standby supply current to a 0.5µA trickle. Tiny 5mmx5mm **Quad Flat No-Lead** (QFN) packaging and the use of small, low value capacitors ensure board space savings as well. Data rates greater than 250kbps are guaranteed at worst case load conditions.

ISL324xE are 3 driver, 5 receiver devices that, coupled with the 5x5 QFN package, provide the industry's smallest, lowest power complete serial port. The 5x5 QFN requires 60% less board area than a 28 Ld TSSOP, and is nearly 20% thinner. These devices also include a noninverting always-active receiver for "wake-up" capability.

The **ISL3243E** features an ***automatic powerdown*** function that powers down the on-chip power supply and driver circuits. This occurs when an attached peripheral device is shut off or the RS-232 cable is removed, conserving system power automatically without changes to the hardware or operating system. It powers up again when a valid RS-232 voltage is applied to any receiver input.

The ISL324xE feature a V_L pin that adjusts the logic pin (see "Pin Descriptions" on page 3) output levels and input thresholds to values compatible with the V_{CC} powering the external logic (e.g., a UART).

Table 1 summarizes the features of the ISL324xE.

Features

- V_L Pin for Compatibility in Mixed Voltage Systems Adjusts Logic Output Levels and Input Thresholds for Compatibility with Lower Supply Voltage Logic
- Parameters Specified for 10% Tolerance Supplies and Full Industrial Temp Range
- Pb-free Small QFN (5mmx5mm) Package is 60% Smaller than a 28 Lead TSSOP
- ESD Protection for RS-232 I/O Pins to ±15kV (IEC61000)
- Meets EIA/TIA-232 and V.28/V.24 Specifications at 3V
- RS-232 Compatible with V_{CC} = 2.7V
- On-Chip Voltage Converters Require Only Four External 0.1µF Capacitors
- Manual and Automatic Power-down Features
- Receiver Hysteresis for Improved Noise Immunity
- Guaranteed Minimum Data Rate 250kbps
- Low Supply Current in Power-down State 0.5µA
- Pb-Free (RoHS compliant)

Applications

- Any Space Constrained System Requiring RS-232 Ports
  - Battery Powered, Hand-Held, and Portable Equipment
  - POS Systems and Scanners
  - Laptop Computers, Notebooks
  - GPS Receivers
- Mixed Voltage Serial Ports

Related Literature

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices
- "Technical Brief TB379 "Thermal Characterization of Packages for ICs"
- Technical Brief TB389 "PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages"

TABLE 1. SUMMARY OF FEATURES

PART NUMBER	NO. OF Tx.	NO. OF Rx.	LOGIC SUPPLY (V_L) PIN?	NO. OF MONITOR Rx. (R_{OUTB})	DATA RATE (kbps)	Rx. ENABLE FUNCTION?	Pb-FREE?	MANUAL POWER-DOWN?	AUTOMATIC POWERDOWN FUNCTION?
ISL3241E	3	5	YES	2	250	YES	YES	YES	NO
ISL3243E	3	5	YES	1	250	NO	YES	YES	YES

Ordering Information

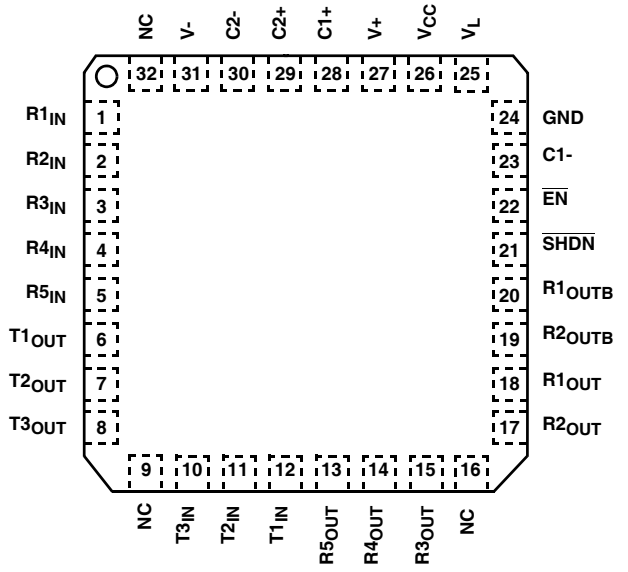
PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL3241EIRZ	ISL3241 EIRZ	-40 to +85	32 Ld 5X5 QFN	L32.5x5B
ISL3241EIRZ-T*	ISL3241 EIRZ	-40 to +85	32 Ld 5X5 QFN (Tape & Reel)	L32.5x5B
ISL3243EIRZ	ISL3243 EIRZ	-40 to +85	32 Ld 5X5 QFN	L32.5x5B
ISL3243EIRZ-T*	ISL3243 EIRZ	-40 to +85	32 Ld 5X5 QFN (Tape & Reel)	L32.5x5B

* Please refer to TB347 for details on reel specifications.

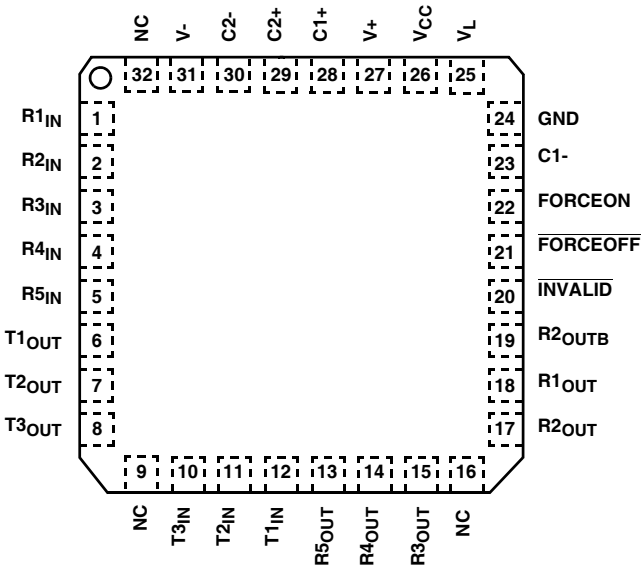
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020

Pinouts

ISL3241E
(32 LEAD QFN)
TOP VIEW



ISL3243E
(32 LEAD QFN)
TOP VIEW

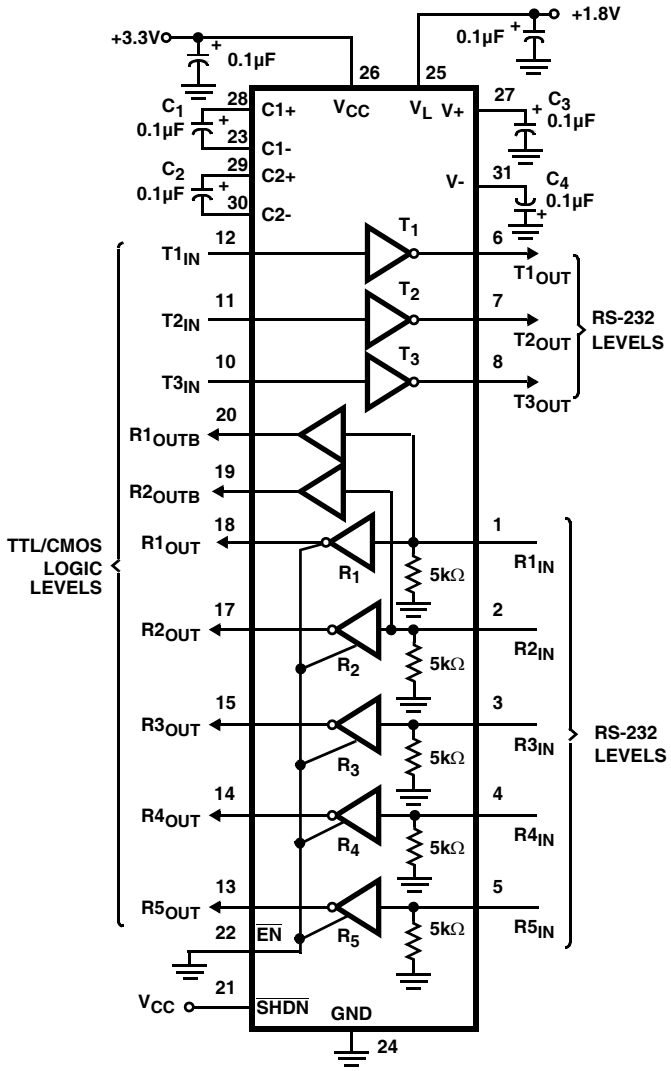


Pin Descriptions

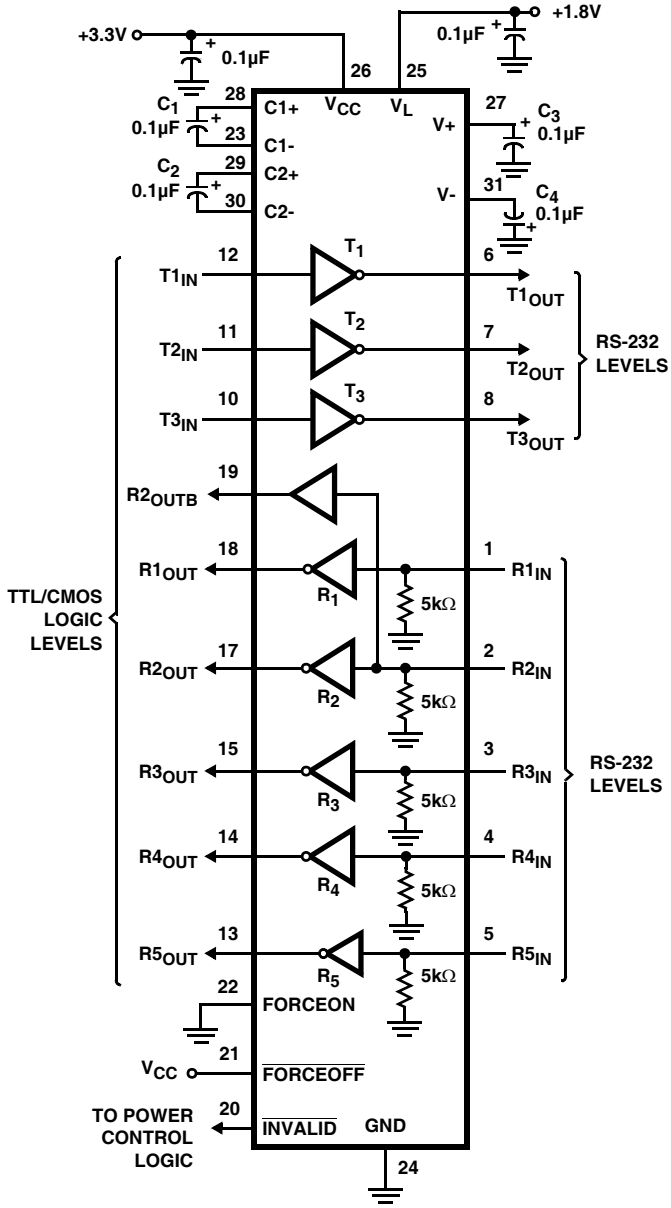
PIN	FUNCTION
V_{CC}	System power supply input (2.7V to 3.6V).
V_L	Logic power supply. Sets the V_{OH} of all the logic outputs and the switching point of all logic inputs. Keep V_L greater than 1.6V (1.8V - 10%) and less than or equal to V_{CC}. Power up V_L after V_{CC}
V+	Internally generated positive transmitter supply (typically +5.5V).
V-	Internally generated negative transmitter supply (typically -5.5V).
GND	Ground connection.
C1+	External capacitor (voltage doubler) is connected to this lead.
C1-	External capacitor (voltage doubler) is connected to this lead.
C2+	External capacitor (voltage inverter) is connected to this lead.
C2-	External capacitor (voltage inverter) is connected to this lead.
T_{IN}	TTL/CMOS compatible transmitter Inputs. The V_L voltage sets the input switching point.
T_{OUT}	±15kV ESD Protected, RS-232 level (nominally ±5.5V) transmitter outputs.
R_{IN}	±15kV ESD Protected, RS-232 compatible receiver inputs.
R_{OUT}	TTL/CMOS level receiver outputs. Swings between GND and V_L.
R_{OUTB}	TTL/CMOS level, noninverting, always enabled receiver outputs. Swings between GND and V_L.
$\overline{\text{INVALID}}$	Active low output that indicates if no valid RS-232 levels are present on any receiver input. Swings between GND and V_L.
$\overline{\text{FORCEOFF}}$	Active low to shut down transmitters and on-chip power supply. This overrides any automatic circuitry and FORCEON (see Table 2). The V_L voltage sets the input switching point.
FORCEON	Active high input to override automatic powerdown circuitry thereby keeping transmitters active. ($\overline{\text{FORCEOFF}}$ must be high). The V_L voltage sets the input switching point.
$\overline{\text{EN}}$	Active low receiver enable control. The V_L voltage sets the input switching point.
$\overline{\text{SHDN}}$	Active low input to shut down transmitters and on-board power supply, to place device in low power mode. The V_L voltage sets the input switching point.
NC	No Connection

Typical Operating Circuits

ISL3241E



ISL3243E



Absolute Maximum Ratings

V_{CC} to Ground . . . . . -0.3V to 6V
V_L to Ground . . . . . -0.3V to (V_{CC} + 0.3V)
V+ to Ground . . . . . -0.3V to 7V
V- to Ground. . . . . +0.3V to -7V
V+ to V- 14V
Input Voltages
T_{IN}, $\overline{FORCEOFF}$, FORCEON, $\overline{EN}$, $\overline{SHDN}$ . . . . . -0.3V to 6V
R_{IN} . . . . . ±25V
Output Voltages
T_{OUT} . . . . . ±13.2V
R_{OUT}, $\overline{INVALID}$. . . . . -0.3V to (V_L + 0.3V)
Short Circuit Duration
T_{OUT} . . . . . Continuous
ESD Rating . . . . . See Specification Table

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32 Ld QFN Package.	31	2.5

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range. . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range. . . . . -40°C to 85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379 for details.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Test Conditions: V_{CC} = 3V to 3.6V, V_L = 1.8V ±10%, C_1 to C_4 = 0.1µF, Unless Otherwise Specified. Typicals are at T_A = +25°C, V_{CC} = 3.3V, V_L = 1.8V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS		TEMP (°C)	MIN (Note 3)	TYP	MAX (Note 3)	UNITS
DC CHARACTERISTICS							
Operating Voltage Range			Full	2.7	-	3.6	V
Supply Current, Automatic Powerdown	All R_{IN} Open, FORCEON = GND, $\overline{FORCEOFF}$ = V_L V_L = V_{CC} (ISL3243E Only)		Full	-	0.5	3	µA
Supply Current, Powerdown	All R_{IN} Open, $\overline{FORCEOFF}$ = $\overline{SHDN}$ = GND, V_L = V_{CC}		Full	-	0.5	3	µA
Supply Current, Automatic Powerdown Disabled	All Outputs Unloaded, FORCEON = $\overline{FORCEOFF}$ = $\overline{SHDN}$ = V_L, V_{CC} = V_L = 3.0V		25	-	0.3	1.0	mA
			Full	-	0.3	1.5	mA
LOGIC AND TRANSMITTER INPUTS; RECEIVER AND LOGIC OUTPUTS							
Input Logic Threshold Low	T_{IN}, FORCEON, $\overline{FORCEOFF}$, $\overline{EN}$, $\overline{SHDN}$		Full	-	-	0.5	V
		V_L = V_{CC} = 3V	Full	-	-	0.8	V
Input Logic Threshold High	T_{IN}, FORCEON, $\overline{FORCEOFF}$, $\overline{EN}$, $\overline{SHDN}$		Full	1.25	-	-	V
		V_L = V_{CC} = 3.6V	Full	2.0	-	-	V
Input Leakage Current	T_{IN}, FORCEON, $\overline{FORCEOFF}$, $\overline{EN}$, $\overline{SHDN}$		Full	-	±0.01	±1.0	µA
Output Leakage Current	$\overline{FORCEOFF}$ = GND (ISL3243E) or $\overline{EN}$ = V_L (ISL3241E)		Full	-	±0.05	±10	µA
Output Voltage Low (See Figure 21)	I_{OUT} = 250µA, R_{OUT}, R_{OUTB}, $\overline{INVALID}$		Full	-	-	0.45	V
	I_{OUT} = 1.6mA, V_L = V_{CC}, R_{OUT}, R_{OUTB}, $\overline{INVALID}$		Full	-	-	0.4	V
Output Voltage High (See Figure 21)	I_{OUT} = -250µA, R_{OUT}, R_{OUTB}, $\overline{INVALID}$		Full	V_L - 0.25	V_L - 0.1	-	V
	I_{OUT} = -1.0mA, V_L = V_{CC}, R_{OUT}, R_{OUTB}, $\overline{INVALID}$		Full	V_L - 0.6	V_L - 0.1	-	V
AUTOMATIC POWERDOWN (ISL3243E Only, FORCEON = GND, $\overline{FORCEOFF}$ = V_L)							
Receiver Input Thresholds to Enable Transmitters	ISL3243E Powers Up (See Figure 10)		Full	-2.7	-	2.7	V
Receiver Input Thresholds to Disable Transmitters	ISL3243E Powers Down (See Figure 10)		Full	-0.3	-	0.3	V
Receiver Threshold to Transmitters Enabled Delay (t_{WU})			25	-	20	-	µs

Electrical Specifications Test Conditions: V_{CC} = 3V to 3.6V, V_L = 1.8V ±10%, C_1 to C_4 = 0.1µF, Unless Otherwise Specified. Typicals are at T_A = +25°C, V_{CC} = 3.3V, V_L = 1.8V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS		TEMP (°C)	MIN (Note 3)	TYP	MAX (Note 3)	UNITS
Receiver Positive or Negative Threshold to INVALID High Delay (t_{INVH})			25	-	0.7	-	µs
Receiver Positive or Negative Threshold to INVALID Low Delay (t_{INVL})			25	-	20	-	µs
RECEIVER INPUTS							
Input Voltage Range			Full	-25	-	25	V
Input Threshold Low	$V_{CC} \geq 2.7V$		Full	-	-	0.6	V
	$V_{CC} \geq 3V$		Full	-	-	0.8	V
Input Threshold High			Full	2.0	1.5	-	V
Input Hysteresis			25	-	0.5	-	V
Input Resistance			Full	3	5	7	kΩ
TRANSMITTER OUTPUTS							
Output Voltage Swing (V_O)	All Transmitter Outputs Loaded with 3kΩ to Ground		Full	±5.0	±5.4	-	V
		V_{CC} = 2.7V	Full	±4.0	±4.7	-	V
Output Resistance	$V_{CC} = V_L = V+ = V- = 0V$, Transmitter Output = ±2V		Full	300	10M	-	Ω
Output Short-Circuit Current			Full	-	±35	±60	mA
Output Leakage Current	V_{OUT} = ±12V, $V_{CC} = V_L$ = 0V or 3V to 3.6V, Automatic Powerdown or $\overline{FORCEOFF}$ = $\overline{SHDN}$ = GND		Full	-	-	±25	µA
TIMING CHARACTERISTICS							
Maximum Data Rate	R_L = 3kΩ, C_L = 1000pF, One Transmitter Switching		Full	250	400	-	kbps
	R_L = 3kΩ, C_L = 200pF, V_{CC} = 3.15V, One Transmitter Switching		Full	-	1.3	-	Mbps
Receiver Propagation Delay	Receiver Input to Receiver Output, C_L = 30pF, R_{IN} = ±3V (See Figure 2)	t_{PHL}	25	-	0.23	0.55	µs
			Full	-	0.26	0.6	µs
		t_{PLH}	25	-	0.16	0.55	µs
			Full	-	0.18	0.6	µs
Receiver Skew	$\lvert t_{PHL} - t_{PLH} \rvert$		25	-	70	300	ns
			Full	-	80	350	ns
Transmitter Propagation Delay	Transmitter Input to Transmitter Output, C_L = 1000pF, R_L = 3kΩ (See Figure 1) (Note 4)	t_{PHL}	25	-	0.7	1.5	µs
			Full	-	0.8	1.7	µs
		t_{PLH}	25	-	0.7	1.5	µs
			Full	-	0.8	1.7	µs
Transmitter Skew	$\lvert t_{PHL} - t_{PLH} \rvert$		25	-	20	500	ns
			Full	-	20	550	ns
Receiver Output Enable Time	From $\overline{EN}$ or $\overline{FORCEOFF}$, $V_L = V_{CC}$, R_L = 1kΩ, C_L = 15pF (See Figure 3)		25	-	120	-	ns
Receiver Output Disable Time			25	-	200	-	ns
Transmitter Output Enable Time From Powerdown	From $\overline{SHDN}$ or $\overline{FORCEOFF}$, R_L = 3kΩ, C_L = 1000pF		25	-	20	-	µs
Transition Region Slew Rate	V_{CC} = 3V to 3.6V, R_L = 3kΩ to 7kΩ, Measured From 3V to -3V or -3V to 3V	C_L = 150pF to 2500pF	25	4	12	30	V/µs
			Full	4	11	30	V/µs
		C_L = 150pF to 1000pF	25	6	18	30	V/µs
			Full	6	17	30	V/µs

Electrical Specifications Test Conditions: V_{CC} = 3V to 3.6V, V_L = 1.8V ±10%, C_1 to C_4 = 0.1µF, Unless Otherwise Specified. Typicals are at T_A = +25°C, V_{CC} = 3.3V, V_L = 1.8V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 3)	TYP	MAX (Note 3)	UNITS
ESD PERFORMANCE						
RS-232 Pins (T_{OUT}, R_{IN})	Human Body Model	25	-	±15	-	kV
	IEC61000-4-2 Contact Discharge	25	-	±8	-	kV
	IEC61000-4-2 Air Gap Discharge	25	-	±15	-	kV
All Pins	Human Body Model	25	-	±2	-	kV
	Machine Model	25	-	±200	-	V

NOTES:

3. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
4. Transmitter propagation delays are measured at the transmitter output 0V crossing points.

Test Circuits and Waveforms

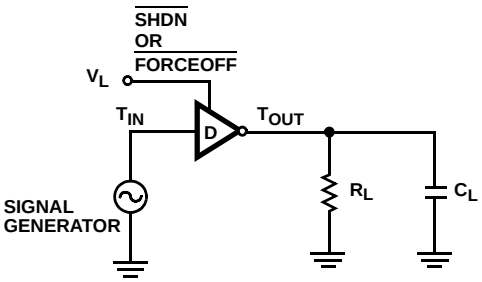


FIGURE 1A. TEST CIRCUIT

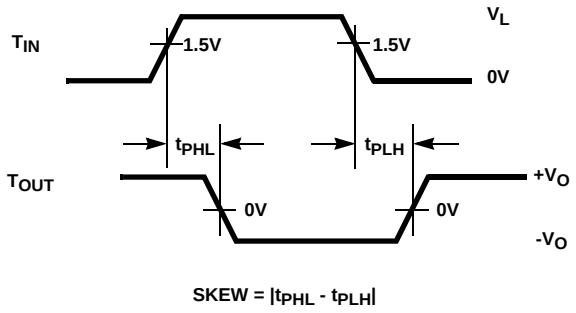


FIGURE 1B. MEASUREMENT POINTS

FIGURE 1. DRIVER PROPAGATION DELAY AND SKEW

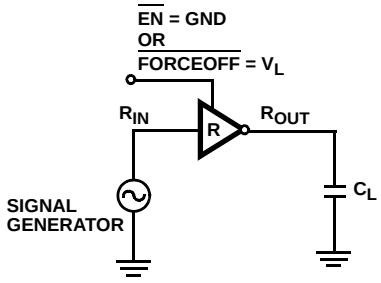


FIGURE 2A. TEST CIRCUIT

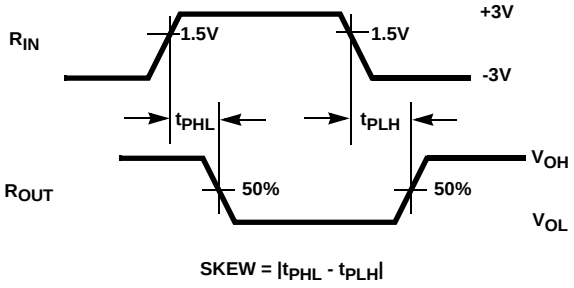
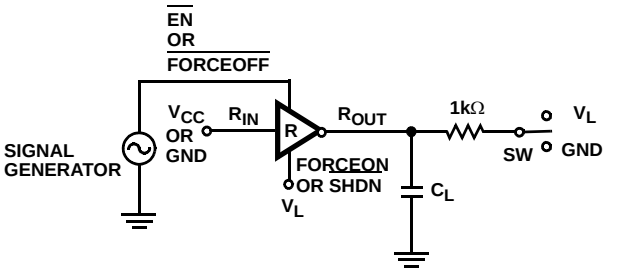


FIGURE 2B. MEASUREMENT POINTS

FIGURE 2. RECEIVER PROPAGATION DELAY AND SKEW

Test Circuits and Waveforms (Continued)



PARAMETER	R_{IN}	SW
t_{PHZ} and t_{PZH}	GND	GND
t_{PLZ} and t_{PZL}	V_{CC}	V_L

FIGURE 3A. TEST CIRCUIT

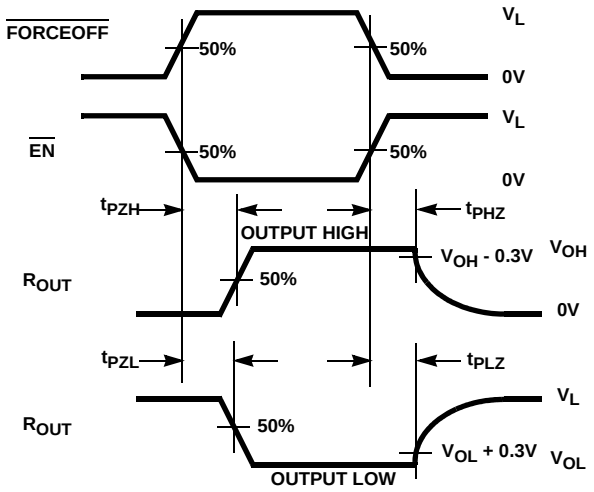


FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. RECEIVER ENABLE AND DISABLE TIMES

Detailed Description

The ISL324xE operate from a single +2.7V to +3.6V supply, guarantee a 250kbps minimum data rate, require only four small external 0.1µF capacitors, feature low power consumption, and meet all EIA RS-232 and V.28 specifications even with V_{CC} = 3.0V. The circuit is divided into three sections: The charge pump, the transmitters, and the receivers.

Charge-Pump

Intersil's new ISL324xE devices utilize regulated on-chip dual charge pumps as voltage doublers, and voltage inverters to generate ±5.5V transmitter supplies from a V_{CC} supply as low as 3.0V. This allows them to maintain RS-232 compliant output levels over the ±10% tolerance range of 3.3V powered systems. The efficient on-chip power supplies require only four small, external 0.1µF capacitors for the voltage doubler and inverter functions. The charge pumps operate discontinuously (i.e., they turn off as soon as the V+ and V- supplies are pumped up to the nominal values), resulting in significant power savings.

Transmitters

The transmitters are proprietary, low dropout, inverting drivers that translate logic input levels to EIA/TIA-232 output levels. Coupled with the on-chip ±5.5V supplies, these transmitters deliver true RS-232 levels over a wide range of single supply system voltages.

All transmitter outputs disable and assume a high impedance state when the device enters the power-down mode (see Table 2). These outputs may be driven to ±12V when disabled.

The devices guarantee a 250kbps data rate for full load conditions (3kΩ and 1000pF), $V_{CC} \geq 3.0V$, with one transmitter operating at full speed. Under more typical conditions of $V_{CC} \geq 3.3V$, R_L = 3kΩ, and C_L = 200pF, one transmitter easily operates at greater than 1Mbps.

The transmitter input switching threshold is set by the voltage applied to the V_L pin, so tying V_L to a voltage lower than V_{CC} reduces the Tx input V_{IH} and V_{IL} to values compatible with logic ICs (e.g., UARTs and µcontrollers) powered by the V_L voltage (see Figure 9 and Table 3). Transmitter inputs float if left unconnected (there are no pull-up resistors), and may cause supply current increases. Connect unused inputs to GND for the best performance.

Receivers

All the ISL324xE devices contain standard inverting receivers that three-state via the $\overline{EN}$ or $\overline{FORCEOFF}$ control lines. Additionally, these products include noninverting "monitor" receivers (denoted by the R_{OUTB} label) that are always active, regardless of the state of any control lines. All the receivers convert RS-232 signals to CMOS output levels, swinging between GND and V_L, and accept inputs up to ±25V while presenting the required 3kΩ to 7kΩ input impedance (see Figure 4) even if the power is off (V_{CC} = 0V). The receivers' Schmitt trigger input stage uses hysteresis to increase noise immunity and decrease errors due to slow input signal transitions.

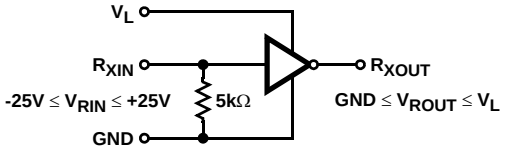


FIGURE 4. INVERTING RECEIVER CONNECTIONS

The ISL3241E inverting receivers disable only when $\overline{EN}$ is driven high. ISL3243E receivers disable during forced (manual) powerdown, but not during automatic powerdown (see Table 2).

ISL324xE monitor receivers remain active even during manual powerdown, making them extremely useful for Ring Indicator monitoring. Standard receivers driving powered down peripherals must be disabled to prevent current flow through the peripheral's protection diodes (see Figures 5 and 6). This renders them useless for wake up functions, but the corresponding monitor receiver can be dedicated to this task as shown in Figure 6.

Low Power Operation

These 3V devices require a nominal supply current of 0.3mA, even at V_{CC} = 3.6V, during normal operation (not in power-down mode). This is considerably less than the 5mA to 11mA current required by comparable 5V RS-232 devices, allowing users to reduce system power simply by switching to this new family.

TABLE 2. POWER-DOWN AND ENABLE LOGIC TRUTH TABLE (NOTE: "H" = V_L)

RS-232 SIGNAL PRESENT AT RECEIVER INPUT?	$\overline{\text{SHDN}}$ OR FORCEOFF INPUT	FORCEON INPUT	$\overline{\text{EN}}$ INPUT	TRANSMITTER OUTPUTS	RECEIVER OUTPUTS	R_{OUTB} OUTPUTS	$\overline{\text{INVALID}}$ OUTPUT	MODE OF OPERATION
ISL3241E								
N/A	L	N/A	L	High-Z	Active	Active	N/A	Manual Power-down
N/A	L	N/A	H	High-Z	High-Z	Active	N/A	Manual Power-down w/Rcvr. Disabled
N/A	H	N/A	L	Active	Active	Active	N/A	Normal Operation
N/A	H	N/A	H	Active	High-Z	Active	N/A	Normal Operation w/Rcvr. Disabled
ISL3243E								
NO	H	H	N.A.	Active	Active	Active	L	Normal Operation (Auto Powerdown Disabled)
YES	H	L	N.A.	Active	Active	Active	H	Normal Operation (Auto Power-down Enabled)
NO	H	L	N.A.	High-Z	Active	Active	L	Power-down Due to Auto Power-down Logic
YES	L	X	N.A.	High-Z	High-Z	Active	H	Manual Power-down
NO	L	X	N.A.	High-Z	High-Z	Active	L	Manual Power-down

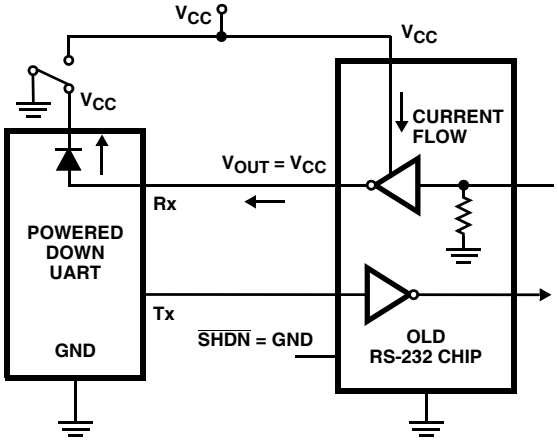


FIGURE 5. POWER DRAIN THROUGH POWERED DOWN PERIPHERAL

Power-down Functionality

The already low current requirement drops significantly when the device enters powerdown mode. In powerdown, supply current drops to less than 1µA, because the on-chip charge pump turns off (V+ collapses to V_{CC}, V- collapses to GND), and the transmitter outputs three-state. Inverting receiver outputs disable only in manual powerdown (ISL3243E) or when $\overline{EN}$ = V_L (ISL3241E); refer to Table 2 for details. This micro-power mode makes the ISL324xE ideal for battery powered and portable applications.

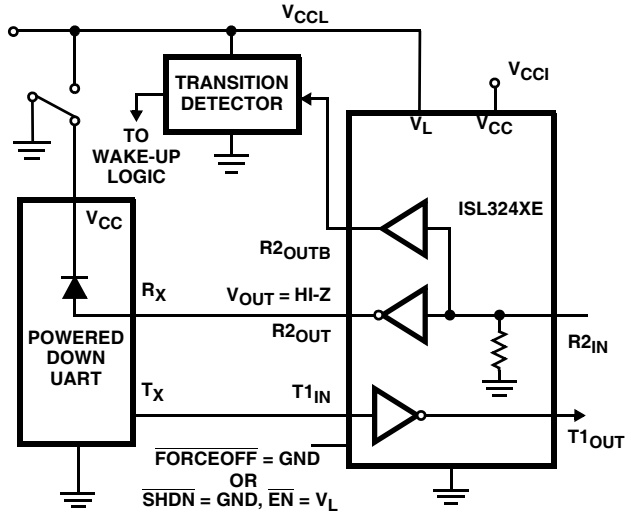


FIGURE 6. DISABLED RECEIVERS PREVENT POWER DRAIN

Software Controlled (Manual) Powerdown

The devices in this family provide pins that allow the user to force the IC into the low power, standby state.

On the ISL3241E, the powerdown control is via a simple shutdown ($\overline{SHDN}$) pin. Driving this pin high enables normal operation, while driving it low forces the IC into it's powerdown state. Connect $\overline{SHDN}$ to V_L if the powerdown function isn't needed. Note that all the receiver outputs remain controlled by $\overline{EN}$ during shutdown (see Table 2). For the lowest power consumption during powerdown, the receivers should also be disabled by driving the $\overline{EN}$ input high (see next section, and Figures 5 and 6).

The ISL3243E utilizes a two pin approach where the FORCEON and $\overline{FORCEOFF}$ inputs determine the IC's mode. For always enabled operation, FORCEON and $\overline{FORCEOFF}$ are both strapped high. To switch between active and powerdown modes, under logic or software control, only the $\overline{FORCEOFF}$ input need be driven. The FORCEON state isn't critical, as $\overline{FORCEOFF}$ dominates over FORCEON. Nevertheless, if strictly manual control over powerdown is desired, the user must strap FORCEON high to disable the automatic powerdown circuitry. ISL3243E inverting (standard) receiver outputs also disable when the device is in manual powerdown, thereby eliminating the possible current path through a shutdown peripheral's input protection diode (see Figures 5 and 6).

Connecting $\overline{FORCEOFF}$ and FORCEON together disables the automatic powerdown feature, enabling them to function as a manual $\overline{SHUTDOWN}$ input (see Figure 7).

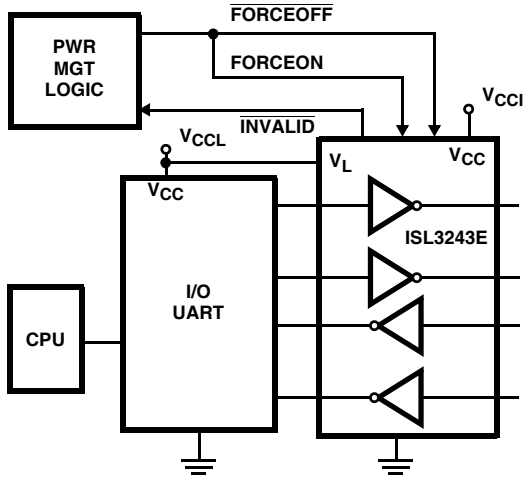


FIGURE 7. CONNECTIONS FOR MANUAL POWERDOWN WHEN NO VALID RECEIVER SIGNALS ARE PRESENT

With any of the above control schemes, the time required to exit powerdown, and resume transmission is only 20µs. A mouse, or other application, may need more time to wake up from shutdown. If automatic power-down is being utilized, the RS-232 device will reenter power-down if valid receiver levels aren't reestablished within 20µs of the ISL3243E powering up. Figure 8 illustrates a circuit that keeps the ISL3243E from initiating automatic power-down for 100ms after powering up. This gives the slow-to-wake peripheral circuit time to reestablish valid RS-232 output levels.

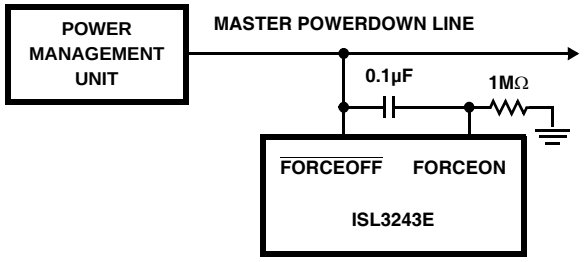


FIGURE 8. CIRCUIT TO PREVENT AUTO POWERDOWN FOR 100ms AFTER FORCED POWERUP

V_L Logic Supply Input

Note: Power-up V_{CC} before powering up the V_L supply.

The ISL324xE feature a V_L pin that powers the logic input and output pins. These pins interface with "logic" devices such as UARTs, ASICs, and µcontrollers, and today most of these devices use power supplies significantly lower than 3.3V. Thus, the logic device's low V_{OH} might not exceed the V_{IH} of a 3.3V powered ISL324xE logic input, or a 3.3V receiver output high level might overdrive and damage the input diodes on an input of a 1.8V powered logic device, as shown in Figure 9. Connecting the V_L pin to the power supply of the logic device (see Figure 9) reduces the ISL324xE's logic input switching points, and limits the receiver output high voltage, to values compatible with the logic device's I/O levels. Tailoring the ISL324XE's logic pin input switching points and output levels to the supply voltage of the UART, ASIC, or µcontroller eliminates the need for a level shifter/translator between the two ICs.

TABLE 3. V_{IH} AND V_{IL} vs V_L FOR V_{CC} = 3.3V

V_L (V)	V_{IH} (V)	V_{IL} (V)
1.6	0.85	0.8
1.8	0.95	0.9
2.5	1.25	1.2

V_L may range from 1.6V to V_{CC}, and Table 3 indicates the ISL324xE's typical V_{IH} and V_{IL} levels for several V_L values. Note that the V_L supply current increases significantly when V_L exceeds V_{CC} (see Figure 20).

If logic translation isn't required, connect V_L to V_{CC}.

$\overline{INVALID}$ Output (ISL3243E Only)

The $\overline{INVALID}$ output always indicates whether or not a valid RS-232 signal (see Figure 10) is present at any of the receiver inputs (see Table 2), giving the user an easy way to

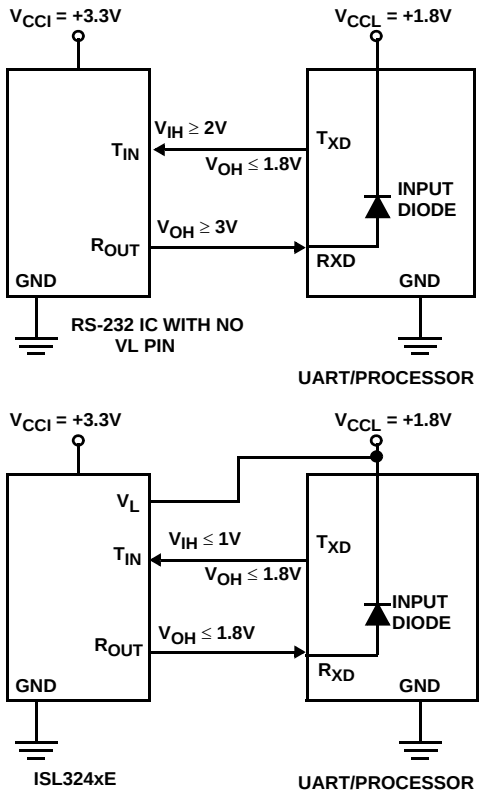


FIGURE 9. USING V_L PIN TO ADJUST LOGIC LEVELS

determine when the interface block should power down. Invalid receiver levels occur whenever the driving peripheral's outputs are shut off (powered down) or when the RS-232 interface cable is disconnected. In the case of a disconnected interface cable where all the receiver inputs are floating (but pulled to GND by the internal receiver pull down resistors), the $\overline{\text{INVALID}}$ logic detects the invalid levels and drives the output low. The power management logic then uses this indicator to power-down the interface block. Reconnecting the cable restores valid levels at the receiver inputs, $\overline{\text{INVALID}}$ switches high, and the power management logic wakes up the interface block. $\overline{\text{INVALID}}$ can also be used to indicate the DTR or RING INDICATOR signal, as long as the other receiver inputs are floating, or driven to GND (as in the case of a powered down driver).

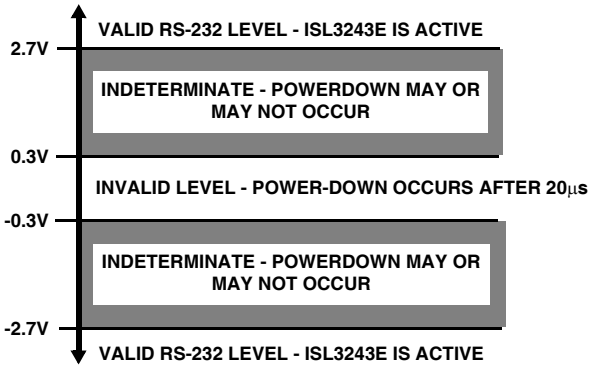


FIGURE 10. DEFINITION OF VALID RS-232 RECEIVER LEVELS

$\overline{\text{INVALID}}$ switches low after invalid levels have persisted on all of the receiver inputs for more than 20µs (see Figure 11). $\overline{\text{INVALID}}$ switches back high 1µs after detecting a valid RS-232 level on a receiver input. $\overline{\text{INVALID}}$ operates in all modes (forced or automatic power-down, or forced on), so it is also useful for systems employing manual power-down circuitry. When automatic powerdown is utilized, $\overline{\text{INVALID}}$ = 0 indicates that the ISL3243E is in powerdown mode.

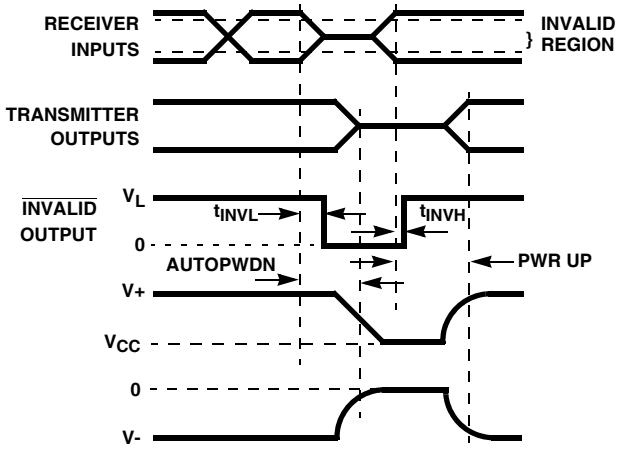


FIGURE 11. AUTOMATIC POWERDOWN AND $\overline{\text{INVALID}}$ TIMING DIAGRAMS

Automatic Power-down (ISL3243E Only)

Even greater power savings is available by using the ISL3243E which features an *automatic* power-down function. When no valid RS-232 voltages (see Figure 11) are sensed on any receiver input for 20µs, the charge pump and transmitters power-down, thereby reducing supply current to less than 1µA. Invalid receiver levels occur whenever the driving peripheral's outputs are shut off (powered down) or when the RS-232 interface cable is disconnected. The ISL3243E powers back up whenever it detects a valid RS-232 voltage level on any receiver input. This automatic power-down feature provides additional system power savings without changes to the existing operating system.

Automatic power-down operates when the FORCEON input is low, and the $\overline{\text{FORCEOFF}}$ input is high. Tying FORCEON high disables automatic power-down, but manual power-down is always available via the overriding $\overline{\text{FORCEOFF}}$ input. Table 2 summarizes the automatic power-down functionality.

The time to recover from automatic power-down mode is typically 20µs.

Capacitor Selection

The charge pumps require 0.1µF, or greater, capacitors for proper operation. Increasing the capacitor values (by a factor of 2) reduces ripple on the transmitter outputs and slightly reduces power consumption.

When using minimum required capacitor values, make sure that capacitor values do not degrade excessively with temperature. If in doubt, use capacitors with a larger nominal value. The capacitor's equivalent series resistance (ESR) usually rises at low temperatures and it influences the amount of ripple on V+ and V-.

Power Supply Decoupling

In most circumstances a 0.1µF bypass capacitor is adequate. In applications that are particularly sensitive to power supply noise, decouple V_{CC} and V_L to ground with a capacitor of the same value as the charge-pump capacitor C_1. Connect the bypass capacitor as close as possible to the IC.

Transmitter Outputs when Exiting Power-down

Figure 12 shows the response of two transmitter outputs when exiting powerdown mode. As they activate, the two transmitter outputs properly go to opposite RS-232 levels, with no glitching, ringing, nor undesirable transients. Each transmitter is loaded with 3kΩ in parallel with 1000pF. Note that the transmitters enable only when the magnitude of V+ and V- exceeds approximately 3V.

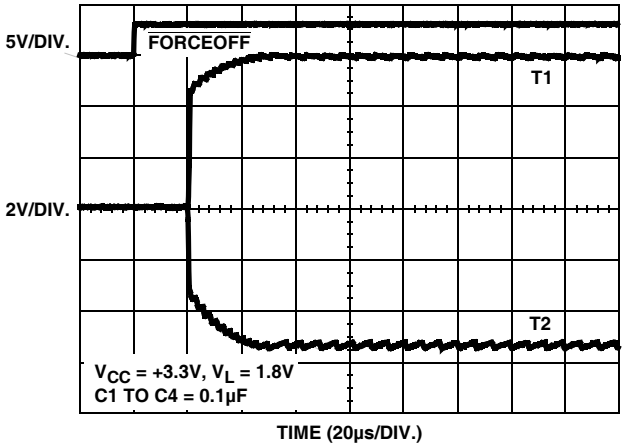


FIGURE 12. TRANSMITTER OUTPUTS WHEN EXITING POWERDOWN

Operation Down to 2.7V

ISL324xE transmitter outputs meet RS-562 levels (±3.7V), at the full data rate, with V_{CC} as low as 2.7V. RS-562 levels typically ensure inter operability with RS-232 devices.

High Data Rates

The ISL324xE maintain the RS-232 ±5V minimum transmitter output voltages even at high data rates. Figure 13 details a transmitter loopback test circuit, and Figure 14 illustrates the loopback test result at 120kbps. For this test, all transmitters were simultaneously driving RS-232 loads in parallel with 1000pF, at 120kbps. Figure 15 shows the loopback results for a single transmitter driving 1000pF and an RS-232 load at 250kbps. The static transmitters were also loaded with an RS-232 receiver.

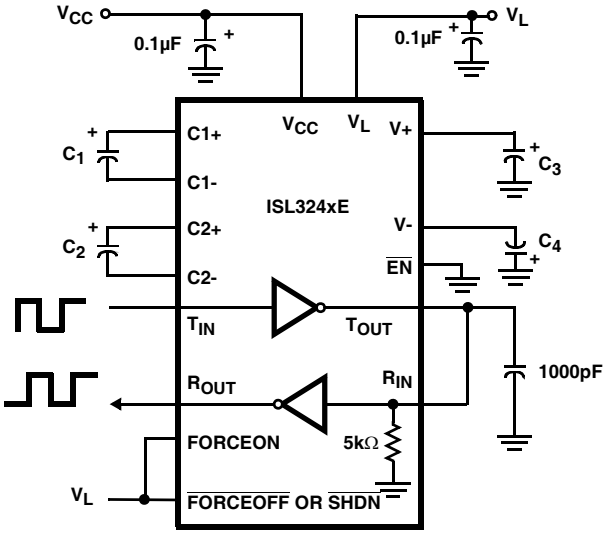


FIGURE 13. TRANSMITTER LOOPBACK TEST CIRCUIT

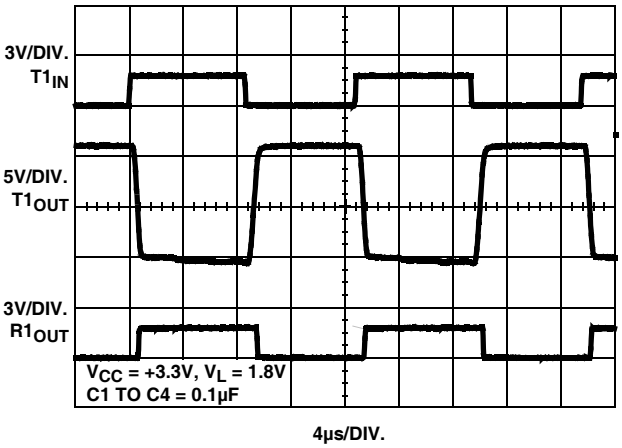


FIGURE 14. LOOPBACK TEST AT 120kbps

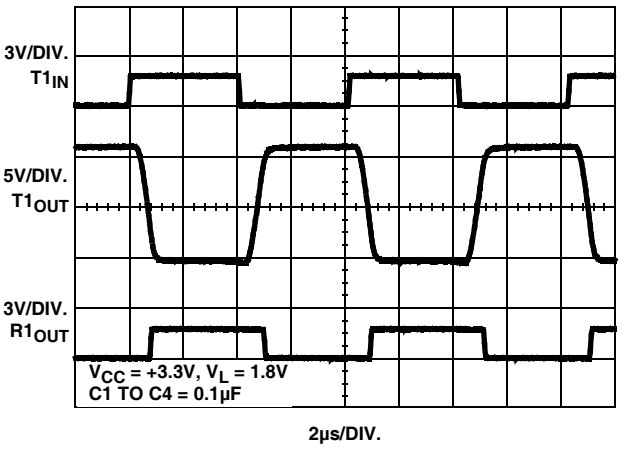


FIGURE 15. LOOPBACK TEST AT 250kbps

Interconnection to 1.8V, and 2.5V Logic

Standard 3.3V powered RS-232 devices interface well with 3V powered TTL compatible logic families (e.g., ACT and HCT).

The ISL324xE V_L supply pin allows interconnection to 1.8V or 2.5V logic. By connecting V_L to the same supply (1.8V or 2.5V) powering the logic device, the ISL324XE logic outputs will swing from GND to the logic V_{CC}.

±15kV ESD Protection

All pins on ISL324xE devices include ESD protection structures, but the RS-232 pins (transmitter outputs and receiver inputs) incorporate advanced structures which allow them to survive ESD events up to ±15kV. The RS-232 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins, or connecting a cable, can cause an ESD event that might destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered up, protect without allowing any latchup mechanism to activate, and don't interfere with RS-232 signals as large as ±25V.

Human Body Model (HBM) Testing

As the name implies, this test method emulates the ESD event delivered to an IC during human handling. The tester delivers the charge through a 1.5kΩ current limiting resistor, making the test less severe than the IEC61000 test which utilizes a 330Ω limiting resistor. The HBM method determines an ICs ability to withstand the ESD transients typically present during handling and manufacturing. Due to the random nature of these events, each pin is tested with respect to all other pins. The RS-232 pins on "E" family devices can withstand HBM ESD events to ±15kV.

IEC61000-4-2 Testing

The IEC61000 test method applies to finished equipment, rather than to an individual IC. Therefore, the pins most likely to suffer an ESD event are those that are exposed to the outside world (the RS-232 pins in this case), and the IC is tested in its typical application configuration (power applied) rather than testing each pin-to-pin combination. The lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is much more severe than the HBM test. The extra ESD protection built into this device's RS-232 pins allows the design of equipment meeting level 4 criteria without the need for additional board level protection on the RS-232 port.

AIR-GAP DISCHARGE TEST METHOD

For this test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on approach speed, humidity, temperature, etc., so it is difficult to obtain repeatable results. The "E" device RS-232 pins withstand ±15kV air-gap discharges.

CONTACT DISCHARGE TEST METHOD

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized, thereby eliminating the variables associated with the air-gap discharge. The result is a more repeatable and predictable test, but equipment limits prevent testing devices at voltages higher than ±8kV. All "E" family devices survive ±8kV contact discharges on the RS-232 pins.

Typical Performance Curves V_{CC} = 3.3V, V_L = 1.8V, T_A = +25°C

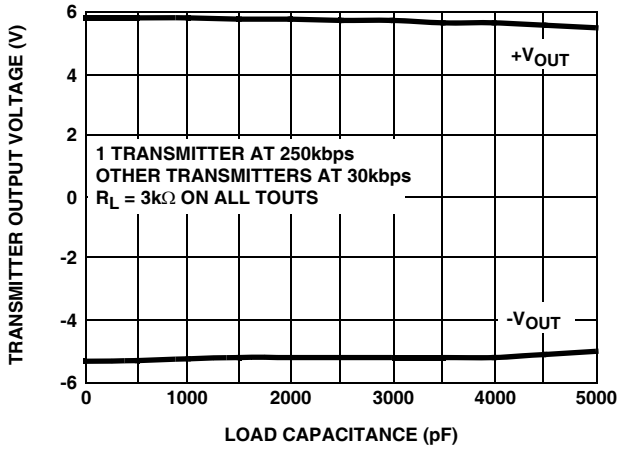


FIGURE 16. TRANSMITTER OUTPUT VOLTAGE vs LOAD CAPACITANCE

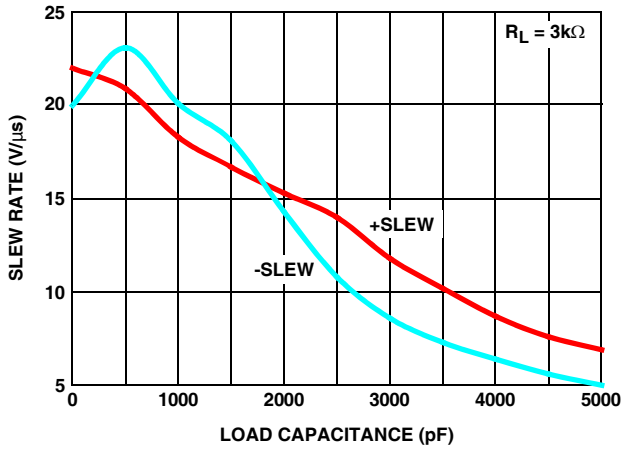


FIGURE 17. SLEW RATE vs LOAD CAPACITANCE

Typical Performance Curves V_{CC} = 3.3V, V_L = 1.8V, T_A = +25°C (Continued)

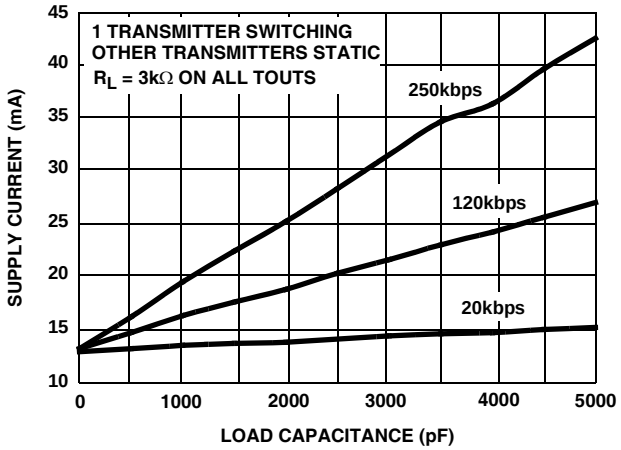


FIGURE 18. SUPPLY CURRENT vs LOAD CAPACITANCE WHEN TRANSMITTING DATA

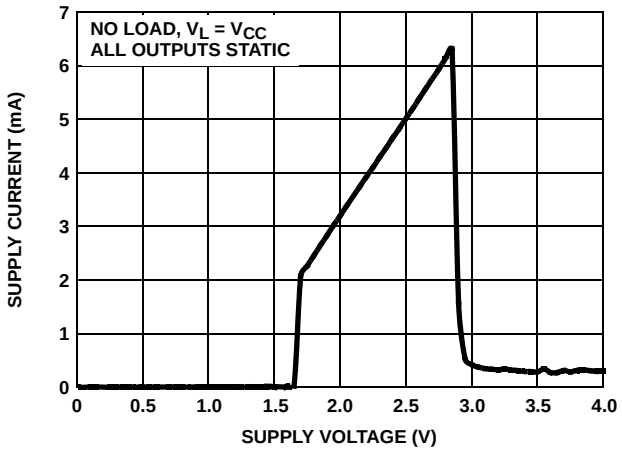


FIGURE 19. SUPPLY CURRENT vs SUPPLY VOLTAGE

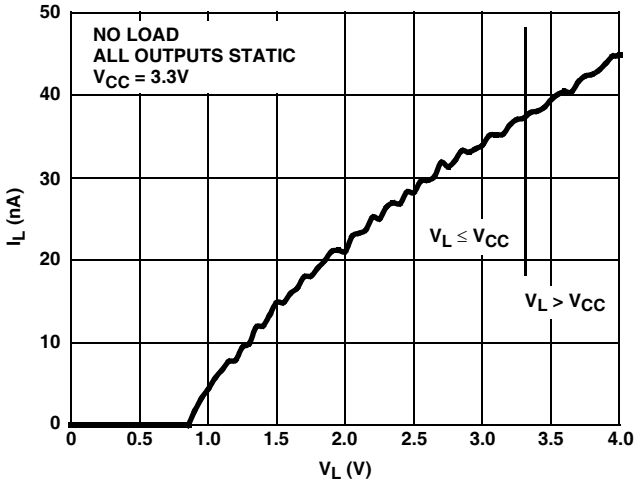


FIGURE 20. V_L SUPPLY CURRENT vs V_L VOLTAGE

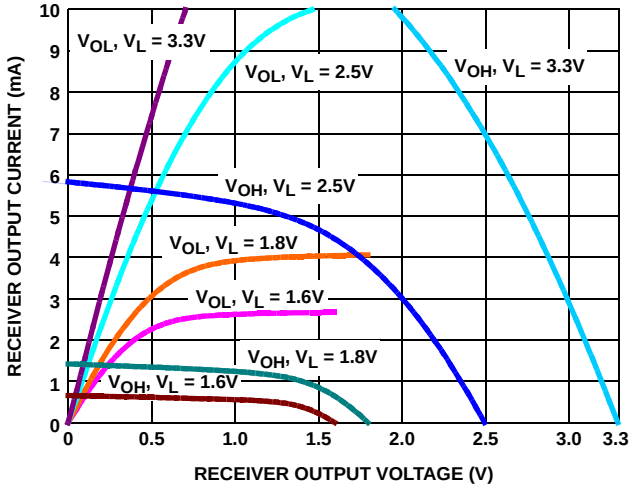


FIGURE 21. RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

Die Characteristics

SUBSTRATE AND QFN EXPOSED PAD POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

464

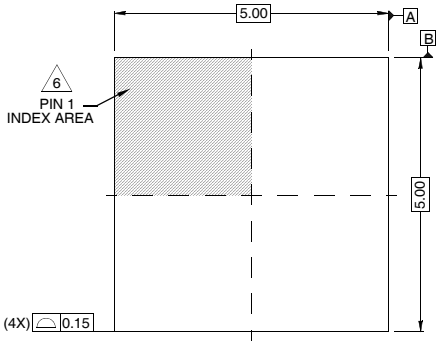
PROCESS:

Si Gate BiCMOS

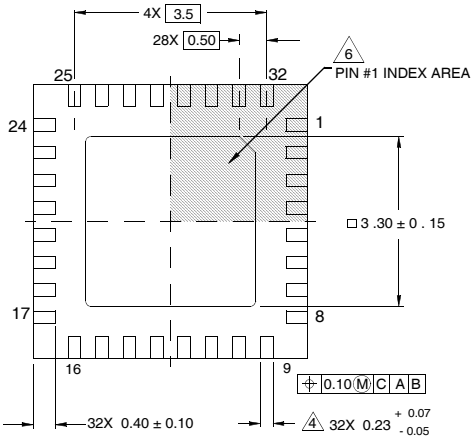
Package Outline Drawing

L32.5x5B

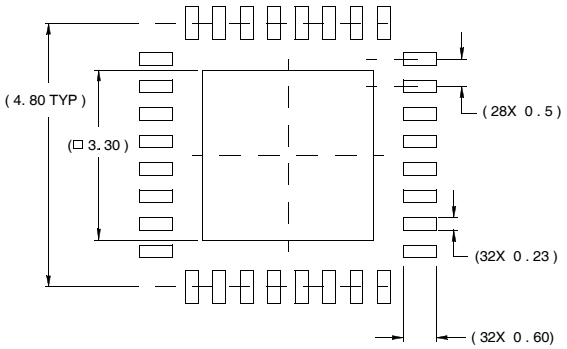
32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 11/07



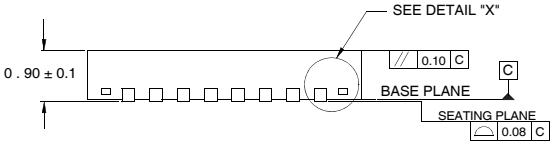
TOP VIEW



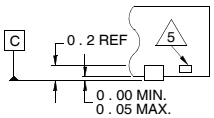
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.