

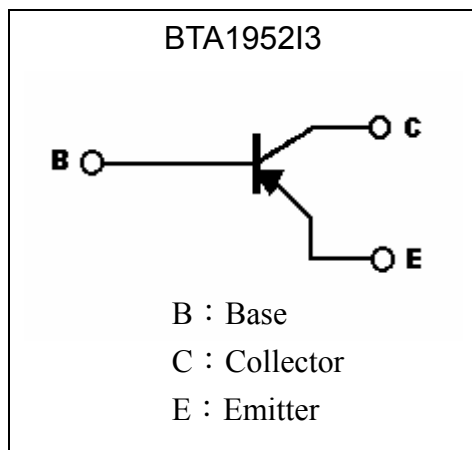
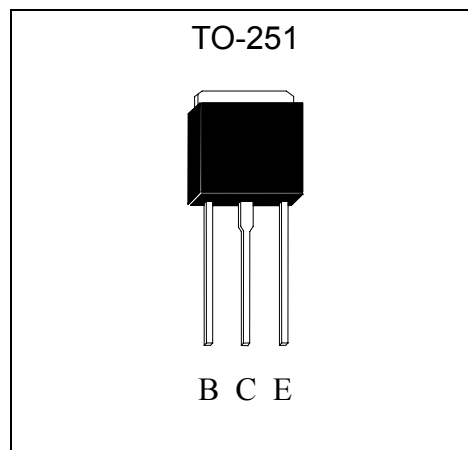
Low Vcesat PNP Epitaxial Planar Transistor

BTA1952I3

BV_{CEO}	-100V
I_C	-5A
R_{CESAT}	150m Ω

Features

- Low $V_{CE(sat)}$, $V_{CE(sat)}=-0.45$ V (typical), at $I_C / I_B = -3A / -0.15A$
- Excellent DC current gain characteristics
- Wide SOA
- Complementary to BTC5103I3
- RoHS compliant package

Symbol

Outline

Absolute Maximum Ratings ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V_{CBO}	-100	V
Collector-Emitter Voltage	V_{CEO}	-60	V
Emitter-Base Voltage	V_{EBO}	-5	V
Collector Current	$I_C(\text{DC})$	-5	A
	$I_C(\text{Pulse})$	-10 *1	
Power Dissipation	$P_d(T_a=25^\circ\text{C})$	1	W
	$P_d(T_c=25^\circ\text{C})$	25	
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55~+150	$^\circ\text{C}$

 Note : *1. Single Pulse $P_w=10\text{ms}$



Characteristics (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV _{CBO}	-100	-	-	V	I _C =-50μA, I _E =0
BV _{CEO}	-60	-	-	V	I _C =-10mA, I _B =0
BV _{EBO}	-5	-	-	V	I _E =-50μA, I _C =0
I _{CBO}	-	-	-1	μA	V _{CB} =-100V, I _E =0
I _{EBO}	-	-	-1	μA	V _{EB} =-5V, I _C =0
*V _{CE(sat)}	-	-0.45	-0.6	V	I _C =-3A, I _B =-0.15A
*V _{BE(sat)}	-	-	-1.2	V	I _C =-3A, I _B =-0.15A
*h _{FE 1}	70	-	240	-	V _{CE} =-1V, I _C =-1A
*h _{FE 2}	30	-	-	-	V _{CE} =-1V, I _C =-3A
f _T	-	60	-	MHz	V _{CE} =-4V, I _C =-1A, f=30MHz

*Pulse Test : Pulse Width ≤380μs, Duty Cycle≤2%

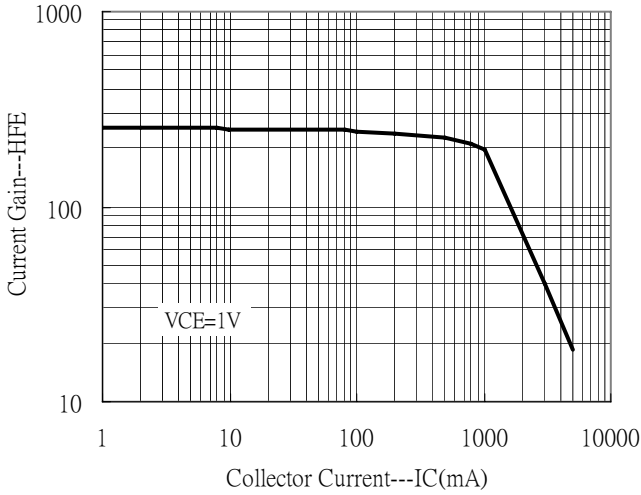
Ordering Information

Device	Package	Shipping	Marking
BTA1952I3	TO-251 (RoHS compliant)	80 pcs / tube, 50 tubes / box	A1952

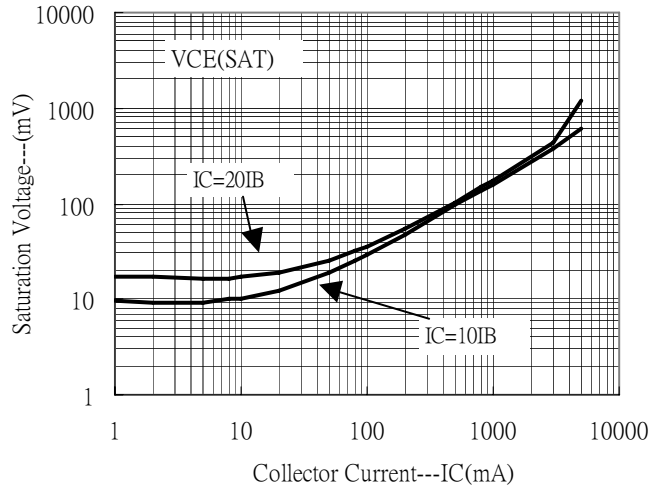


Characteristic Curves

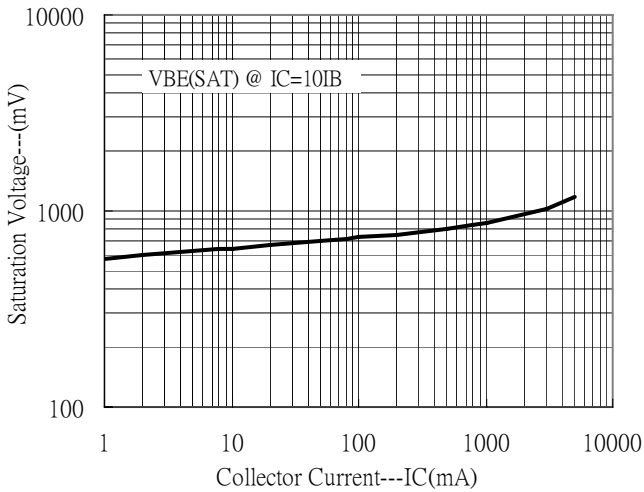
Current Gain vs Collector Current



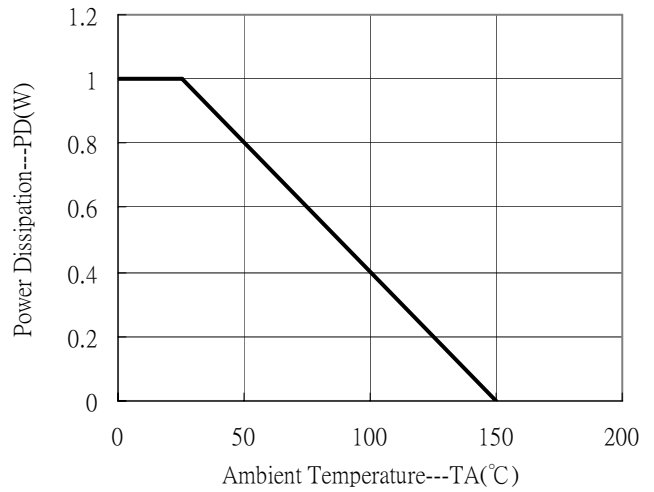
Saturation Voltage vs Collector Current



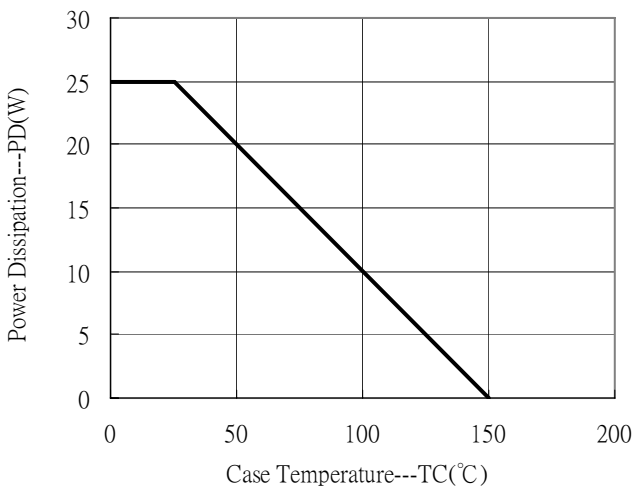
Saturation Voltage vs Collector Current



Power Derating Curve



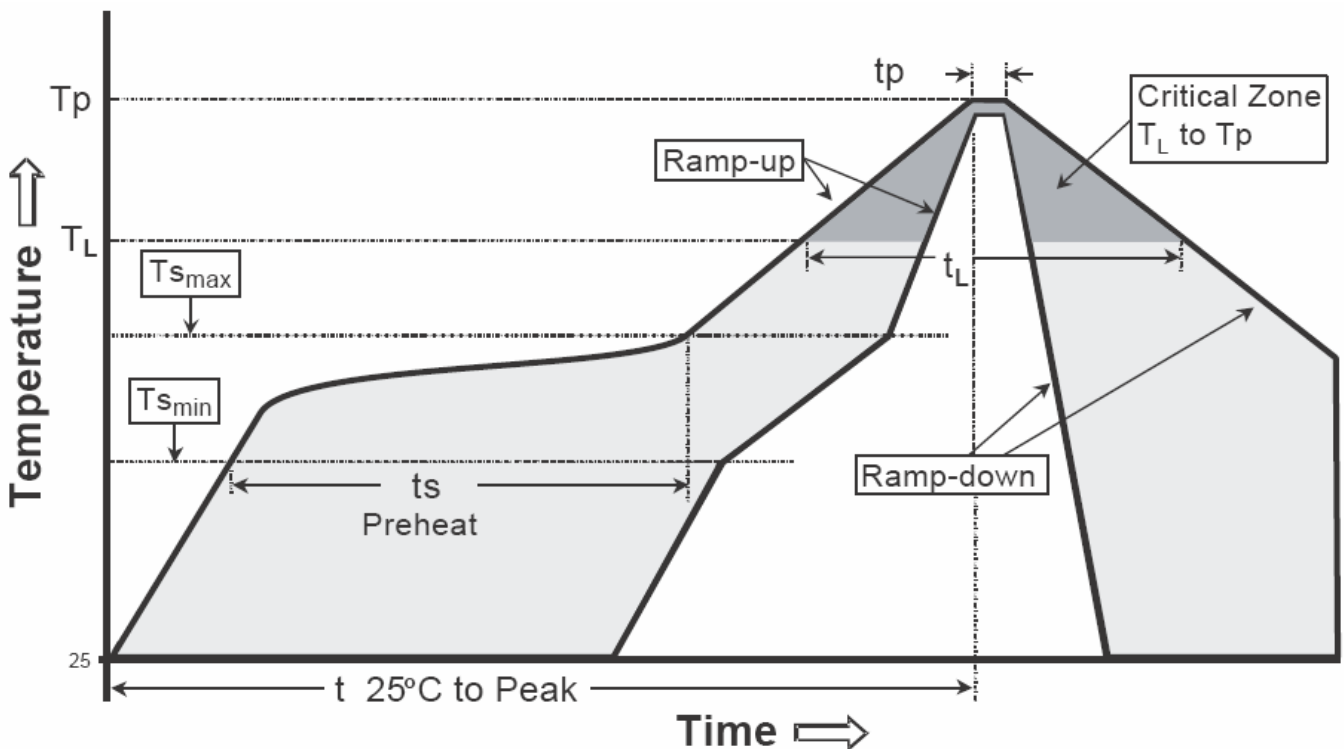
Power Derating Curve



Recommended wave soldering condition

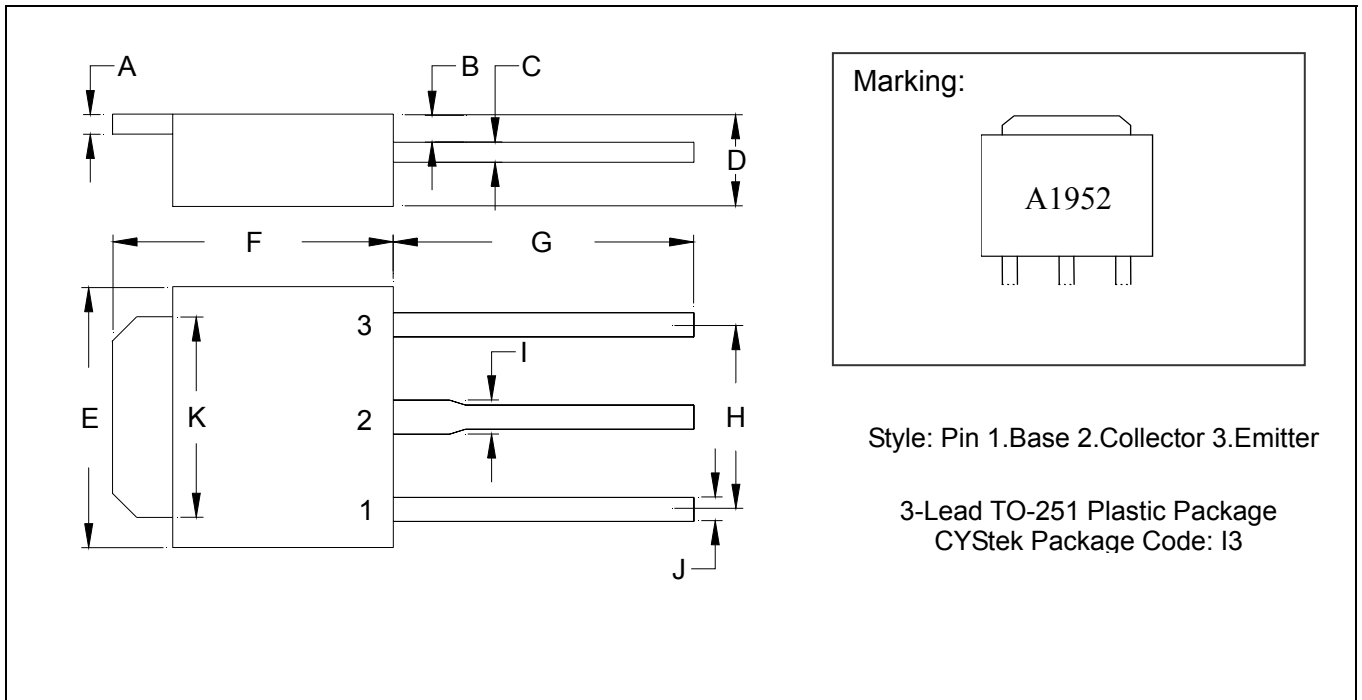
Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

TO-251 Dimension



Style: Pin 1.Base 2.Collector 3.Emitter

3-Lead TO-251 Plastic Package
 CYStek Package Code: I3

*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.0177	0.0217	0.45	0.55	G	0.2559	-	6.50	-
B	0.0354	0.0591	0.90	1.50	H	-	*0.1811	-	*4.60
C	0.0177	0.0236	0.45	0.60	I	-	0.0449	-	1.14
D	0.0866	0.0945	2.20	2.40	J	-	0.0346	-	0.88
E	0.2441	0.2677	6.20	6.80	K	0.2047	0.2165	5.20	5.50
F	0.2677	0.2835	6.80	7.20					

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: KFC; pure tin plated
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.