



DES-011

SERIAL DIGITAL TO PARALLEL TTL MODULE

- Small compact design for pcb mounting
- Composite or Component digital inputs
- 8 or 10 bit data
- Reclocked SD outputs available.
- Auto 144,177,270, 360 mb/s Operation
- Automatic Cable equalisation
- + 5V DC power

This interface card accepts multistandard serial digital signals and converts these to a 10 bit parallel data stream with a word rate clock. In addition outputs indicating the presence of TRS and EAV timing reference signals are provided to allow easy decoding of the parallel data stream.

Input Requirements

<i>Input data format</i>	SMPTE 259M
<i>Input data rates</i>	360 Mb/s serial 4:2:2 widescreen component 270 Mb/s serial 4:2:2 component 144,177 Mb/s serial NTSC/PAL
<i>Input Impedance</i>	75 ohm terminating
<i>Equalisation</i>	Automatic up to 40 dB at 200 MHz (Typically 300m of Belden 8281 at 270mb/s)

Output Characteristics

<i>Parallel Output</i>	One parallel word at 14.4, 17.7, 27 or 36Mb/s TTL/CMOS levels.
<i>SD Outputs</i>	2 reclocked serial outputs, SMPTE 259M
<i>EAV Output</i>	End of active video flag. For component video, a logic low is output for one cycle of the parallel clock every time an EAV timing reference signal is detected. The pulse is aligned with the fourth word of the timing reference (the XYZ word.) For composite video, this line is always asserted high.
<i>TRS Output</i>	Timing reference flag. A logic low is output for the duration of the TRS.

Other parameters

<i>Power</i>	+5V \pm 0.25V (300 mA max)
<i>Operating Temperature</i>	0°C to 40°C
<i>Aqueous Washable</i>	No
<i>Package</i>	DR00174A

ORDERING CODES

DES-011A
DES-011B

Reclocked o/p's

x
√

© Faraday Technology. As part of continual product improvement the specifications, details and dimensions shown in this publication are subject to change without notice

PACKAGE DETAIL

