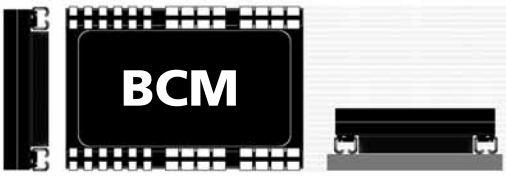
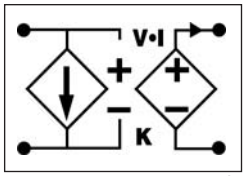


B352F110T24

V•I Chip™ – BCM
Bus Converter Module

- 352 V to 11.0 V V•I Chip Converter
- 240 Watt (360 Watt for 1 ms)
- High density – up to 876 W/in³
- Small footprint – 210 W/in²
- Low weight – 0.5 oz (14 g)
- ZVS/ZCS isolated sine amplitude converter
- Typical efficiency 95%
- 125°C operation
- <1 µs transient response
- >2.6 million hours MTBF
- No output filtering required



©

Vin = 330 - 365 V
Vout = 10.3 - 11.4 V
Iout = 21.8 A
K = 1/32
Rout = 15.0 mΩ max

Actual size

Product Description

The V•I Chip Bus Converter Module (BCM) is a high efficiency (>95%), narrow input range Sine Amplitude Converter (SAC) operating from a 330 to 365 Vdc primary bus to deliver an isolated low voltage secondary. The off-line BCM provides an isolated 10.3 -11.4 V distribution bus and is ideal for use in silver boxes and PFC front ends. Due to the fast response time and low noise of the BCM, the need for limited life aluminum electrolytic or tantalum capacitors at the input of POL converters is reduced—or eliminated—resulting in savings of board area, materials and total system cost.

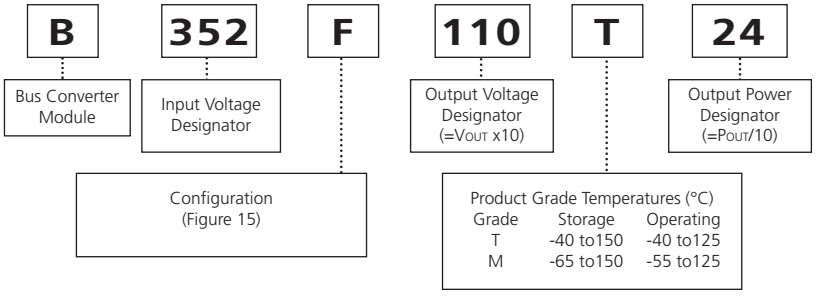
The BCM achieves a power density of 876 W/in³ in a V•I Chip package compatible with standard pick-and-place and surface mount assembly processes. The V•I Chip package provides flexible thermal management through its low Junction-to-Case and Junction-to-Board thermal resistance. Owing to its high conversion efficiency and safe operating temperature range, the BCM does not require a discrete heat sink in typical applications. Low junction to case and junction to lead thermal impedances assure low junction temperatures and long life in the harshest environments.

Absolute Maximum Ratings

Parameter	Values	Unit	Notes
+In to -In	-1.0 to 400	Vdc	
+In to -In	500	Vdc	For 100 ms
PC to -In	-0.3 to 7.0	Vdc	
+Out to -Out	-0.5 to 16.0	Vdc	
Isolation voltage	4,242	Vdc	Input to Output
Output current	24.1	A	Continuous
Peak output current	32.7	A	For 1 ms
Output power	240	W	Continuous
Peak output power	360	W	For 1 ms
Case temperature	208	°C	During reflow
Operating junction temperature(1)	-40 to 125	°C	T - Grade
	-55 to 125	°C	M - Grade
Storage temperature	-40 to 150	°C	T - Grade
	-65 to 150	°C	M - Grade

Note:
(1) The referenced junction is defined as the semiconductor having the highest temperature. This temperature is monitored by a shutdown comparator.

Part Numbering



Input (Conditions are at 352 Vin, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Input voltage range	330	352	365	Vdc	
Input dV/dt			1	V/µs	
Input undervoltage turn-on			325	Vdc	
Input undervoltage turn-off	275			Vdc	
Input overvoltage turn-on	370			Vdc	
Input overvoltage turn-off			395	Vdc	
Input quiescent current		1.2		mA	PC low
Inrush current overshoot		0.2		A	Using test circuit in Figure 25; See Figure 1
Input current			0.7	Adc	
Input reflected ripple current		610		mA p-p	Using test circuit in Figure 25; See Figure 4
No load power dissipation		4.9	7.0	W	
Internal input capacitance		0.25		µF	
Internal input inductance		5		nH	
Recommended external input capacitance		2		µF	200 nH maximum source inductance; See Figure 25

Input Waveforms

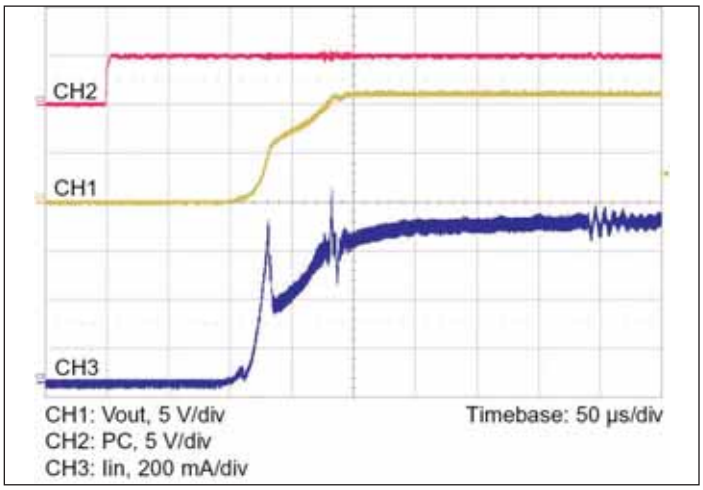


Figure 1— *Inrush transient current at full load and 352 Vin with PC enabled*

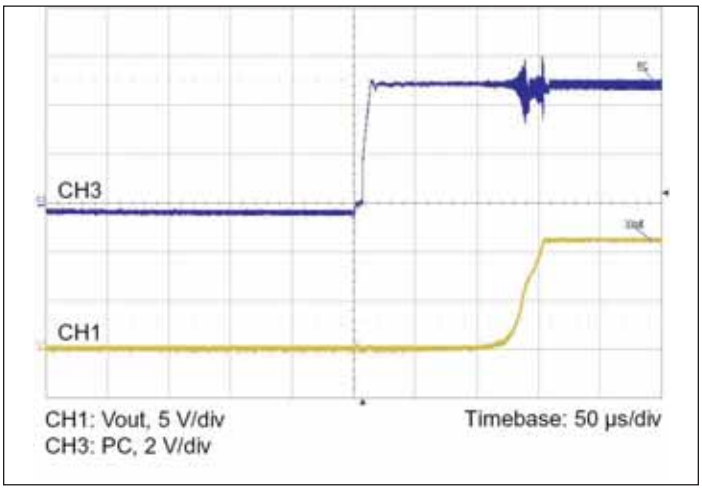


Figure 2— *Output voltage turn-on waveform with PC enabled at full load and 352 Vin*

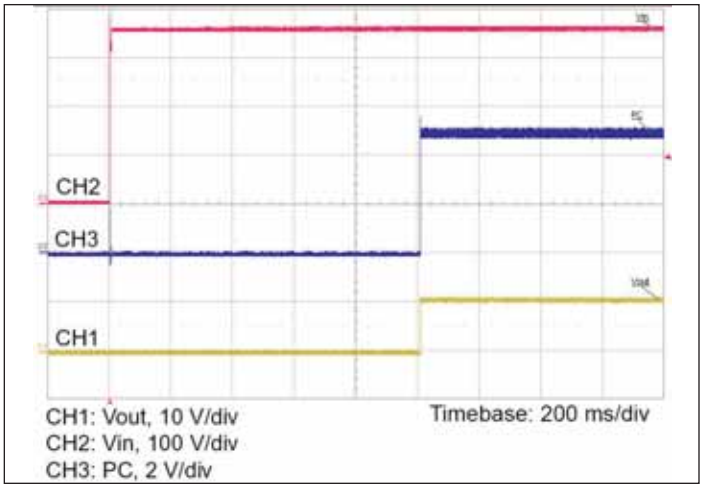


Figure 3— *Output voltage turn-on waveform with input turn-on at full load and 352 Vin*

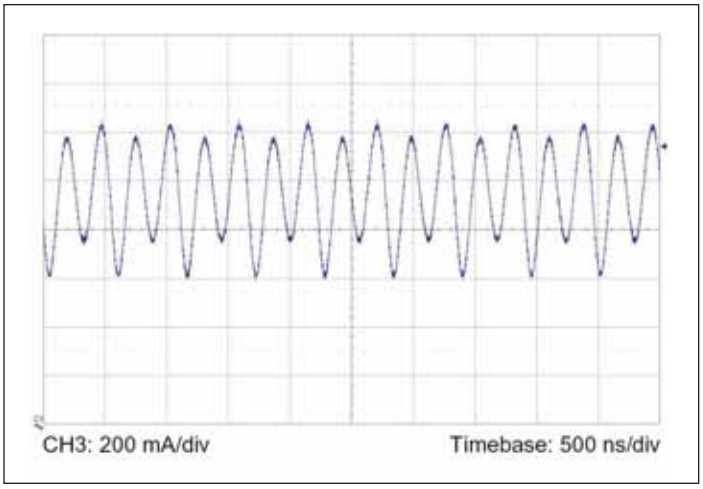


Figure 4— *Input reflected ripple current at full load and 352 Vin*

Output (Conditions are at 352 Vin, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Output voltage	10.3		11.4	Vdc	No load
	9.99		11.1	Vdc	Full load
Output power	0		240	W	330 - 365 V_{IN}
Rated DC current	0		24.1	Adc	$P_{OUT} \leq 240$ W
Peak repetitive power			360	W	Max pulse width 1ms, max duty cycle 10%, baseline power 50%
Current share accuracy		5	10	%	See Parallel Operation on page 9
Efficiency					
Half load	94.5	95.6		%	See Figure 5
Full load	94.7	95.8		%	See Figure 5
Internal output inductance		1.1		nH	
Internal output capacitance		31		µF	Effective value
Load capacitance			1,000	µF	
Output overvoltage setpoint	11.6			Vdc	
Output ripple voltage					
No external bypass		240	300	mV p-p	See Figures 7 and 9
10 µF bypass capacitor		14		mV p-p	See Figure 8
Short circuit protection set point	30.0			Adc	Module will shut down
Average short circuit current		0.12		A	
Effective switching frequency	3.3	3.5	3.7	MHz	Fixed, 1.75 MHz per phase
Line regulation					
K	0.0309	1/32	0.0316		$V_{OUT} = K \bullet V_{IN}$ at no load
Load regulation					
R_{OUT}		11.0	15.0	mΩ	
Transient response					
Voltage overshoot		46		mV	100% load step; See Figures 10 and 11
Response time		200		ns	See Figures 10 and 11
Recovery time		1		µs	See Figures 10 and 11
Output overshoot					
Input turn-on		0		mV	No output filter; See Figure 3
PC enable		0		mV	No output filter; See Figure 2
Output turn-on delay					
From application of power		800		ms	No output filter; See Figure 3
From release of PC pin		250		ms	No output filter

Output Waveforms

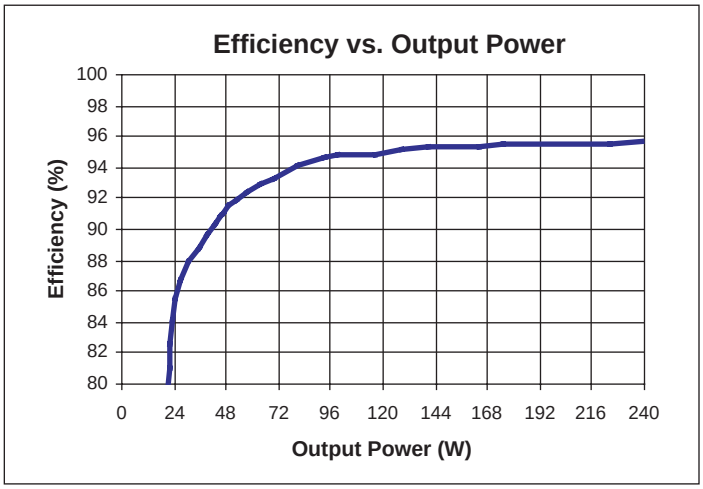


Figure 5— *Efficiency vs. output power at 352 Vin*

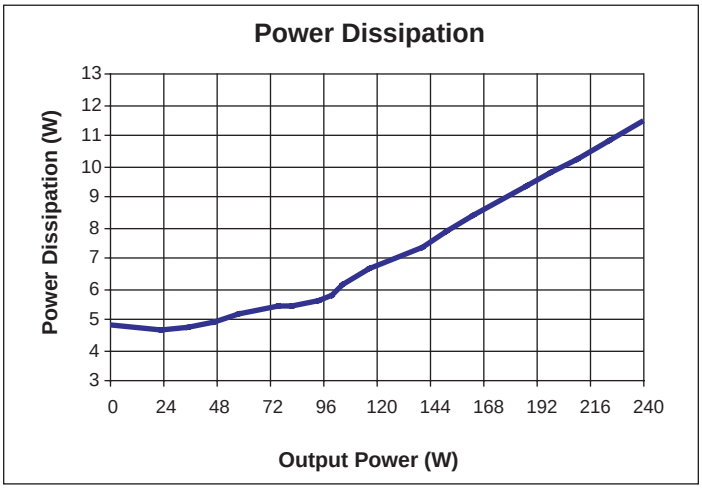


Figure 6—*Power dissipation as a function of output power*

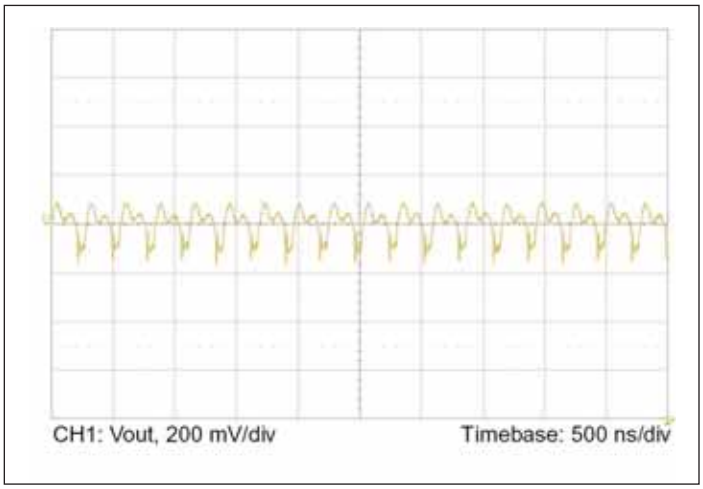


Figure 7— *Output voltage ripple at full load and 352 Vin; without any external bypass capacitor.*

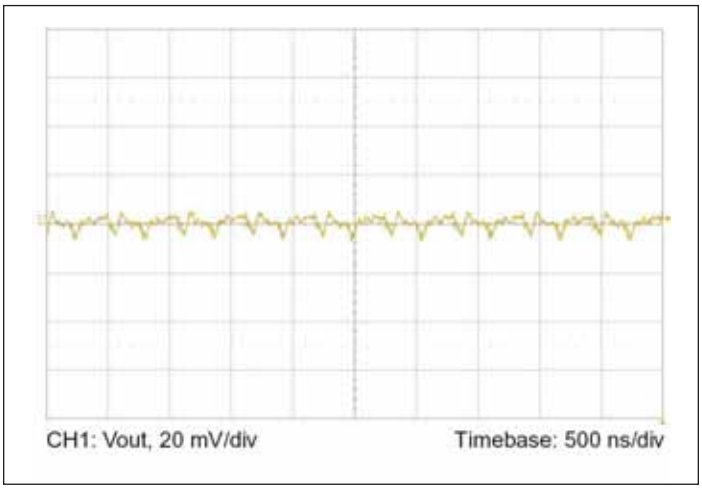


Figure 8—*Output voltage ripple at full load and 352 Vin with 10 µF ceramic external bypass capacitor and 20 nH of distribution inductance.*

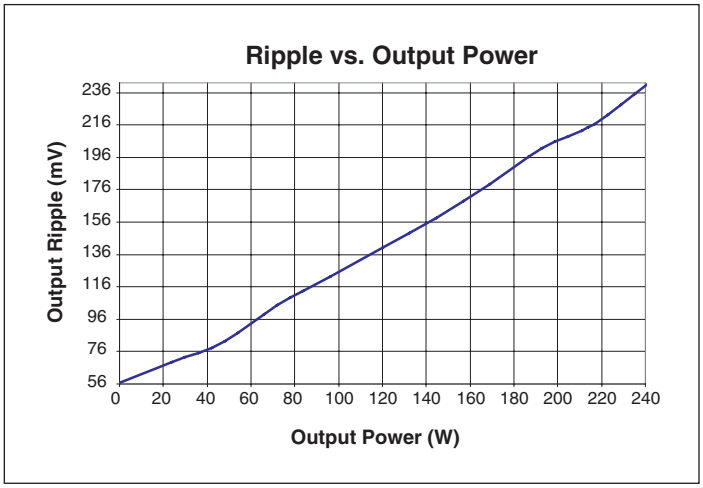


Figure 9— *Output voltage ripple vs. output power at 352 Vin without any external bypass capacitor.*

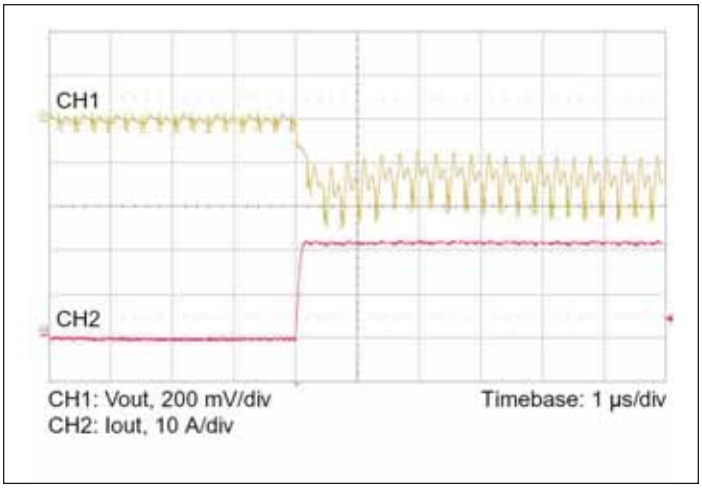


Figure 10— *0 -21.8 A load step with 2 µF input capacitor and no output capacitor.*

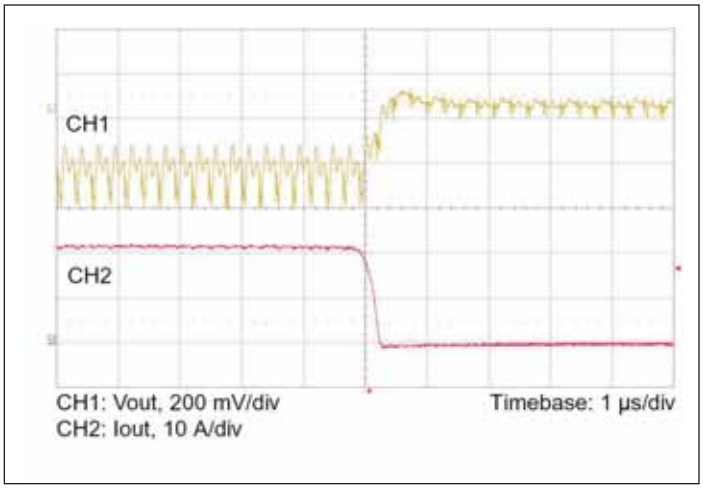


Figure 11— *21.8-0 A load step with 2 µF input capacitance.*

General

Parameter	Min	Typ	Max	Unit	Note
MTBF					
MIL-HDBK-217F		2.6		Mhrs	25°C, GB
Isolation specifications					
Voltage	4,242			Vdc	Input to Output
Capacitance		500		pF	Input to Output
Resistance	10			MΩ	Input to Output
Agency approvals (pending)		cTÜVus			UL/CSA 60950, EN 60950
		CE Mark			Low Voltage Directive
Mechanical parameters					See mechanical drawing, Figures 15
Weight		0.50 / 14		oz / g	
Dimensions					
Length		1.26 / 32		in / mm	
Width		0.87 / 22		in / mm	
Height		0.25 / 6,2		in / mm	

Auxiliary Pins (Conditions are at 48 Vin, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Primary control (PC)					
DC voltage	4.8	5.0	5.2	Vdc	
Module disable voltage	2.4	2.5		Vdc	
Module enable voltage		2.5	2.6	Vdc	
Current limit	2.4	2.5	2.9	mA	Source only
Enable delay time		250		ms	
Disable delay time		20		µs	See Figure 12, time from PC low to output low

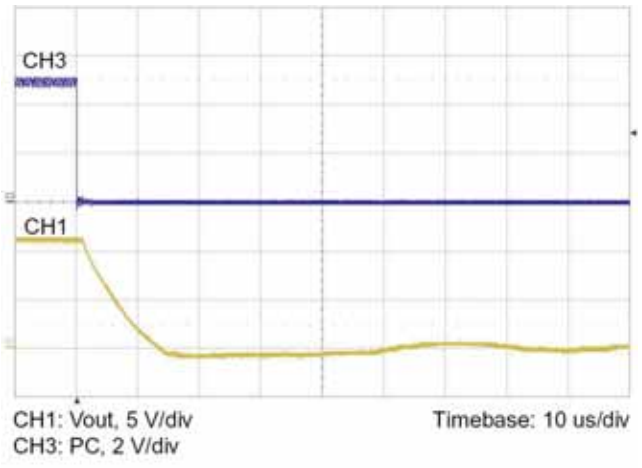


Figure 12— *VOUT at full load vs. PC disable*

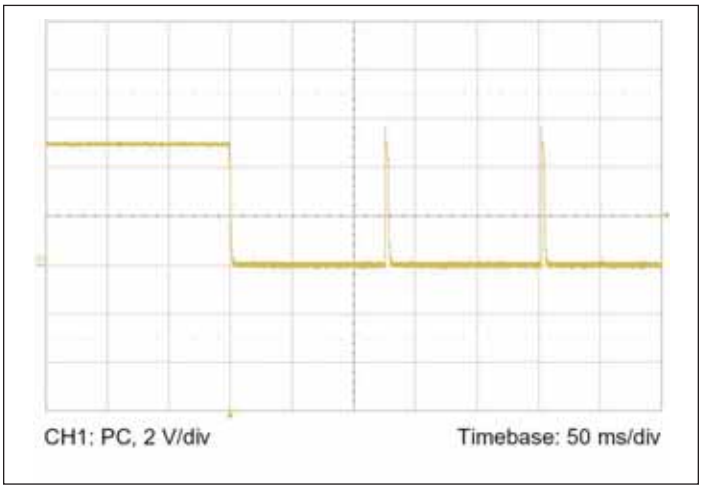


Figure 13— *PC signal during fault*

+IN/-IN – DC Voltage Input Ports

The V•I Chip input voltage range should not be exceeded. An internal under/over voltage lockout-function prevents operation outside of the normal operating input range. The BCM turns ON within an input voltage window bounded by the "Input under-voltage turn-on" and "Input over-voltage turn-off" levels, as specified. The V•I Chip may be protected against accidental application of a reverse input voltage by the addition of a rectifier in series with the positive input, or a reverse rectifier in shunt with the positive input located on the load side of the input fuse.

The connection of the V•I Chip to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100 nH, the input should be bypassed with a RC damper to retain low source impedance and stable operation. With an interconnect inductance of 200 nH, the RC damper may be 2 µF in series with 0.3Ω. A single electrolytic or equivalent low-Q capacitor may be used in place of the series RC bypass.

PC – Primary Control

The Primary Control port is a multifunction node that provides the following functions:

Enable/Disable – If the PC port is left floating, the BCM output is enabled. Once this port is pulled lower than 2.4 Vdc with respect to –In, the output is disabled. This action can be realized by employing a relay, opto-coupler, or open collector transistor. Refer to Figures 1-3, 12 and 13 for the typical Enable/Disable characteristics. This port should not be toggled at a rate higher than 1 Hz. The PC port should also not be driven by or pulled up to an external voltage source.

Primary Auxiliary Supply – The PC port can source up to 2.4 mA at 5.0 Vdc. The PC port should never be used to sink current.

Alarm – The BCM contains circuitry that monitors output overload, input over voltage or under voltage, and internal junction temperatures. In response to an abnormal condition in any of the monitored parameters, the PC port will toggle. Refer to Figure 13 for PC alarm characteristics.

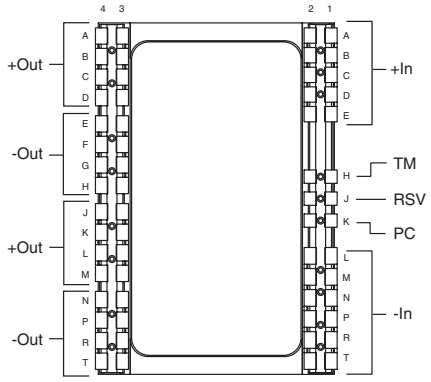
TM and RSV – Reserved for factory use.

+OUT/-OUT – DC Voltage Output Ports

Two sets of contacts are provided for the +Out port. They must be connected in parallel with low interconnect resistance. Similarly, two sets of contacts are provided for the –Out port. They must be connected in parallel with low interconnect resistance. Within the specified operating range, the average output voltage is defined by the Level 1 DC behavioral model of Figure 22. The current source capability of the BCM is rated in the specifications section of this document.

The low output impedance of the BCM reduces or eliminates the need for limited life aluminum electrolytic or tantalum capacitors at the input of POL converters.

Total load capacitance at the output of the BCM should not exceed the specified maximum. Owing to the wide bandwidth and low output impedance of the BCM, low frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the input of the BCM.



Signal Name	Designation
+In	A1-E1, A2-E2
–In	L1-T1, L2-T2
TM	H1, H2
RSV	J1, J2
PC	K1, K2
+Out	A3-D3, A4-D4, J3-M3, J4-M4
–Out	E3-H3, E4-H4, N3-T3, N4-T4

Figure 14*—BCM pin configuration*

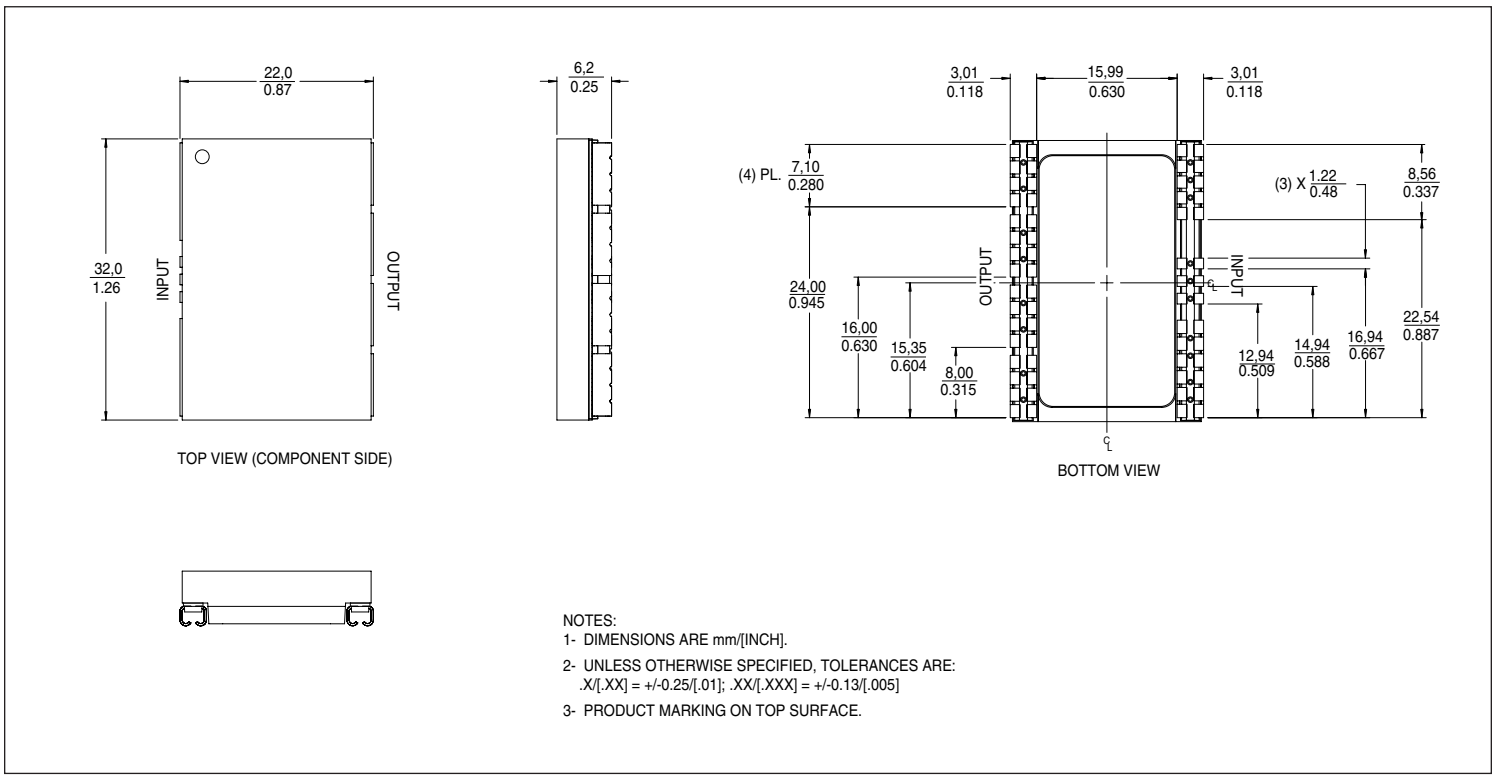


Figure 15*—BCM J-Lead mechanical outline; Onboard mounting*

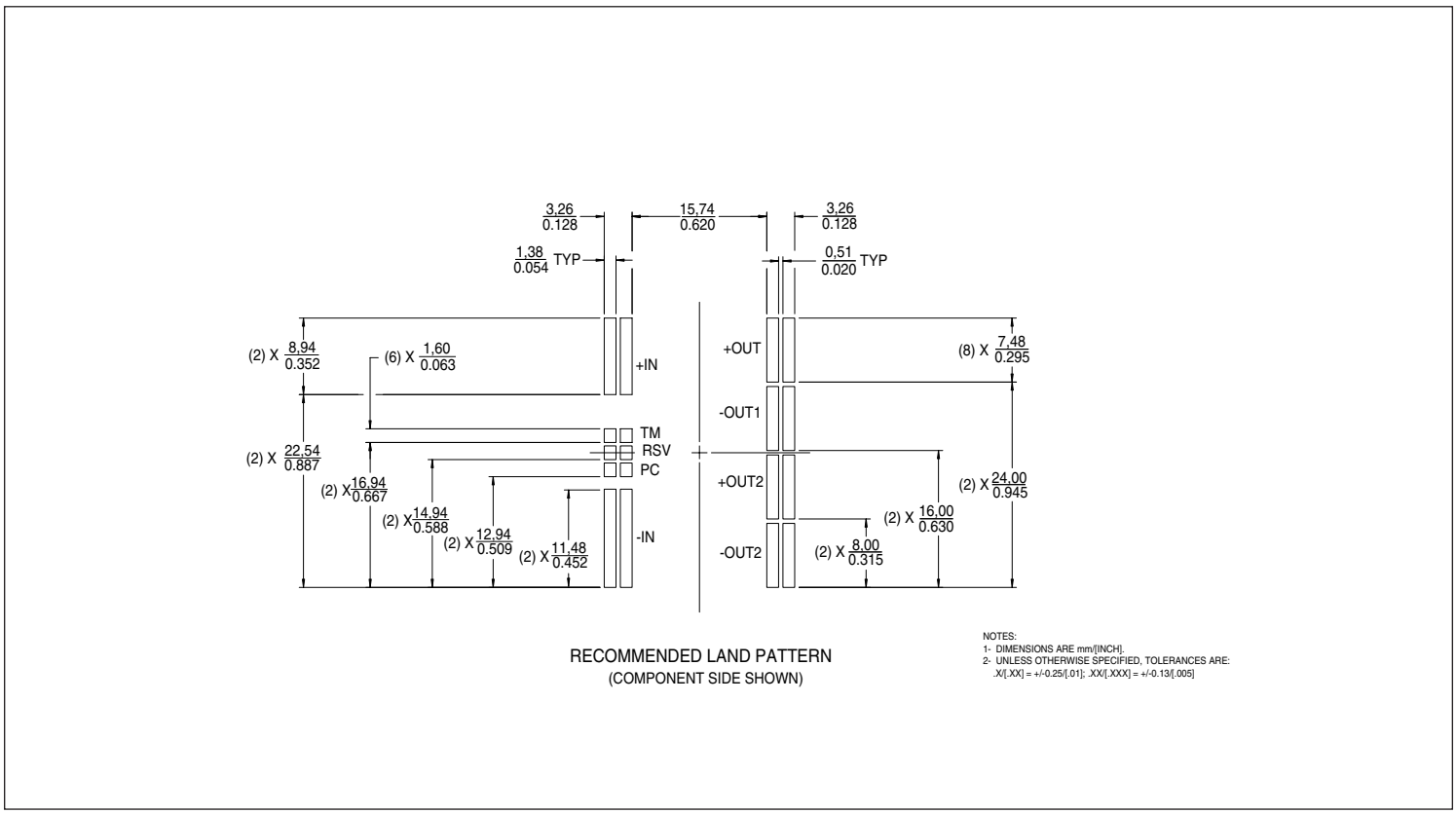


Figure 16*— BCM PCB land layout information*

CONFIGURATION	Standard(1) (Figure 17)	Standard with 0.25" heatsink
Effective power Density	876 W/in^3	440 W/in^3
Junction-board Thermal Resistance	2.4 °C/W	2.4 °C/W
Junction-Case Thermal Resistance	1.1 °C/W	N/A
Junction-Ambient Thermal Resistance 300LFM	6.8 °C/W	5.0 °C/W

Notes:

(1) Surface mounted to a 2" x 2" FR4 board, 4 layers 2 oz Cu

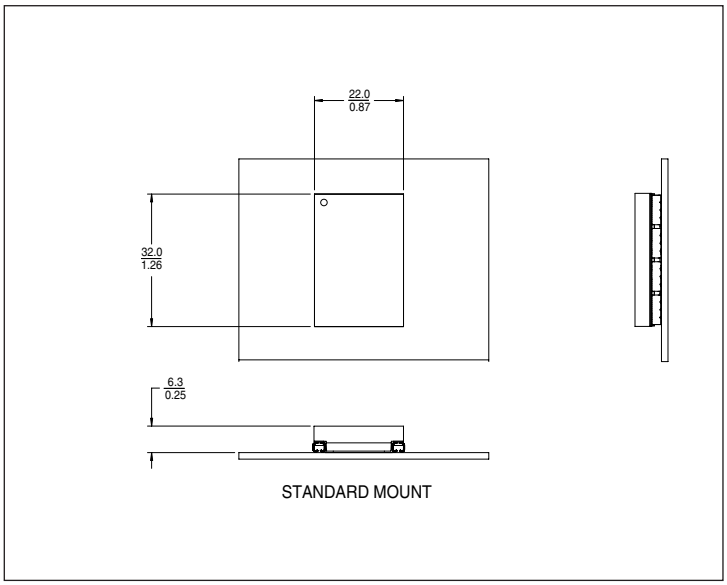


Figure 17*—Onboard mounting – package F*

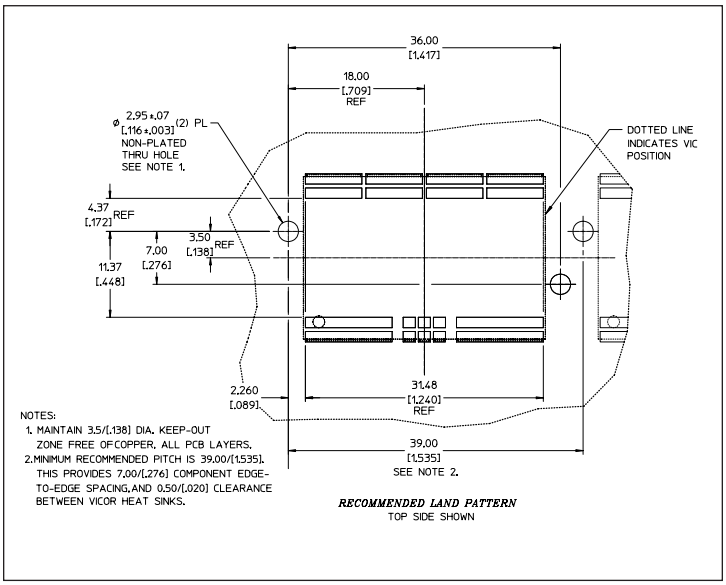


Figure 18*—Hole location for push pin heatsink relative to VIC*

Thermal

Symbol	Parameter	Min	Typ	Max	Unit	Note
	Over temperature shutdown	125	130	135	°C	Junction temperature
	Thermal capacity		0.61		Ws/°C	
$R_{\theta JC}$	Junction-to-case thermal impedance		1.1		°C/W	
$R_{\theta JB}$	Junction-to-board thermal impedance		2.1		°C/W	
$R_{\theta JA}$	Junction-to-ambient (1)		6.5		°C/W	
$R_{\theta JA}$	Junction-to-ambient (2)		5.0		°C/W	

Notes:

(1) B352F110T24 surface mounted to a 2" x 2" FR4 board, 4 layers 2 oz Cu, 300 LFM.

(2) B352F110T24 with a 0.25"H Heatsink surface mounted on FR4 board, 300 LFM.

Parallel Operation

The BCM will inherently current share when operated in an array. Arrays may be used for higher power or redundancy in an application.

Current sharing accuracy is maximized when the source and load impedance presented to each BCM within an array are equal.

The recommended method to achieve matched impedances is to dedicate common copper planes within the PCB to deliver and return the current to the array, rather than rely upon traces of varying lengths. In typical applications the current being delivered to the load is larger than that sourced from the input, allowing traces to be utilized on the input side if necessary. The use of dedicated power planes is, however, preferable.

The BCM power train and control architecture allow bi-directional power transfer, including reverse power processing from the BCM output to its input. Reverse power transfer is enabled if the BCM input is within its operating range and the BCM is otherwise enabled. The BCM's ability to process power in reverse improves the BCM transient response to an output load dump.

Thermal Management

The high efficiency of the V•I Chip results in relatively low power dissipation and correspondingly low generation of heat. The heat generated within internal semiconductor junctions is coupled with low effective thermal resistances, $R\theta_{JC}$ and $R\theta_{JB}$, to the V•I Chip case and the PCB allowing thermal management flexibility to adapt to specific application requirements (Figure 19).

CASE 1 Convection via heatsink to air.

The total Junction-to-Ambient thermal resistance, $R\theta_{JA}$, of a surface mounted V•I Chip with a 0.25"heatsink is 5°C/W in 300 LFM air flow (Figure 21). At full rated output power of 240 W, the heat generated by the BCM is approximately 11 W (Figure 6). Therefore, the junction temperature rise to ambient is approximately 53°C. Given a maximum junction temperature of 125°C, a temperature rise of 53°C allows the V•I Chip to operate at rated output power at up to 72°C ambient temperature. At 100 W of output power, operating ambient temperature extends to 103°C.

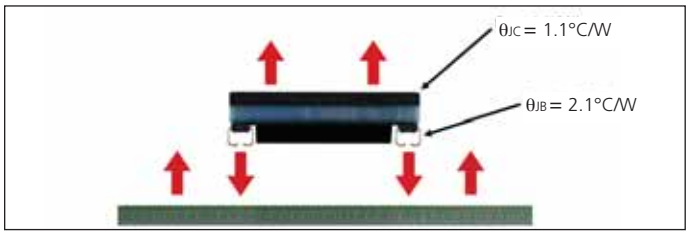


Figure 19—*Thermal resistance*

CASE 2—Conduction to the PCB

The low thermal resistance Junction-to-board, $R\theta_{JB}$, allows use of the PCB to exchange heat from the V•I Chip, including convection from the PCB to the ambient or conduction to a cold plate.

For example, with a V•I Chip surface mounted on a 2" x 2" area of a multi-layer PCB, with an aggregate 8 oz of effective copper weight, the total Junction-to-Ambient thermal resistance, $R\theta_{JA}$, is 6.5°C/W in 300 LFM air flow (see Thermal section, page 8). Given a maximum junction temperature of 125°C and 11 W dissipation at 240 W of output power, a temperature rise of 72°C allows the V•I Chip to operate at rated output power at up to 53°C ambient temperature.

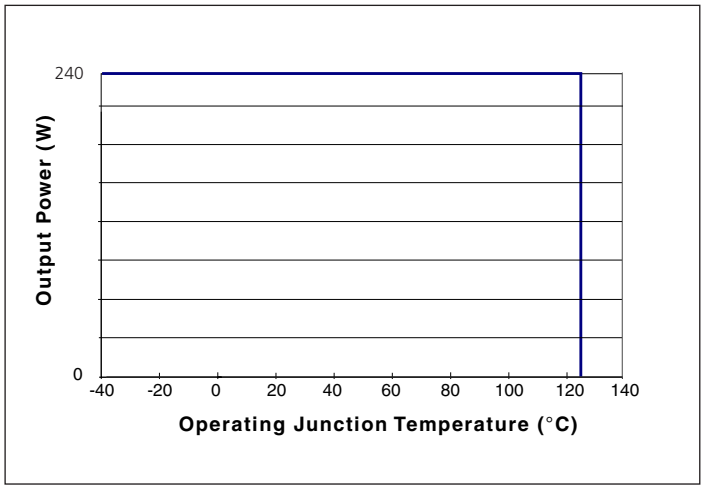


Figure 20— *Thermal derating curve*

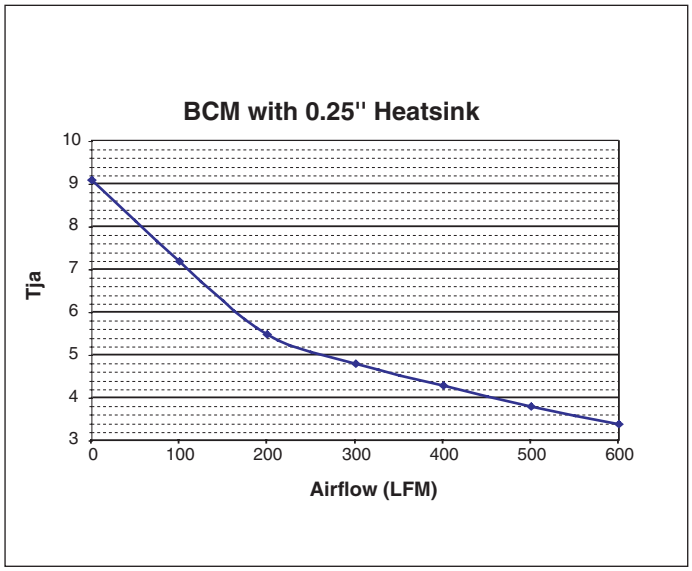


Figure 21—*Junction-to-ambient thermal resistance of BCM with 0.25" Heatsink*

The thermal resistance of the PCB to the surrounding environment in proximity to V•I Chips may be reduced by low profile heat sinks surface mounted to the PCB.The PCB may also be coupled to a cold plate by low thermal resistance standoff elements as a means of achieving effective cooling for an array of V•I Chips, without a direct interface to their case.

CASE 3—Combined direct convection to the air and conduction to the PCB.

Parallel use of the V•I Chip internal thermal resistances (including Junction-to-Case and Junction-to-board) in series with external thermal resistances provides an efficient thermal management strategy as it reduces total thermal resistance. This may be readily estimated as the parallel network of two pairs of series configured resistors.

V•I Chip Bus Converter Level 1 DC Behavioral Model for 352 V to 11.0 V, 240 W

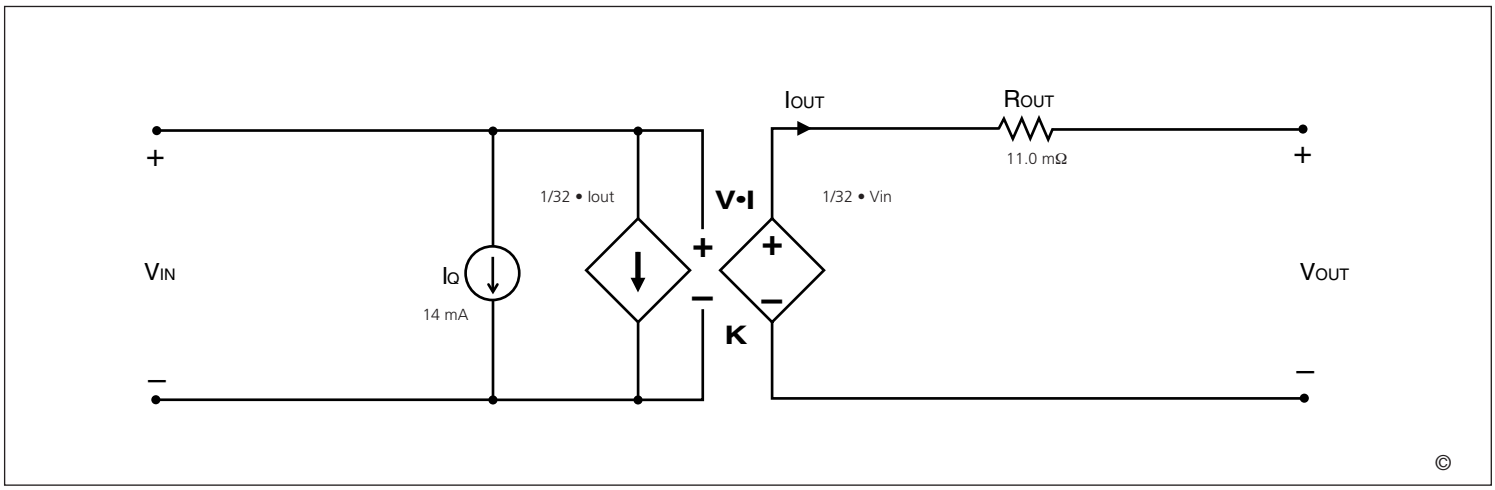


Figure 22*—This model characterizes the DC operation of the V•I Chip bus converter, including the converter transfer function and its losses. The model enables estimates or simulations of output voltage as a function of input voltage and output load, as well as total converter power dissipation or heat generation.*

V•I Chip Bus Converter Level 2 Transient Behavioral Model for 352 V to 11.0 V, 240 W

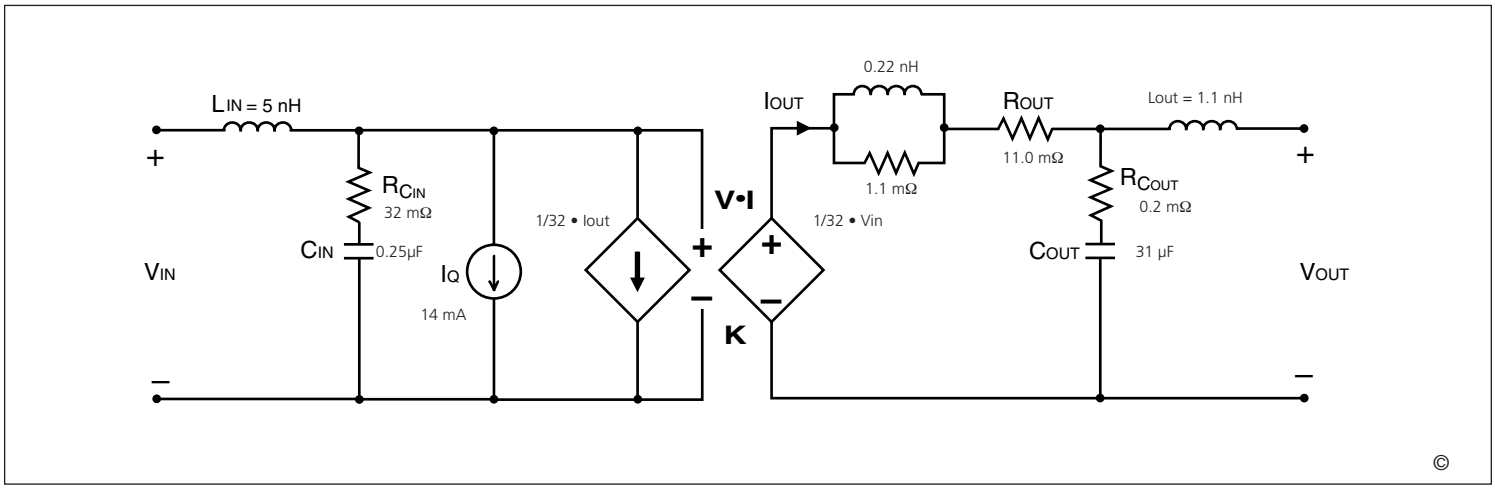


Figure 23*—This model characterizes the AC operation of the V•I Chip bus converter including response to output load or input voltage transients or steady state modulations. The model enables estimates or simulations of input and output voltages under transient conditions, including response to a stepped load with or without external filtering elements.*

Input Impedance Recommendations

To take full advantage of the BCM capabilities, the impedance presented to its input terminals must be low from DC to approximately 5 MHz. The source should exhibit low inductance (less than 100 nH) and should have a critically damped response. If the interconnect inductance exceeds 100 nH, the BCM input pins should be bypassed with an RC damper (e.g., 2 µF in series with 0.3 ohm) to retain low source impedance and stable operations. Given the wide bandwidth of the BCM, the source response is generally the limiting factor in the overall system response.

Anomalies in the response of the source will appear at the output of the BCM multiplied by its K factor. The DC resistance of the source should be kept as low as possible to minimize voltage deviations. This is especially important if the BCM is operated near low or high line as the over/under voltage detection circuitry could be activated.

Input Fuse Recommendations

V•I Chips are not internally fused in order to provide flexibility in configuring power systems. However, input line fusing of V•I Chips must always be incorporated within the power system. A fast acting fuse should be placed in series with the +IN port.

Applying the BCM

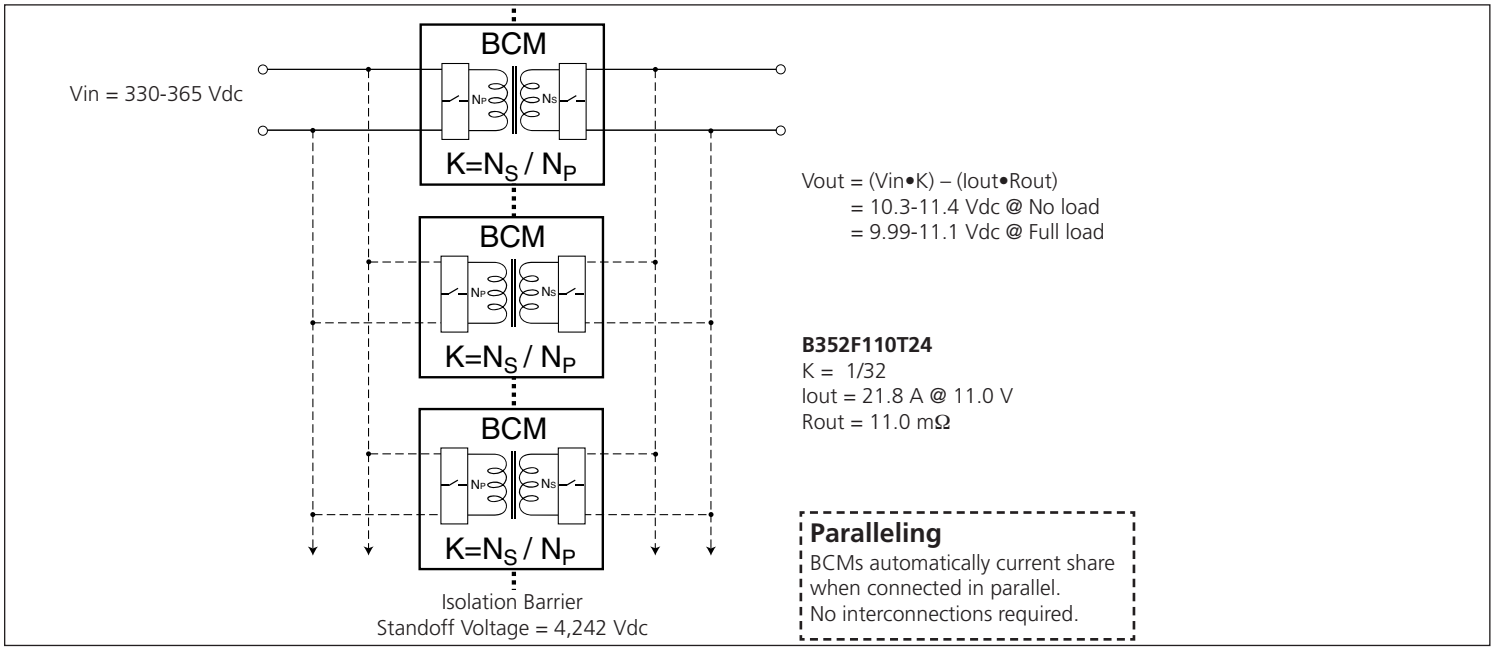


Figure 24*—The BCM provides an isolated output proportional to its input. It is easily parallelable to create high power arrays and/or for N+M redundancy.*

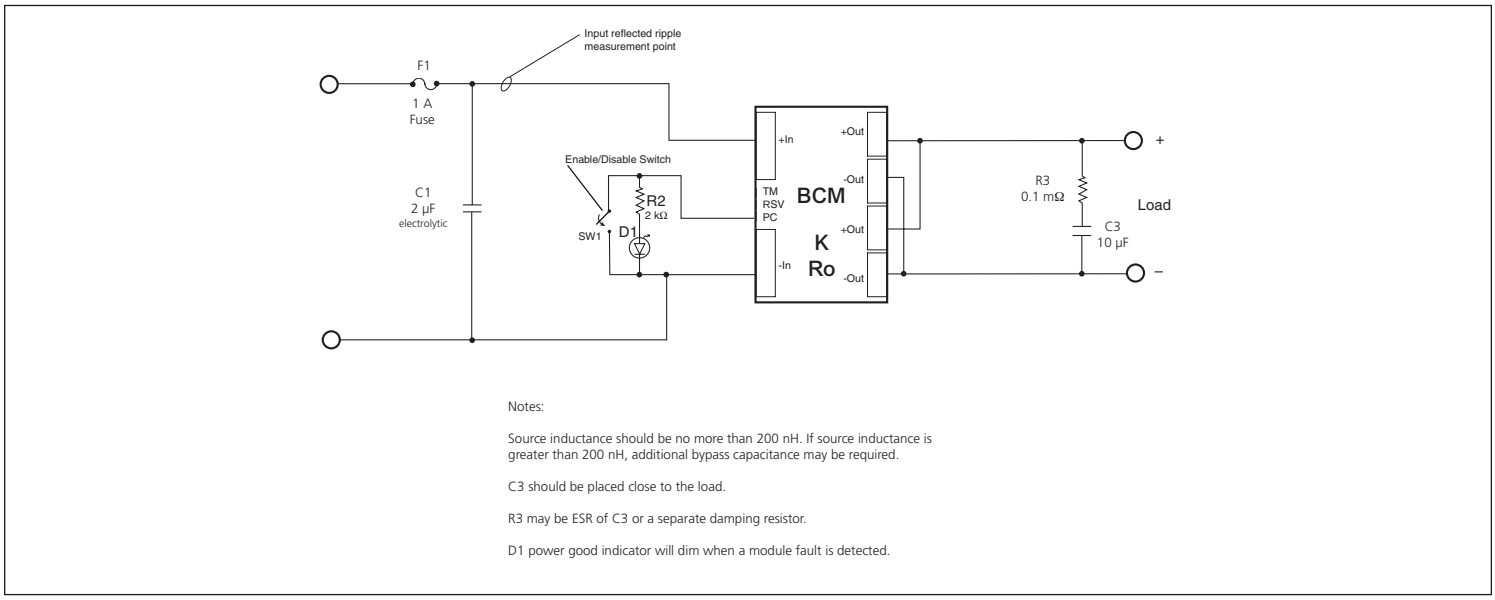


Figure 25*—BCM test circuit*

V•I Chip soldering recommendations

V•I Chip modules are intended for reflow soldering processes. The following information defines the processing conditions required for successful attachment of a V•I Chip to a PCB. Failure to follow the recommendations provided can result in aesthetic or functional failure of the module.

Storage

V•I Chip modules are currently rated at MSL 5. Exposure to ambient conditions for more than 48 hours requires a 24 hour bake at 125°C to remove moisture from the package.

Solder paste stencil design

Solder paste is recommended for a number of reasons, including overcoming minor solder sphere co-planarity issues as well as simpler integration into overall SMD process.

63/37 SnPb, either no-clean or water-washable, solder paste should be used. Pb-free development is underway.

The recommended stencil thickness is 6 mils. The apertures should be 0.9-0.9:1.

Pick and place

Modules should be placed within ±5 mils.to maintain placement position, the modules should not be subjected to acceleration greater than 500 in/sec^2 prior to reflow.

Reflow

There are two temperatures critical to the reflow process; the solder joint temperature and the module's case temperature. The solder joint's temperature should reach at least 220°C, with a time above liquidus (183°C) of ~30 seconds.

The module's case temperature must not exceed 208 °C at anytime during reflow.

Because of the ΔT needed between the pin and the case, a forced-air convection oven is preferred for reflow soldering. This reflow method generally transfers heat from the PCB to the solder joint. The module's large mass also reduces its temperature rise. Care should be taken to prevent smaller devices from excessive temperatures. Reflow of modules onto a PCB using Air-Vac-type equipment is not recommended due to the high temperature the module will experience.

Inspection

The solder joints should conform to IPC 12.2

- Properly wetted fillet must be evident.
- Heel fillet height must exceed lead thickness plus solder thickness.

Removal and rework

V•I Chip modules can be removed from PCBs using special tools such as those made by Air-Vac. These tools heat a very localized region of the board with a hot gas while applying a tensile force to the component (using vacuum). Prior to component heating and removal, the entire board should be heated to 80-100°C to decrease the component heating time as well as local PCB warping. If there are adjacent moisture-sensitive components, a 125°C bake should be used prior to component removal to prevent popcorning. V•I Chip modules should not be expected to survive a removal operation.

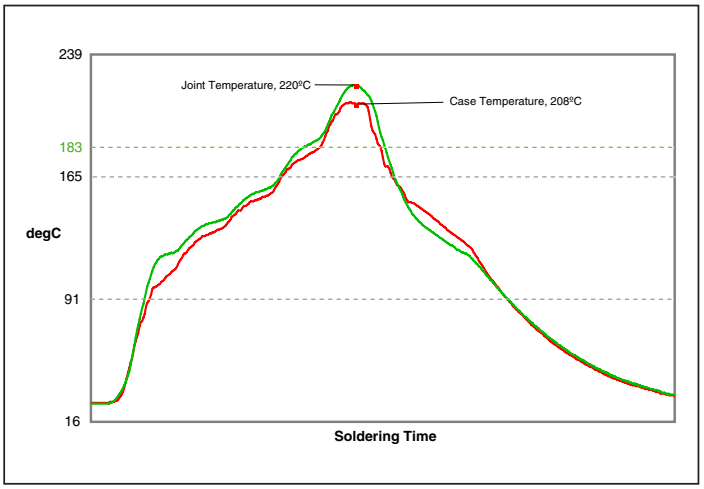


Figure 26—*Thermal profile diagram*

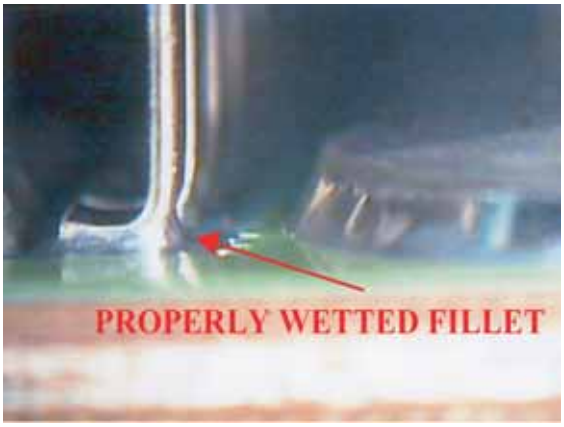


Figure 27— *Properly reflowed V•I Chip J-Lead*

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Vicor Corporation
25 Frontage Road
Andover, MA, USA 01810
Tel: 800-735-6200
Fax: 978-475-6715

email
Vicor Express: vicorexp@vicr.com
Technical Support: apps@vicr.com