30V/4A Half Bridge Driver

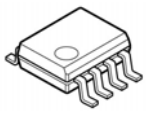
■ GENERAL DESCRIPTION

The **NJW4800** is a general purpose, half bridge power driver capable of supplying 4A current. The internal gate driver drives high-side/low-side power MOSFET; therefore, it has fast switching.

Additionally, it has protection features such as over current protection and thermal shutdown.
And in the case of failure, it can output a fault flag.

It is suitable for power switching applications of DSP/micro controller.

■ PACKAGE OUTLINE

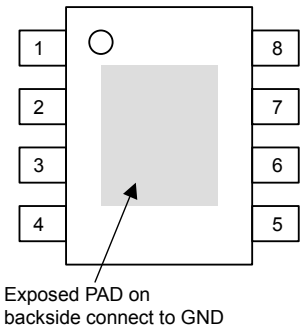


NJW4800GM1

■ FEATURES

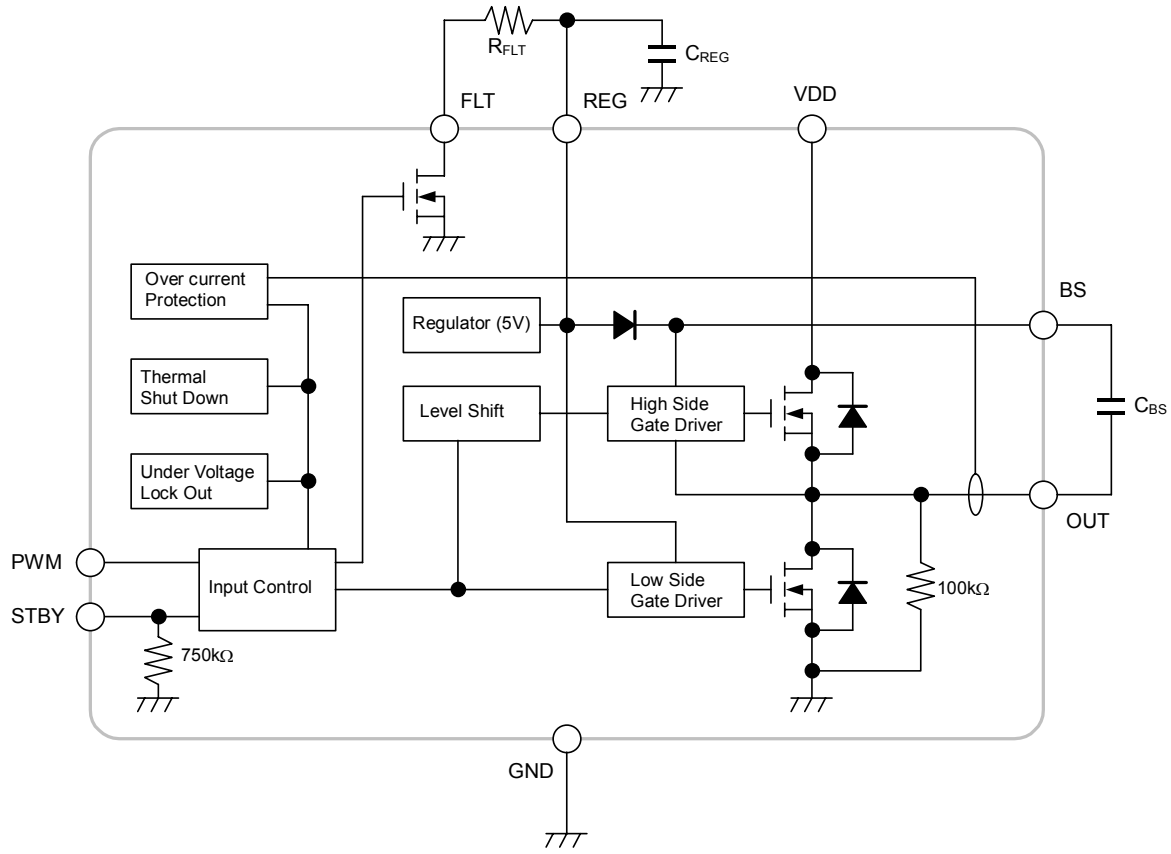
- Output Switch Current ±4A
- Operating Voltage 7.5V to 30V
- Up to 1.2MHz Switching Frequency
- Thermal Shut Down
- Over Current Protection
- Under Voltage Lockouts
- Fault Indicator Output
- Stand-by Current I_{QOFF} =3μA typ.
- High Heat Radiation Package
- Package Outline HSOP8

■ PIN CONFIGURATION



PIN FUNCTION
1. PWM
2. VDD
3. OUT
4. GND
5. BS
6. STBY
7. REG
8. FLT

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
Supply Voltage	V^+	35	V	VDD-GND pin
Input Voltage	V_{STBY} V_{PWM}	-0.3 ~ 6	V	STBY, PWM-GND pin
FLT pin Voltage	V_{FLT}	-0.3 ~ 6	V	FLT-GND pin
BS pin Voltage	V_{BS}	40	V	BS-GND pin
BS-OUT pin Voltage	V_{BS-OUT}	-0.3 ~ 6	V	BS-OUT pin
Power Dissipation	P_D	900 (*1) 3100 (*2)	W	–
Operating Junction Temperature	T_j	-40 ~ +150	°C	–
Operating Temperature Range	T_{opr}	-40 ~ +85	°C	–
Storage Temperature Range	T_{stg}	-50 ~ +150	°C	–

■ RECOMMENDED OPERATING CONDITIONS (Ta=25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARKS
Operating Voltage	V_{opr}	7.5	–	30	V	VDD-GND pin
Output Switch Current	I_{OM}	0	–	4	A	OUT pin
Input Voltage	V_{STBY}, V_{PWM}	0	–	5.5	V	STBY, PWM-GND pin
FLT pin Voltage	V_{FLT}	0	–	V_{REG1}	V	FLT-GND pin

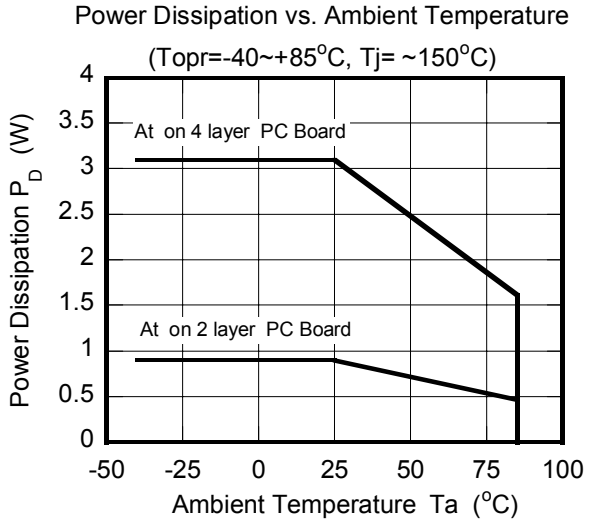
■ THERMAL CHARACTERISTICS (Ta=25°C)

PARAMETER	SYMBOL	THERMAL RESISTANCE	UNIT
Junction-to- Ambient Temperature	θja	139 (*1) 40 (*2)	°C/W
Junction-to-Case	ψjt	19 (*1) 3.7 (*2)	°C/W

(*1): Mounted on glass epoxy board based on EIA/JEDEC. (76.2 × 114.3 × 1.6mm: 2-Layers)

(*2): Mounted on glass epoxy board based on EIA/JEDEC.

(76.2 × 114.3 × 1.6mm: 4-Layers Internal foil area: 74.2 × 74.2mm)



■ ELECTRICAL CHARACTERISTICS (Unless otherwise noted, V^+=12V, V_{STBY}=0V, C_{BS}=0.1μF, C_{REG}=1μF, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
General Characteristics						
Quiescent Current 1 (Operating)	I_{Q1}	V_{PWM}=0V	–	1	2	mA
Quiescent Current 2 (Switching)	I_{Q2}	V_{PWM}=0V to 3V, f_{PWM}=1.2MHz	–	9	14	mA
Quiescent Current 3 (Standby)	I_{QOFF}	V_{STBY}=5.5V, V_{PWM}=0V	–	3	10	μA
Output Block						
High-side SW ON Resistance	R_{DSH}	$I_{OSOURCE}$=1A, V_{BS-OUT}=5V	–	0.25	0.45	Ω
Low-side SW ON Resistance	R_{DSL}	I_{OSINK}=1A	–	0.25	0.45	Ω
Over Current Limit	I_{LIMIT}	High-side and Low-side	4	5.5	7	A
Output Rise Time	tr	V_{PWM}=0V to 3V	–	3	–	ns
Output Fall Time	tf	V_{PWM}=3V to 0V	–	3	–	ns
Dead Time	Dt	V_{PWM}=0V to 3V	–	20	–	ns
PWM Rise Delay Time	t_{d_ON}	V_{PWM}=0V to 3V	–	60	–	ns
PWM Fall Delay Time	t_{d_OFF}	V_{PWM}=3V to 0V	–	60	–	ns
OUT pin – VDD pin Potential Difference	V_{PDOV}	V^+=5.7V, I_{ORH}=1A	–	0.85	1.1	V
GND pin – OUT pin Potential Difference	V_{PDGO}	V^+=5.7V, I_{ORL}=1A	–	0.85	1.1	V
Output Pull-down Resistance	R_{PD}	V^+ =5.7V, V_{STBY}=5.5V	50	100	200	kΩ
Output Leak Current (High Side SW OFF)	$I_{OLEAKOUT}$	V^+=30V, V_{STBY}=5.5V, V_{OUT}=0V	–	–	1	μA
OUT pin Output Current (FLT Signal Output)	I_{O-FLT}	V^+=5.7V, V_{OUT}=0V	–	30	60	μA
Input Circuit Block						
STBY pin High Voltage (Standby Mode)	V_{IHSTBY}		2.4	–	5.5	V
STBY pin Low Voltage (Operating Mode)	V_{ILSTBY}		0	–	0.8	V
STBY pin Input Current	I_{ISTBY}	V_{STBY}=5.5V	–	0.01	1	μA
STBY Pull-down Resistance	I_{ISTBY}		500	750	1000	kΩ
PWM pin High Voltage	V_{IHPWM}		2.2	–	5.5	V
PWM pin Low Voltage	V_{ILPWM}		0	–	0.9	V
PWM pin Input Current	I_{IPWM}	V_{PWM}=5.5V	–	0.01	1	μA
Continuous Output High Time	t_{HPWM}	V_{PWM}=5.5V	140	300	–	μs
Under Voltage Lockout (UVLO) Block						
UVLO Release Voltage	V_{UVLO2}	V+ = L → H	5.9	6.6	7.3	V
UVLO Operation Voltage	V_{UVLO1}	V+ = H → L	5.65	6.35	7.05	V
UVLO Hysteresis Voltage	ΔV_{UVLO}	V_{UVLO2}-V_{UVLO1}	–	0.25	–	V

■ ELECTRICAL CHARACTERISTICS (Unless otherwise noted, V^+=12V, V_{STBY}=0V, C_{BS}=0.1μF, C_{REG}=1μF, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Internal Power Supply Circuit						
Output Voltage 1	V_{REG1}	I_{REG}=0mA	4.75	5	5.25	V
Line Regulation	$\Delta V_{REG-VDD}$	V^+=8 ~ 30V, I_{REG}=0mA	–	2	20	mV
Load Regulation	ΔV_{REG-IO}	I_{REG}=0 ~ 20mA	–	20	50	mV
REG pin Output Current	I_{OREG}	V_{REG1}×0.95, Input signal=500kHz	30	–	–	mA
Fault Function (FLT pin)						
Low Level Output Voltage	V_{LFLT}	I_{FLT}=500μA	–	0.25	0.5	V
OFF Leak Current	$I_{OLEAKFLT}$	V_{FLT}=5.5V	–	–	1	μA

■ PIN OPERATION TABLE

INPUT			OUTPUT			Mode
PWM	STBY	VDD	FLT	High-side SW	Low-side SW	
L	L	$V^+ \geq V_{RUVLO}$	ON	OFF	ON	Normal
H	L	$V^+ \geq V_{RUVLO}$	ON	ON (*3)	OFF	Normal
L	H	–	OFF	OFF	OFF	Stand-by
H	H	–	OFF	OFF	OFF	Stand-by
L	L	$V^+ < V_{DUVLO}$	OFF	OFF	OFF	UVLO
H	L	$V^+ < V_{DUVLO}$	OFF	OFF	OFF	UVLO

(*3) If PWM=H continues by t_{HPWM} or more and is input, it becomes low-side SW=ON during t_{HPWM}/128.

INPUT		OUTPUT			Mode
Tj	I_{OUT}	FLT	High-side SW	Low-side SW	
Tj >150°C	–	OFF	OFF	OFF	TSD
–	$I_{OUT} \geq I_{OM}$	OFF	OFF	OFF	OCP

■ TIMING CHART

Fig1. Output Rise/Fall Time, PWM Rise/Fall Delay Time

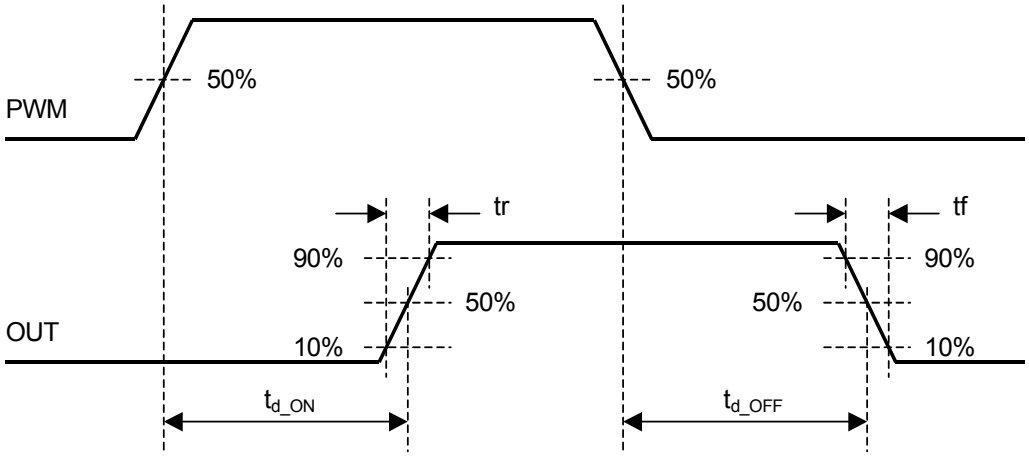


Fig2. Maximum Continuous Output Time (High-level)

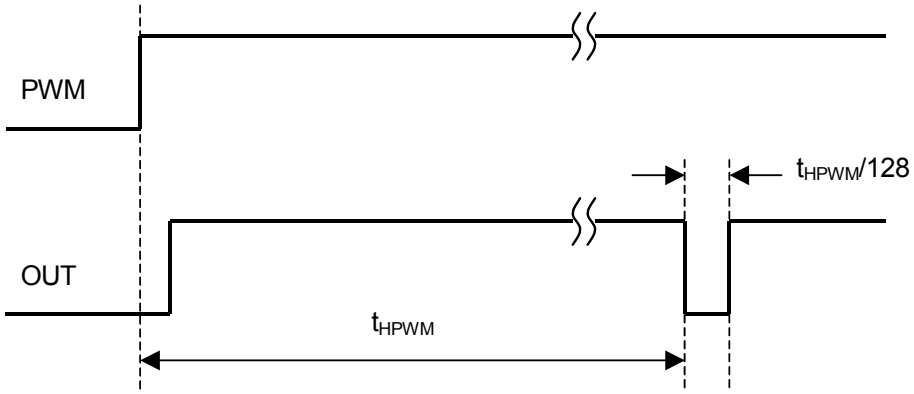
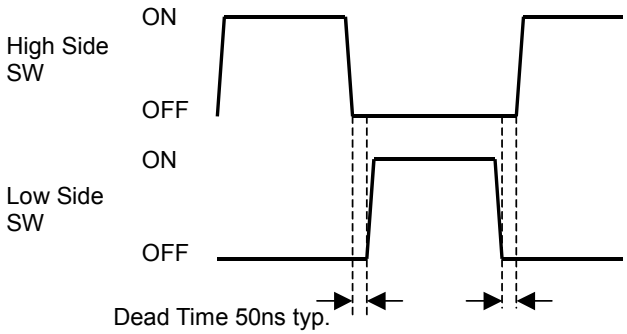
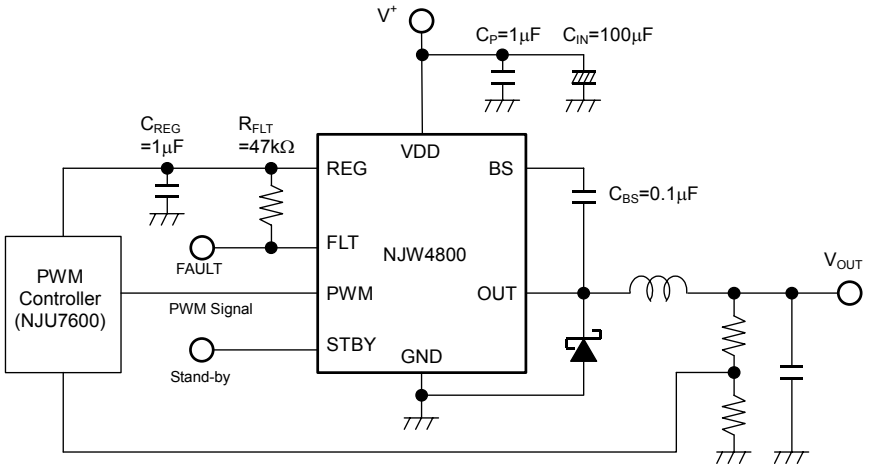


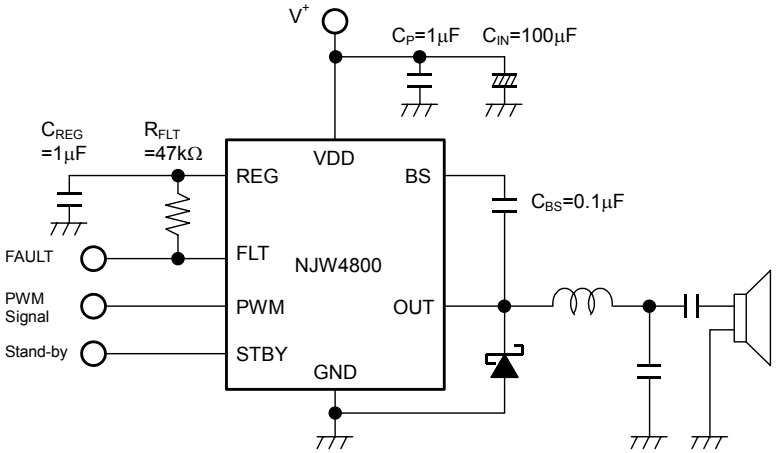
Fig3. Switching and Dead Time



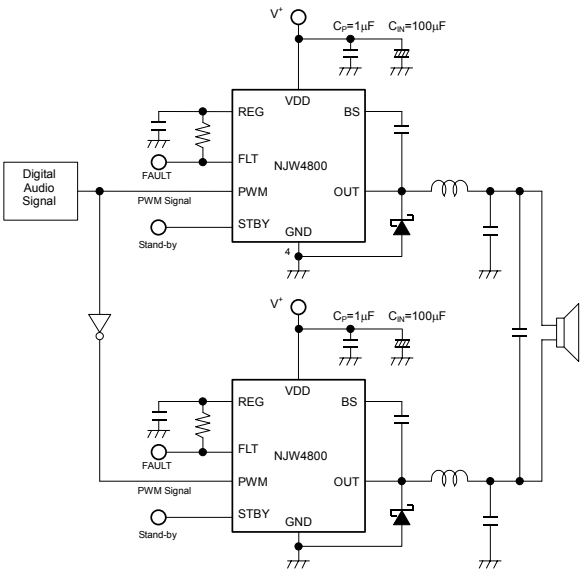
■ TYPICAL APPLICATIONS



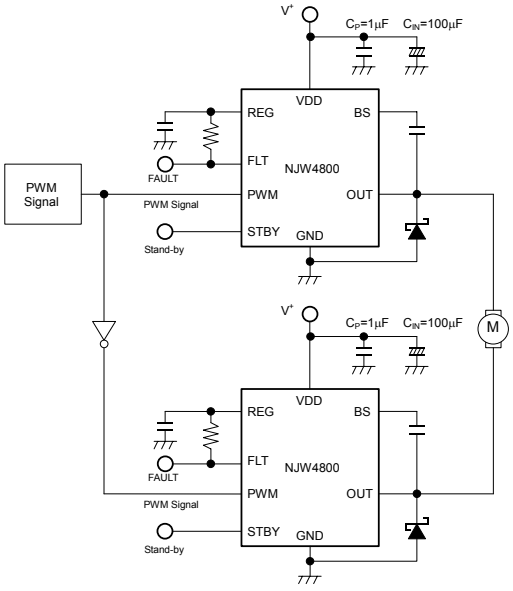
Synchronous PWM step down switching regulator



Class-D single ended audio amplifier



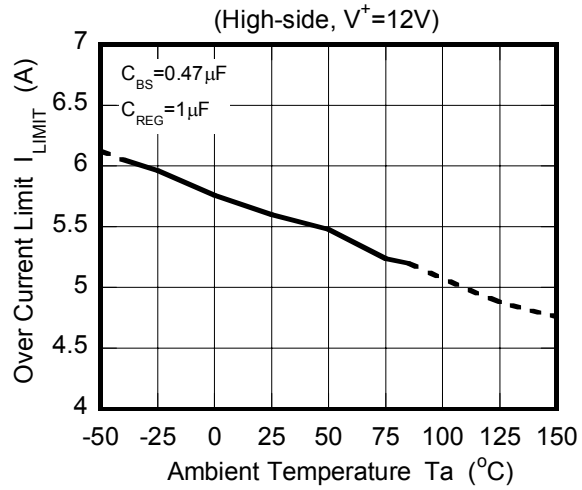
Class-D full bridge audio amplifier



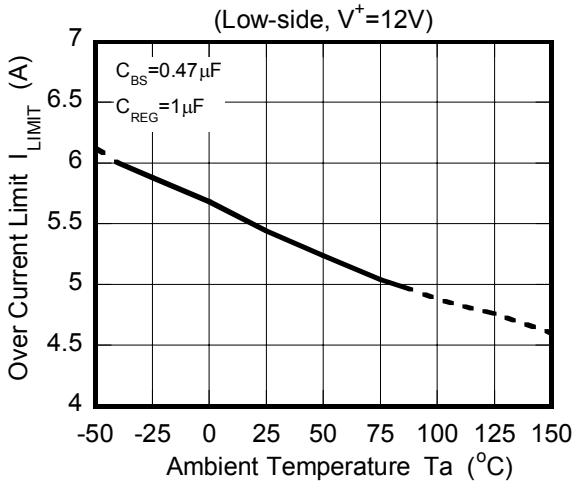
Full bridge motor driver

■ CHARACTERISTICS

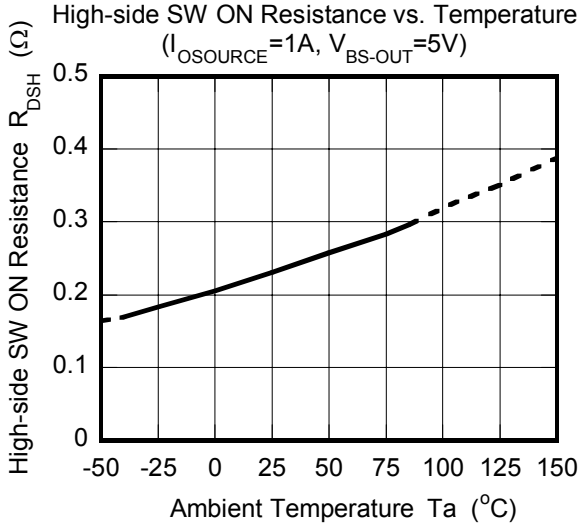
Over Current Limit vs. Temperature
(High-side, V^+=12V)



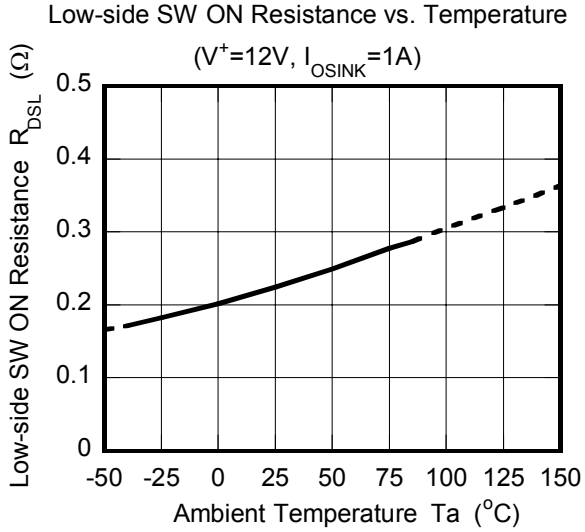
Over Current Limit vs. Temperature
(Low-side, V^+=12V)



High-side SW ON Resistance vs. Temperature
($I_{OSOURCE}$=1A, V_{BS-OUT}=5V)



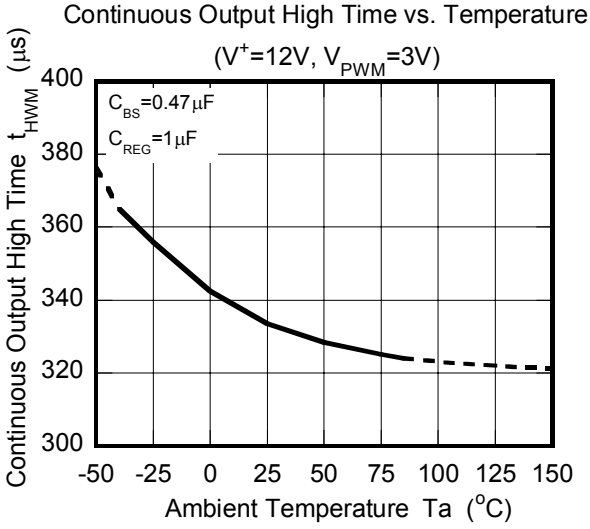
Low-side SW ON Resistance vs. Temperature
(V^+=12V, I_{OSINK}=1A)



■ CHARACTERISTICS

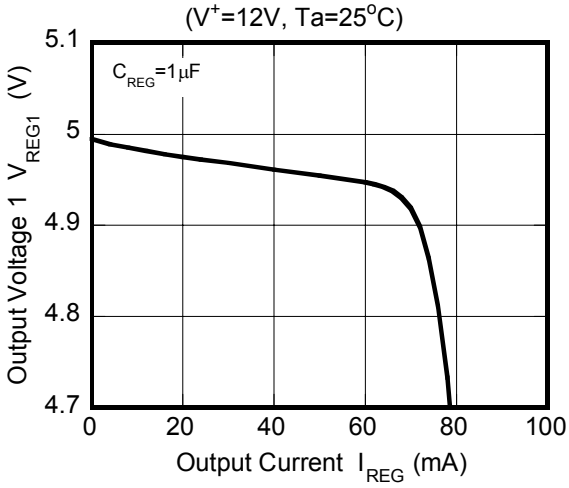
Continuous Output High Time vs. Temperature

(V^+=12V, V_{PWM}=3V)

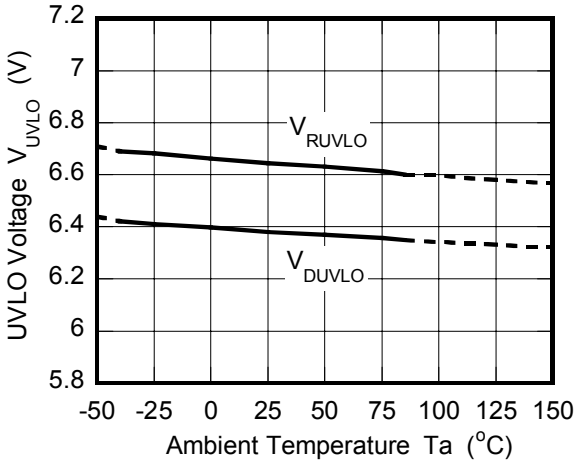


Internal Power Supply Circuit Load Regulation

(V^+=12V, Ta=25°C)

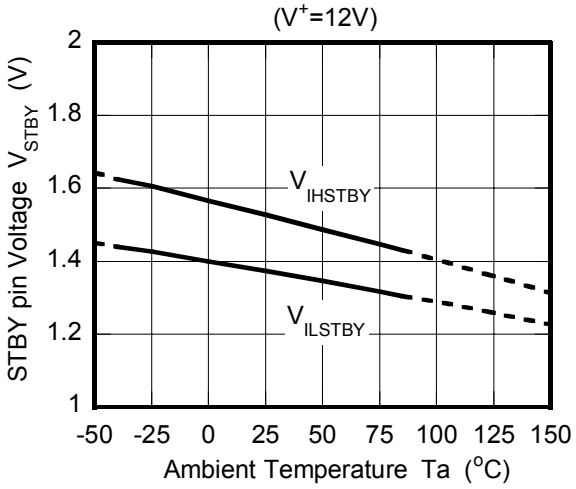


Under Voltage Lockout Block vs. Temperature



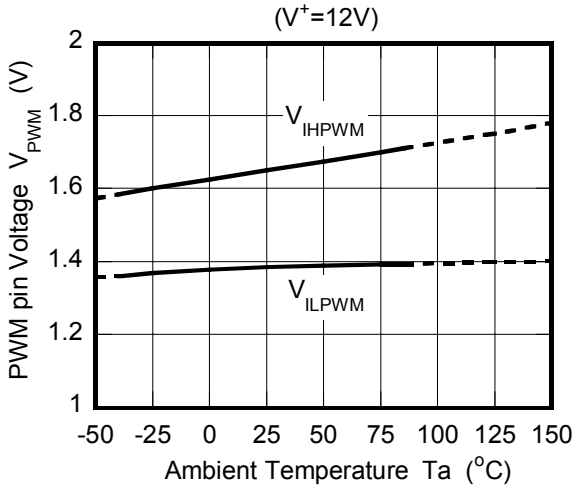
STBY pin Voltage vs. Temperature

(V^+=12V)



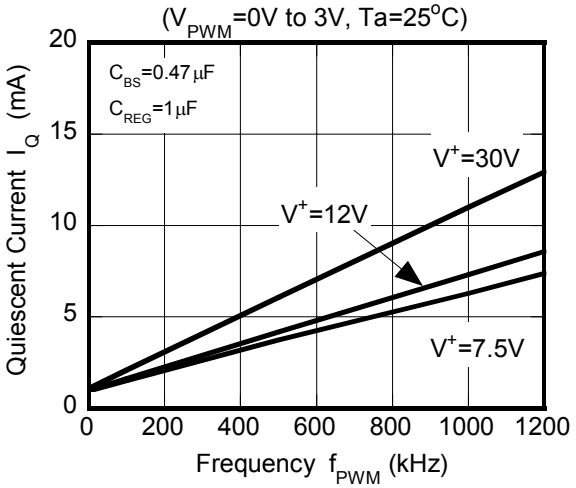
PWM pin Voltage vs. Temperature

(V^+=12V)



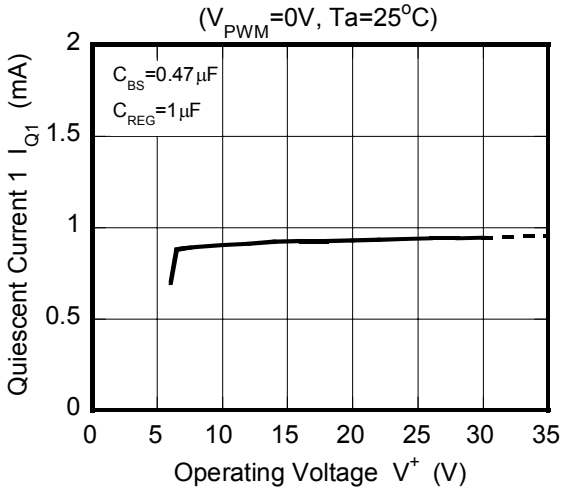
Frequency vs. Operating Voltage

(V_{PWM}=0V to 3V, Ta=25°C)

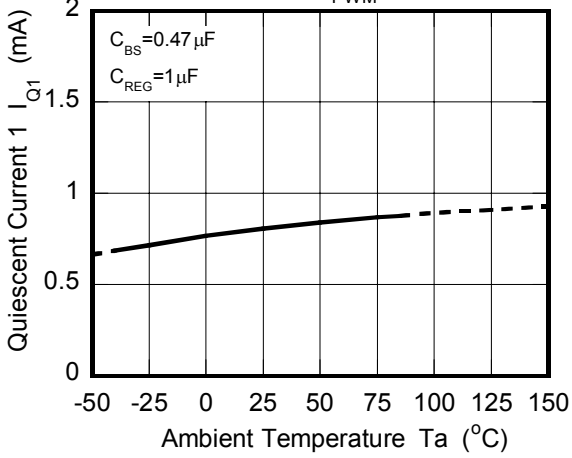


■ CHARACTERISTICS

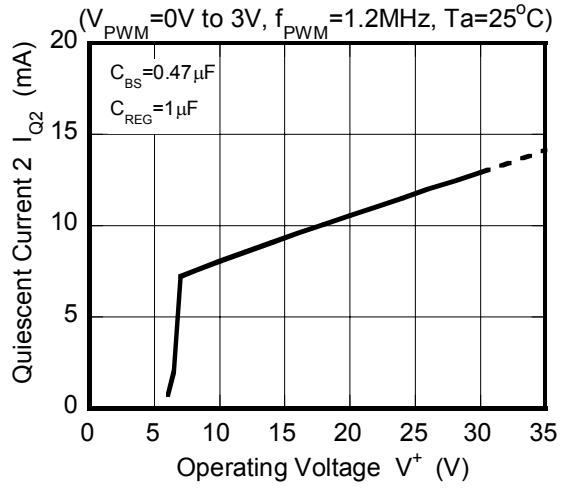
Quiescent Current 1 vs. Operating Voltage
(V_{PWM}=0V, Ta=25°C)



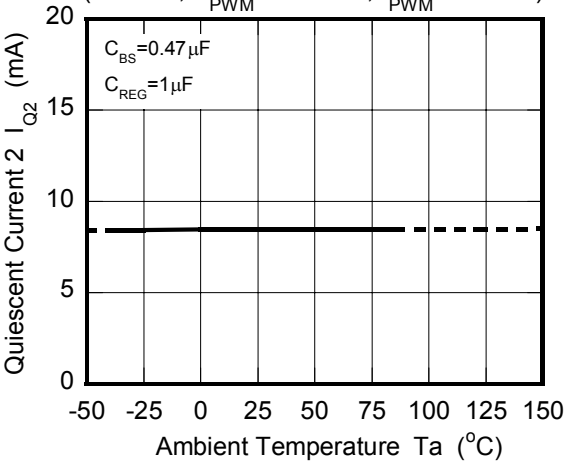
Quiescent Current 1 vs. Temperature
(V^+=12V, V_{PWM}=0V)



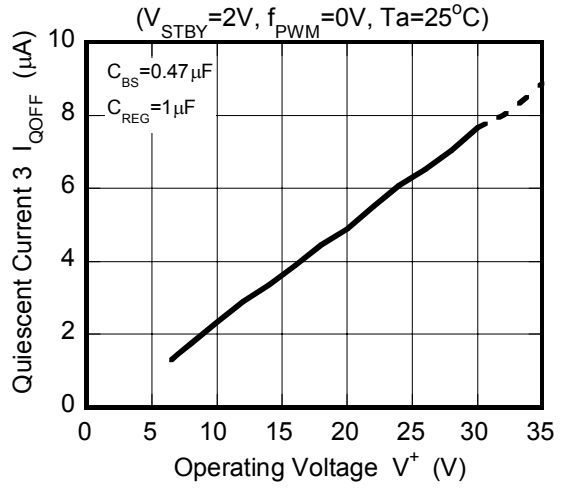
Quiescent Current 2 vs. Operating Voltage
(V_{PWM}=0V to 3V, f_{PWM}=1.2MHz, Ta=25°C)



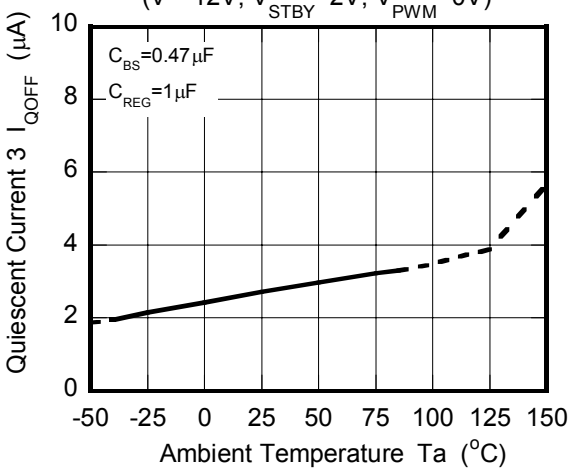
Quiescent Current 2 vs. Temperature
(V^+=12V, V_{PWM}=0V to 3V, f_{PWM}=1.2MHz)



Quiescent Current 3 vs. Operating Voltage
(V_{STBY}=2V, f_{PWM}=0V, Ta=25°C)



Quiescent Current 3 vs. Temperature
(V^+=12V, V_{STBY}=2V, V_{PWM}=0V)



■ PIN DESCRIPTION

PIN NUMBER	PIN NAME	FUNCTION
1	PWM	PWM Signal Input Terminal As for Control Logic, Refer to PIN OPERATION TABLE (page.5)
2	VDD	Power Supply Terminal You should connect capacitor (AL and MLCC) for reducing Input Impedance.
3	OUT	Output Terminal The High-side/Low-side Switch are Limited to 5.5A(typ.) by Over Current Protection Circuit.
4	GND	Ground Terminal
5	BS	Boot Strap Output Terminal Boot Strap Output drives the High-side Switch. You should connect capacitor larger than 0.1μF between BS Terminal (5-pin) and Out Terminal (3-pin).
6	STBY	Standby Terminal NJW4800 becomes standby status by High Level NJW4800 operates by Low Level
7	REG	Built-in Regulator (5V) Output Terminal You should connect capacitor larger than 1μF for stable output.
8	FLT	Fault Signal Output Terminal It is Open Drain Output Type. You should connect through Pull-up Resister to REG Terminal (7-pin) or External Power Supply. It outputs Low Level under normal operating condition and outputs High Level under Abnormal Conditions.
–	Exposed PAD	Connected to 4pin (Ground Terminal)

■ FUNCTIONAL EXPLANATION

● High-side, Low-side Switch

The SW output drives the load. It is controlled by the logic input signal from PWM terminal at PWM. When the signal at PWM is high (above 2.2V), the high-side switch is turned on. When the signal at PWM is low (less than 0.9V), the low-side switch is turned on.

The NJW4800 uses built-in Nch MOSFETs (R_{ON}=0.25Ω typ.) for both the high-side and low-side switches. The high-side SW gate is driven with V^++5V that generated by bootstrap. The high-side SW turn on time is limited to 300μsec(typ.). (ex. Fig2)

There is a dead time region (20nsec (typ.): design value) to prevent short circuit (high-side and low-side) where both the high-side and low-side switches are off. (ex. Fig3)

The NJW4800 is suitable for high-frequency switching regulator. The NJW4800 operates at frequencies up to 1.2MHz.

The OUT terminal is pulled down inside with 100kΩ, compensates the leak current of the High-side SW.

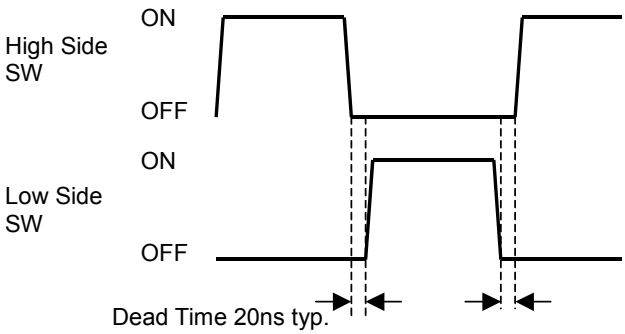


Fig3. SW Function and Dead Time Relation

● Over Current Protection Function

The internal over-current protection circuit monitors the flow currents of both the high-side and low-side switches. The over-current protection circuit operates at 5.5A (typ.) and stops the SW operation. The FLT signal is output from FLT terminal at the same time. The over-current protection operation is released at the PWM input signal falling edge. (ex. Fig4)

If OUT terminal is shorted directly to GND, a large surge current is flowing for fast current change and may exceed current limit. Because that time big electric power consumption occurs instantaneously in NJW4800, you should design sufficient heat dissipation.

When a load condition is inductive property, a reverse direction current flows to the high-side and low-side SW body diode by inductive kickback.

The built-in over-current protection circuit has not aimed at protection against the inductive kickback. Therefore, an external diode should be considered usage against reverse-current regeneration according to the kind of the application.

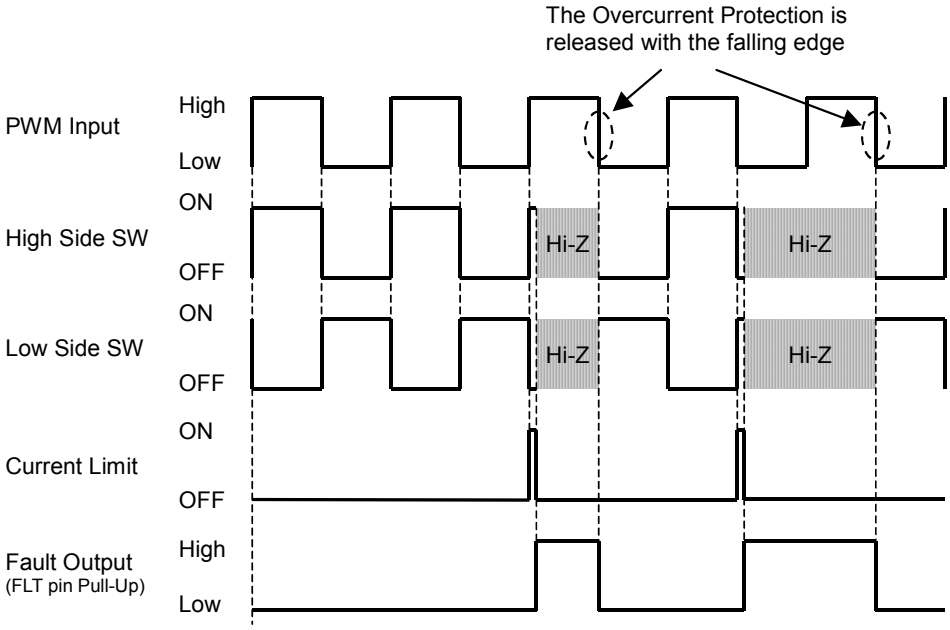
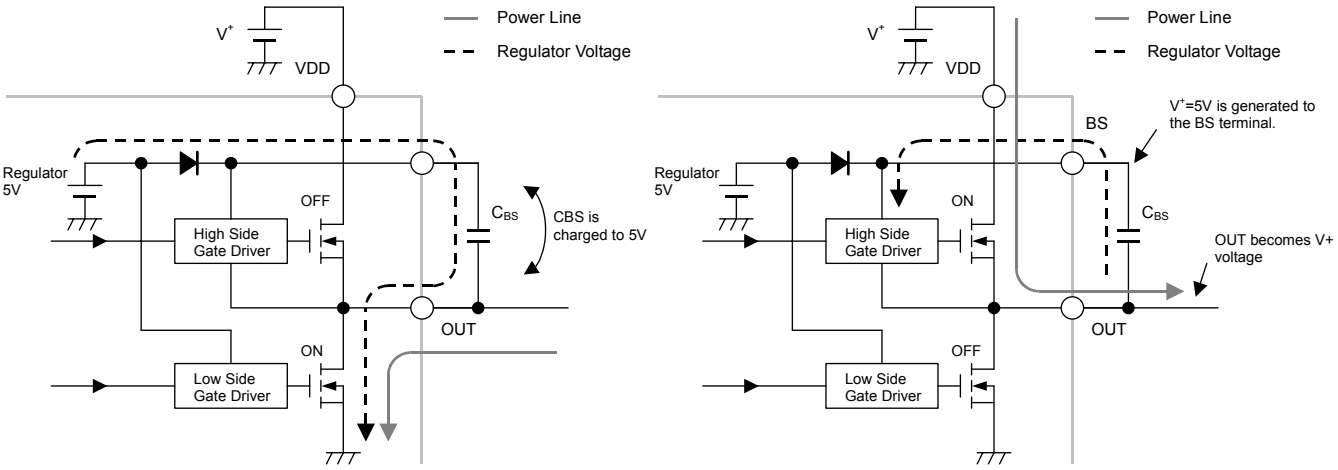


Fig4. Timing Chart of High-side/Low-side Switch at Over Current Protection Operating

● Boot Strap

In order to drive the gate of the high side SW, the voltage that is higher than power supply voltage is necessary. The bootstrap condenser generates the power supply voltage of V^++5V to BS terminal and it supplies the power to the gate of the high side SW. As Shown as Fig5 in detail.



High-side SW: OFF
Low-side SW: ON

High-side SW: ON
Low-side SW: OFF

Fig5. High-side SW driven by Boot Strap

You should connect bootstrap condenser larger than C_{BS}=0.1μF between BS Terminal and OUT Terminal. The internal counter decides the bootstrap condenser Charge and Discharge time.

A capacitor discharge time (t_{HPWM}) for High-side SW Maximum ON Time is 300ms (typ).

A capacitor charge time (t_{HPWM} / 128) for Low-side SW Minimum ON Time is 2.34μs (typ).

● Built-in Regulator

The REG Terminal outputs Reference Voltage (5V). It can be used as generating of the voltage for the bootstrap or a power supply voltage for other device(s). You should connect capacitor (C_{REG}) larger than 1μF for stable regulator output.

This regulator current capability (I_{OREG}) is 30mA (min) at (V_{REG1}×0.95). This regulator over current protection is a drooping characteristic type. It has drooping characteristic at over current protection function.

● Thermal Shut Down Function

When NJW4800 chip temperature exceeds the 170°C, internal thermal shutdown circuit operates and SW function is stopped. The Fault signal is output simultaneously from the FLT terminal. In order to return SW operation, you should make chip surface temperature (Junction Temperature: Tj) below the 150°C*.

This function is a circuit to prevent IC at the high temperature from malfunctioning and is not something that urges positive use. You should make sure to operate inside the junction temperature range rated. (* Design value)

● Under Voltage Lockout(UVLO)

The UVLO circuit operating is released above V^+=6.6V(typ.) and IC operation starts. When power supply voltage is low, because the UVLO circuit operates, IC does not operate. There is 0.25V width hysteresis voltage at rise and decay of power supply voltage. Hysteresis prevents the malfunction at the time of UVLO operating and releasing.

● FAULT Signal Output

This Terminal is Open Drain Output Type. You should connect through Pull-up Resister to REG Terminal (7-pin) or External Power Supply. It outputs Low Level under normal operating condition and outputs High Level under Abnormal Conditions.

The following information is output as FAULT signal.

- Stop Operation at Under Voltage Lockout (UVLO)
- Over Current Protection Function
- Thermal Shut Down

At the time of standby state, it outputs High Level.

When outputting the FAULT signal, it has stopped SW operation, but the internal regulator continues operation. Because of this 30mA it is flowing via the OUT terminal from the regulator circuit.

● Standby Function

NJW4800 stops the operating and becomes standby status when 2.4V or more is supplied to STBY terminal. You should connect the terminal with GND level to prevent the malfunction by a noise when you do not use this function.

■ APPLICATION TIPS

In the application that does a high-speed switching of NJW4800, because the current flow corresponds to the input frequency, the substrate (PCB) layout becomes an important.

NJW4800 is driving the High-side/Low-side SW gate with high speed to reduce switching losses. The transient voltage is generated by parasitic inductance and a high-speed current change of high side and low side SW.
You should attempt the transition voltage decrease by making a current loop area minimize as much as possible. Therefore, you should make a current flowing line thick and short as much as possible.

You should insert a bypass capacitor between VDD terminal and GND terminal to prevent malfunction by generating over voltage and/or exceed maximum input voltage rating. The recommended bypass capacitor is 1μF or more high frequency capacitor.

A 100μF aluminum electrolysis capacitor is recommended for smoothing condenser. However, you should use larger capacitor by sufficient evaluation (assessment) due to load condition and/or application use environment. (There is a possibility that the supply voltage rises by inductive kickback when the supply current of the inductive load is large.)
The bypass capacitors should be connected as much as possible near VDD terminal.

Ex. Bill of Materials

Components	Parts Name	Functions	Manufacturers
C_{IN}	—	Aluminum-Cap.	Nippon Chemi-con
C_P	GRM21BB11H104KA01B	Ceramic-Cap. 0.1μF, 50V (B-val)	Murata
C_{REG}	GRM31MB31H105KA87B	Ceramic-Cap. 1μF, 50V (B-val)	Murata
C_{BS}	GRM21BR71H474KA88B	Ceramic-Cap. 0.1μF, 50V (X7R-val)	Murata
R_{FLT}	RK73B1JT473	47kΩ	KOA

MEMO