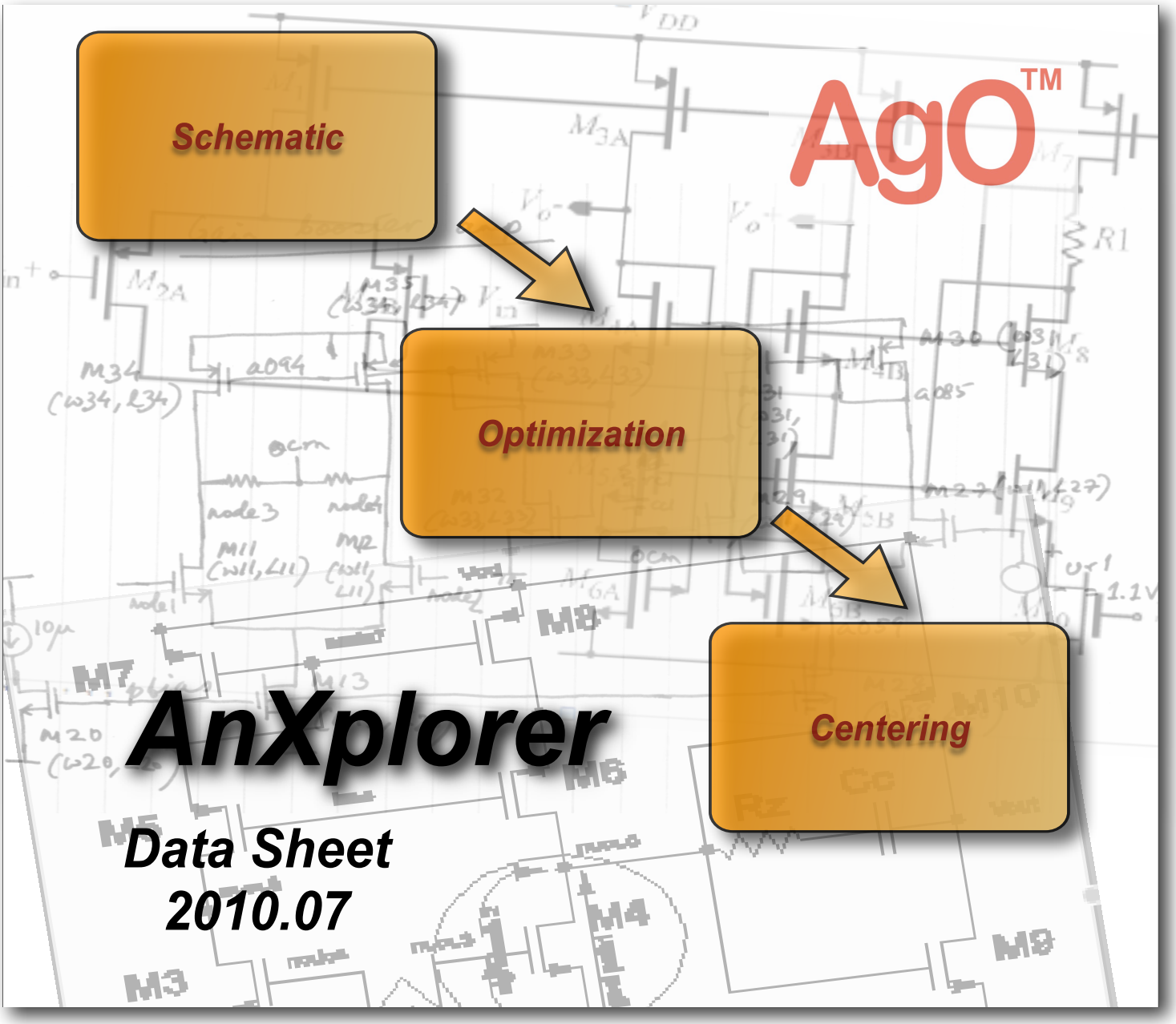

ANXPLORER: EDA TOOL FOR SCHEMATIC LEVEL OPTIMIZATION OF ANALOG & RF CIRCUITS

OVERVIEW

Market analysis

Demand for faster devices consuming less power has revived interest in analog circuits for interface, data conversion, amplification, and even fast signal processing. As a result, Analog and Mixed signal (AMS) IC (Integrated Circuit) industry is growing much faster than its digital counterpart. According to market analysis, AMS IC business is expected to grow at 10% CAGR while the overall semiconductor market is growing at 5%. It will therefore cross $60 billion by 2010 from $37 billion in 2005. Such an explosive growth involves development of numerous circuits in a short period of time.

Challenges in analog design

Analog circuits account for approximately 2% or less of the total transistor count. However, they take up around 20% of total IC area, and consume around 40% of the total design effort. Furthermore, analog circuits are also responsible for 50% of all design re-spins. The reason for the long development time and unpredictability is that analog design lacks adequate automation. The design flow is utterly effort intensive and dependent on individual skill and knowledge. Analog designers are in short supply, and it is difficult to grow the numbers quickly. This throws a management challenge where it is needed to deliver a lot more in a shorter time with very little resource. The need of the hour for the industry is, therefore, a design synthesis tool for analog and RF which which address issues like centering, mismatch, noise, and post layout parasitics.

PRODUCT OFFERING

AnXplorer is a software solution to address the above problem. It is a simulation and design equation based synthesis and optimization tool for analog and radio frequency (RF) circuits, by efficient design space exploration. At the heart of it is a multi-

variate, muti-objective optimization algorithm for arbitrary cost functions having multiple local optima. It can be used by circuit designers to quickly explore different circuit schematics to identify the right choice. It also helps in finding a robust design solution against variations in the manufacturing process, temperature, and supply voltage. It takes as input an unsized SPICE netlist along with design specifications and constraints. It calls a SPICE simulator in a loop to evaluate the circuit at different test points. Finally, it produces an optimized and centered netlist.

Inputs

- **SPICE netlist** of circuit to be optimized, and/or a set of design equations the user wants to optimize.
- Set of **design objectives** which the circuit should meet and a set of constraints which must be honored. Any quantity which can be simulated and measured can be a design objective.
- Set of **design variables** which the tool can tune, along with their allowed range of values. Typically, these design variables represent transistor dimensions, bias voltages, etc.
- Set of "**corners**", including manufacturing process corners (e.g. fast, typical, slow), different temperatures and different supply voltages. *AnXplorer* optimizes the circuit to ensure that design objectives are met across these corners.

Outputs

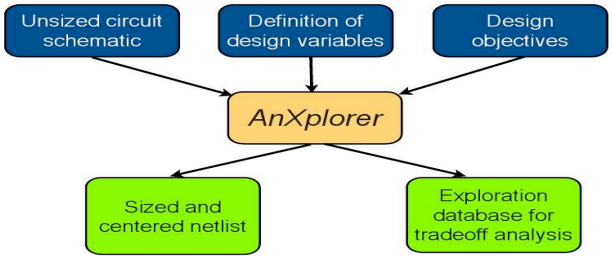

Figure 1: Inputs and outputs of *AnXplorer*

- An **optimized and centered circuit netlist**, which meets or exceeds the design objectives across all the user specified corners.
- An **exploration database**, which is a persistent storage for all design points explored by the tool. This database can be queried and used for effective trade-off analysis between conflicting design objectives.

Pictorially, the inputs and outputs are shown in figure 1. Figure 2 explains how *AnXplorer* automates the existing design flow.

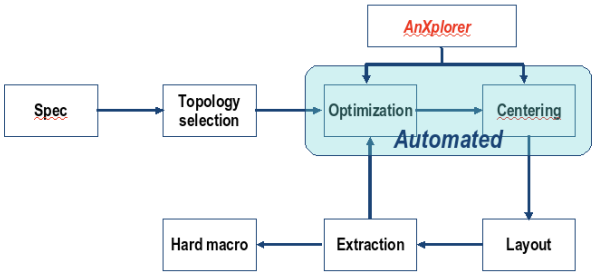

Figure 2: Analog design flow with *AnXplorer*

Currently, *AnXplorer* **works seamlessly with several industry standard SPICE simulators**.

DIFFERENTIATING FEATURES

Design equation based optimization: In addition to simulation based design optimization, *AnXplorer* also supports design equation based optimization, or a combination of both. Unlike gradient-search based tools, *AnXplorer* supports arbitrary functions with multiple local and global optima.

Hierarchical design objectives: Unlike a weight based prioritization of multiple objectives, commonly used in other optimization tools, *AnXplorer* employs a hierarchical arrangement for design objectives. The user specifies the relative order of importance of each objective, instead of a weight. This is specified in the form of a directed graph. The tool tries to achieve the objective with higher priority before optimizing the other objectives.

Trade-off analysis with exploration database: *AnXplorer* records all design points explored during the optimization process and these are stored in a persistent database. This database can be queried. This creates an effective tool for "what-if" analysis (how much can one objective be achieved, if another is constrained below a certain value?). It also enables trade-off analysis for conflicting objectives (e.g. circuit area and noise, speed and power) if all objectives cannot be realistically met.

Implicit objectives: In addition to explicit objectives specified by the user, AnXplorer imposes certain implicit objectives on the operating condition of devices. Transistors which are supposed to be in saturation are pushed deep into saturation. This ensures an inherently robust design.

VALUE ADDITION

Productivity improvement: *AnXplorer* improves engineering efficiency by at least 5X. This is achieved by automating the manual and routine job of sizing circuit elements to meet design objectives. This leads to faster time-to-market. The productivity improvement enabled by *AnXplorer* has other benefits as well. It helps engineers to quickly judge the suitability of any given schematic for a particular purpose, and thus helps in evaluating multiple options before selecting a topology. It also helps less experienced engineers to take up challenging design tasks.

Yield improvement: *AnXplorer* helps achieve a robust design point for any circuit, so that it meets its design objectives in the face of variation in the manufacturing process, temperature, and supply voltage. This is a major challenge in the current manual design flow, and is responsible for most silicon re-spins. *AnXplorer*, by rigorously exploring the design space for robust solutions, improves yield and increases the chances of first-time silicon success, thereby saving millions.

Porting across process nodes: As manufacturing processes change every day, it becomes necessary to port designs from one process node to another. This involves re-sizing the circuit elements so that the circuit meets its objectives in the new process. *AnXplorer* can automate this task. This is especially helpful for analog IP companies who often have to re-target the same design for different customer foundries.

EXAMPLES OF SIMULATION BASED OPTIMIZATION

Two-stage OpAmp

Source: Krasnicki, M. J., Phelps, R., Hellums, J. R., McClang, M., Rutenbar, R. A., Carley, L. R., "ASF: A practical simulation-based

methodology for the synthesis of custom analog circuits", Proc. ICCAD 2001, pp 350-357. Shown in figure 3.

Technology: IBM 0.5um BSIM3v3 models, obtained from http://www.mosis.org/test

METRIC	SPECIFICATION	RESULT
Gain	≥ 68 dB	72.6 dB
Unity gain BW	≥ 255 MHz	697 MHz
Phase margin	≥ 52 degrees	56 degrees
CMRR	≥ 55 dB	56.2 dB
PSRR (Vdd)	≥ 80 dB	86.5 dB
Slew rate	≥ 250 V/us	403 V/us
Propagation delay	≤ 2 ns	1.13 ns
Area	≤ 24000 sq. micron	6000 sq. micron

Table 1: Specification and optimization for two stage OpAmp

Ultra wide-band OpAmp

Source: Advanced VLSI Design Lab, Indian Institute of Technology, Kharagpur, shown in figure 4.

Technology: TSMC 0.18um BSIM3v3 models, obtained from http://www.mosis.org/test

METRIC	SPECIFICATION	RESULT
Gain	≥ 60 dB	67.5 dB
Unity gain BW	≥ 2 GHz	2.18 GHz
Phase margin	≥ 50 degrees	55 degrees
ICMR	-	0.4 - 1.5 V
CMRR	-	86 dB
PSRR (Vdd)	-	83 dB
Settling time	-	3 ns
Static power	≤ 50 mW	46 mW

Table 2: Specification and optimization for ultra wide band OpAmp

Missing entries in the specification column denote metrics which were not part of the optimization objectives, but measured post optimization.

High gain OpAmp

Source: Advanced VLSI Design Lab, Indian Institute of Technology, Kharagpur, shown in figure 5.

Technology: TSMC 0.18um BSIM3v3 models, obtained from http://www.mosis.org/test

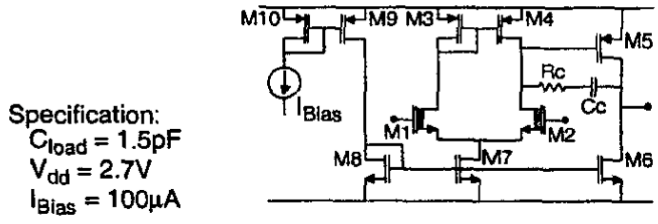

Figure 3: Two stage OpAmp schematic

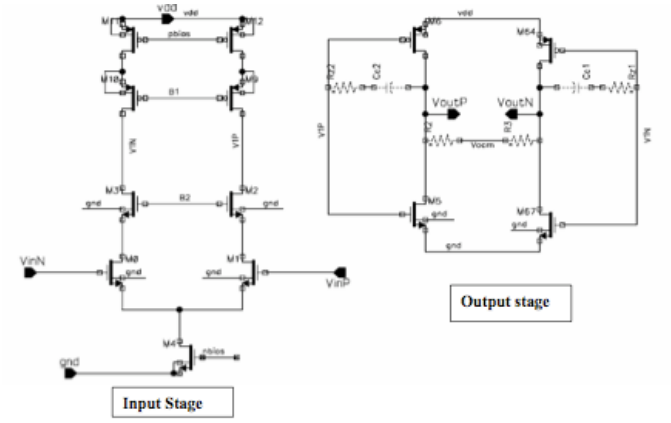

Figure 4: Ultra wide-band OpAmp schematic

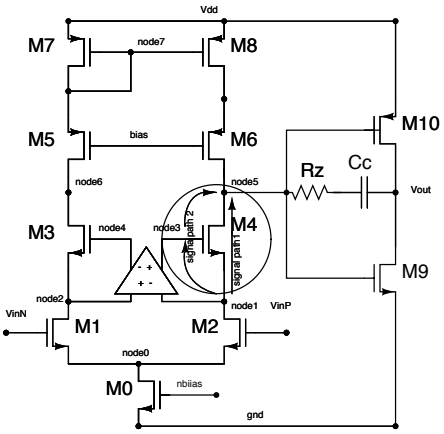

Figure 5: High gain OpAmp schematic, with gain-booster stage shown as a block.

METRIC	SPECIFICATION	RESULT
Gain	≥ 80 dB	94 dB
Unity gain BW	≥ 500 MHz	915 MHz
Phase margin	≥ 60 degrees	64 degrees
Static current consumption	≤ 25 mA	18 mA
Settling time	≤ 10 ns	3 ns

Table 3: Specification and optimization for high gain OpAmp

EXAMPLES OF EQUATION BASED OPTIMIZATION

AnXplorer can perform general equation based function optimization as well. It is especially suitable for any cost function which is known to have multiple local and global minima. A few examples of well known benchmark functions for optimization algorithms are shown next.

Rastrigin's function

A visualization of Rastrigin's function for 2 variables is shown in figure 6. The function is highly multimodal with numerous local optima. The global optima lies at the point where all variables have the value 0. AnXplorer has been used to find the global optima of this function for many (≥8) variables.

Griewank's function

Another example of a multimodal function with numerous local optima is the Griewank's function. The visualization for 2 variables is shown in figure 7. Here, too, the global minimum lies at the point where all variables are 0. AnXplorer successfully finds this point for several variables.

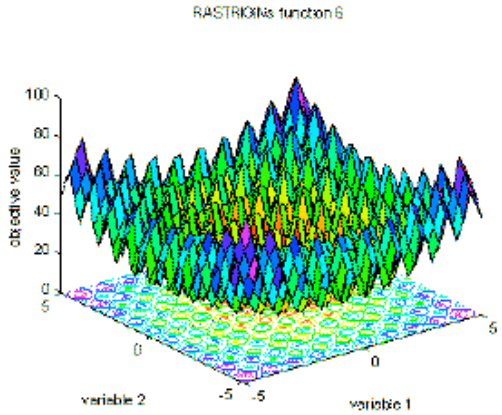

Figure 6: Visualization of Rastrigin's function for 2 variables

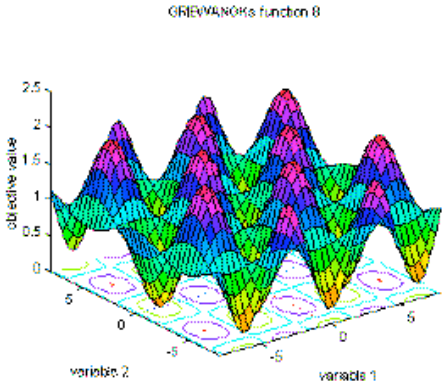

Figure 7: Visualization of Griewank's function for 2 variables

CONTACT INFORMATION

Website: http://www.ago-inc.com

USA
Email: alcpower@gmail.com
Tel: 1 408 543 9650
23252 Orange Ave Unit 2,
Lake Forest, CA-92630

Asia
Email: hillol.sarkar@gmail.com
Tel: 91 983 035 7206

Europe
Alpha Star
Email: roddy@alpha-star.eu
Tel: 44 1264 36 9483,
Mobile: 44 753 158 7023
10 Pitts Lane, Andover, Hampshire,
SP10 2HY, UK.