FUJITSU MICROELECTRONICS
DATA SHEET

DS07-13706-6E

16-bit Proprietary Microcontroller

CMOS

F²MC-16LX MB90550A/550B Series

MB90552A/552B/553A/553B/T552A/T553A
MB90F553A/P553A/V550A

■ DESCRIPTION

The MB90550A/550B series is a line of general-purpose, high-performance, 16-bit microcontrollers designed for applications which require high-speed real-time processing, such as industrial machines, OA equipment, and process control systems.

While inheriting the AT architecture of the F²MC*-8 family, the instruction set for the MB90550A/550B series incorporates additional instructions for high-level languages, supports extended addressing modes, and contains enhanced multiplication and division instructions as well as a substantial collection of improved bit manipulation instructions. In addition, the MB90550A/550B has an on-chip 32-bit accumulator which enables processing of long-word data.

MB90552B and MB90553B are radiation noise decreased type. There are no change in the functional specification.

*: F²MC is the abbreviation of FUJITSU MICROELECTRONICS Flexible Microcontroller.

■ FEATURES

- Minimum instruction execution time: 62.5 ns (at oscillation of 4 MHz, × four times the PLL clock)
- Maximum memory space: 16 Mbytes

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The information for microcontroller supports is shown in the following homepage.
Be sure to refer to the "Check Sheet" for the latest cautions on development.

"Check Sheet" is seen at the following support page

"Check Sheet" lists the minimal requirement items to be checked to prevent problems beforehand in system development.

http://edevice.fujitsu.com/micom/en-support/

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- Instruction set optimized for controller applications
  Supported data types: Bit, byte, word and long word
  Typical addressing mode: 23 types
  Enhanced precision calculation realized by 32-bit accumulator
  Enhanced signed multiplication/division instruction and RETI instruction functions
- Instruction set designed for high level language (C) and multi-task operations
  Adoption of system stack pointer
  Symmetrical instruction set and barrel shift instructions
- Integrated address match detection function (for two address pointers)
- Faster execution speed: 4-byte queue
- Powerful interrupt functions (Eight priority levels programmable)
  External interrupt inputs: 8 channels
- Data transfer functions (Intelligent I/O service): Up to 16 channels
  DTP request inputs: 8 channels
- Embedded ROM size (EPROM, Flash: 128 Kbytes)
  Mask ROM: 64 Kbytes/128 Kbytes
- Embedded RAM size (EPROM, Flash: 4 Kbytes)
  Mask ROM: 2 Kbytes/4 Kbytes
- General-purpose ports: Up to 83 channels
  (Input pull-up resistor settable for: 16 channels; Open drain settable for: 8 channels; I/O open drains: 6 channels)
- A/D converter (RC successive approximation type): 8 channels
  (Resolution: 8 or 10 bits selectable; Conversion time of 26.3 μs minimum)
- UART: 1 channel
- Extended I/O serial interface: 2 channels
- I^2C interface: 2 channels
  (Two channels, including one switchable between terminal input and output)
- 16-bit reload timer: 2 channels
- 8/16-bit PPG timer: 3 channels
  (8 bits × 2 channels; 16 bits x 1 channel: Mode switching function provided)
- 16-bit I/O timer
  (Input capture × 4 channels, output compare × 4 channels, free run timer ×1 channel)
- Clock monitor function integrated (Delivering the oscillation clock divided by 21 to 28)
- Timebase timer/watchdog timer: 18 bits
- Low power consumption modes (sleep, stop, hardware standby, and CPU intermittent operation modes)
- Package: QFP-100, LQFP-100
- CMOS technology

■ PRODUCT LINEUP

Item \ Part number		MB90552A MB90552B	MB90553A MB90553B	MB90F553A	MB90P553A	MB90T552A	MB90T553A	MB90V550A
Classification		Mask ROM products		Flash ROM products	OTP	External ROM products		Evaluation product
		Mass Product						
ROM size		64 Kbytes	128 Kbytes			None		None
RAM size		2 Kbytes	4 Kbytes			2 Kbytes	4 Kbytes	6 Kbytes
CPU functions		The number of instructions: 340 Instruction bit length: 8 bits, 16 bits Instruction length: 1 byte to 7 bytes Data bit length: 1 bit, 8 bits, 16 bits Minimum execution time: 62.5 ns (at machine clock of 16 MHz) Interrupt processing time: 1.5 µs (at machine clock of 16 MHz, minimum value)						
Ports		General-purpose I/O ports (CMOS output): 53 General-purpose I/O ports (with pull-up resistor): 16 General-purpose I/O ports (N-channel open-drain output): 6 General-purpose I/O ports (N-channel open-drain function selectable): 8 Total: 83						
UART (SCI)		Clock synchronized transmission (62.5 Kbps to 2 Mbps) Clock asynchronized transmission (62500 bps to 9615 bps) Transmission can be performed by bi-directional serial transmission or by master/slave connection.						
8/10-bit A/D converter		Conversion precision: 8/10-bit can be selectively used. Number of inputs: 8 One-shot conversion mode (converts selected channel only once) Scan conversion mode (converts two or more successive channels and can program up to 8 channels.) Continuous conversion mode (converts selected channel continuously) Stop conversion mode (converts selected channel and stop operation repeatedly)						
8/16-bit PPG timer		Number of channels: 3 (8-bit × 6 channels) PPG operation of 8-bit or 16-bit A pulse wave of given intervals and given duty ratios can be output. Pulse interval: 62.5 ns to 1 ms (at oscillation of 4 MHz, machine clock of 16 MHz)						
16-bit I/O timer	16-bit free run timer	Number of channels: 1 Overflow interrupts						
	Output compare (OCU)	Number of channels: 4 Pin input factor: A match signal of compare register						
	Input capture (ICU)	Number of channels: 4 Rewriting a register value upon a pin input (rising, falling or both edges)						

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Part number / Item	MB90552A MB90552B	MB90553A MB90553B	MB90F553A	MB90P553A	MB90T552A	MB90T553A	MB90V550A
DTP/external interrupt circuit	Number of inputs: 8 Started by a rising edge, a falling edge, an “H” level input, or an “L” level input. External interrupt circuit or extended intelligent I/O service (EI^{2}OS) can be used.						
Extended I/O serial interface	Clock synchronized transmission (3125 bps to 1 Mbps) LSB first/MSB first						
I^{2}C interface	Serial I/O port for supporting Inter IC BUS						
Timebase timer	18-bit counter Interrupt interval: 1.024 ms, 4.096 ms, 16.384 ms, 131.072 ms (at oscillation of 4 MHz)						
Watchdog timer	Reset generation interval: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (at oscillation of 4 MHz, minimum value)						
Process	CMOS						
Power supply voltage for operation*	4.5 V to 5.5 V						

*:Varies with conditions such as the operating frequency. (See section “■ ELECTRICAL CHARACTERISTICS”)
Assurance for the MB90V550A is given only for operation with a tool at a power voltage of 4.5 V to 5.5 V, an operating temperature of 0°C to +25°C, and an operating frequency of 1 MHz to 16 MHz.

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB90552A MB90552B	MB90553A MB90553B	MB90F553A	MB90P553A
FPT-100P-M20	○	○	○	×
FPT-100P-M06	○	○	○	○

○ : Available × : Not available

Note:For more information about each package, see section “■ PACKAGE DIMENSIONS”

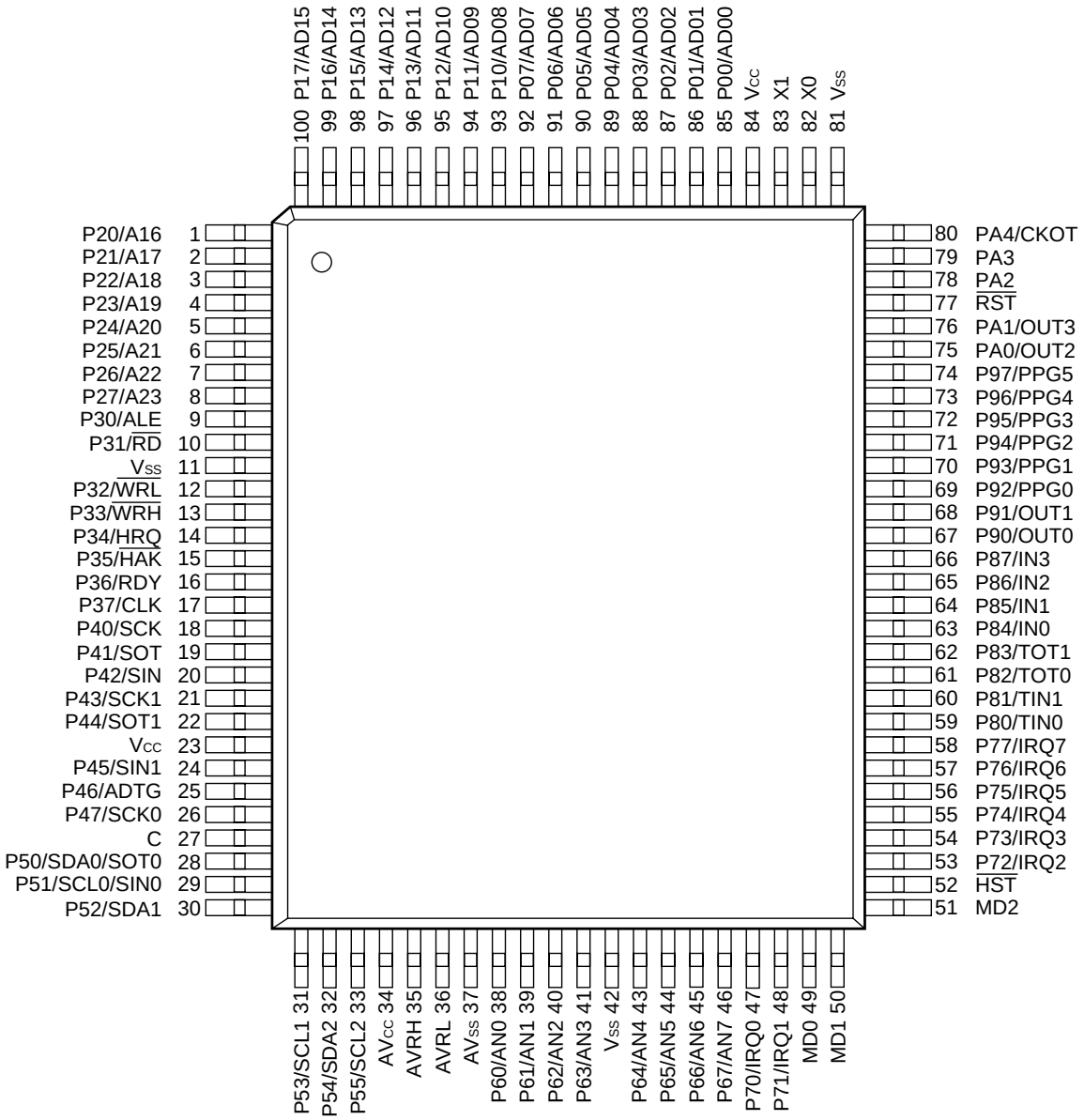
■ DIFFERENCES AMONG PRODUCTS

Memory Size

In evaluation with an evaluation product, note the difference between the evaluation product and the product actually used. The following items must be taken into consideration.

- The MB90V550A does not have an internal ROM. However, operations equivalent to those performed by a chip with an internal ROM can be evaluated by using a dedicated development tool, enabling selection of ROM size by setting the development tool.
- In the MB90V550A, images from FF4000$_H$ to FFFFFF$_H$ are mapped to bank 00, and FE0000$_H$ to FF3FFF$_H$ are mapped to bank FE and FF only. (This setting can be changed by configuring the development tool.)
- In the MB90F553A/553A/553B/552A/552B, images from FF4000$_H$ to FFFFFF$_H$ are mapped to bank 00, and FF0000$_H$ to FF3FFF$_H$ to bank FF only.

■ PIN ASSIGNMENTS



(FPT-100P-M06)

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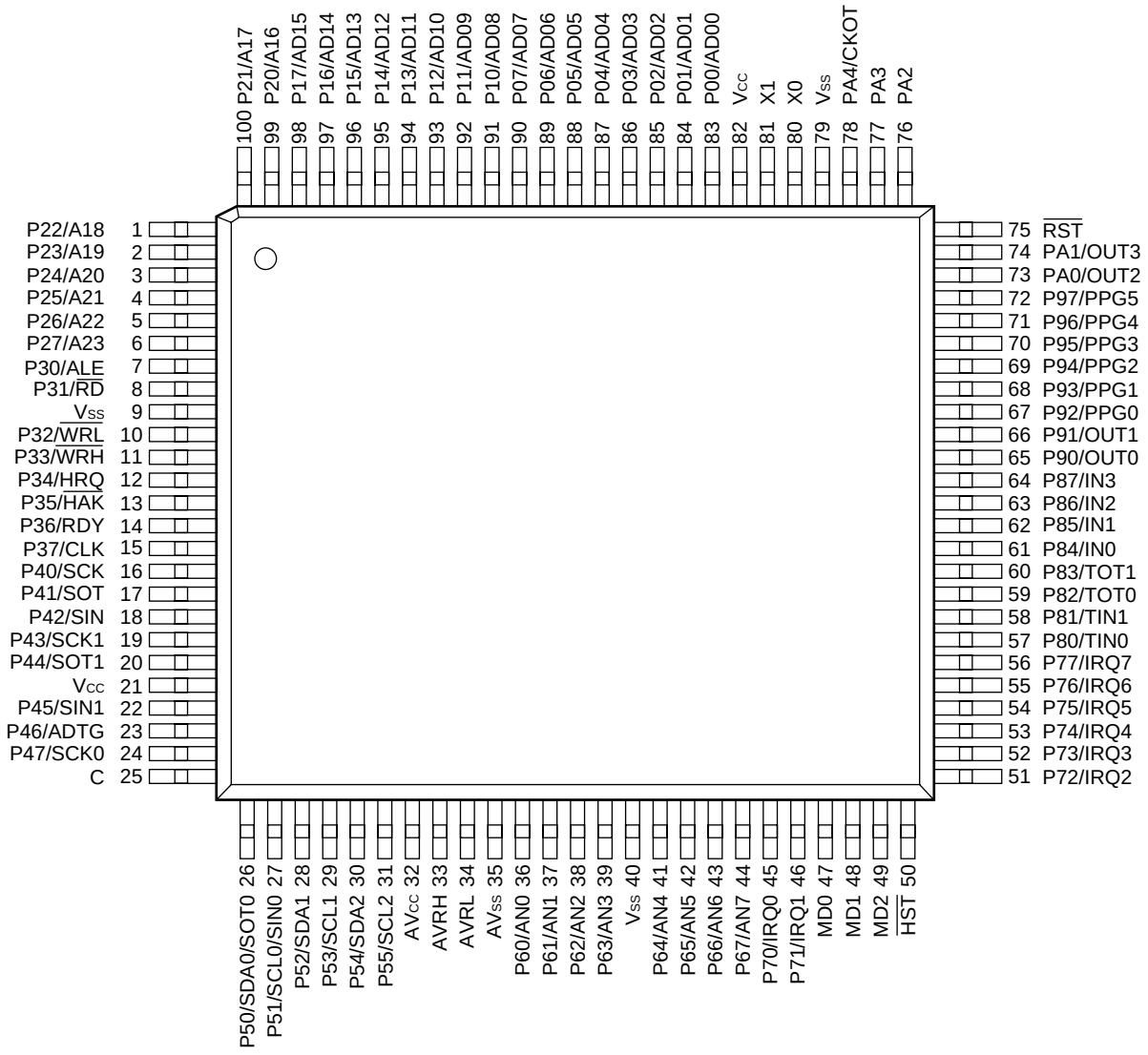
(Top view)



(FPT-100P-M20)

■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Function
QFP	LQFP			
82	80	X0	A	Oscillation pin
83	81	X1	A	Oscillation pin
77	75	$\overline{RST}$	B	Reset input pin
52	50	$\overline{HST}$	C	Hardware standby input pin
85 to 92	83 to 90	P00 to P07	D (CMOS)	General-purpose I/O ports. A pull-up resistor can be added (RD07 to RD00 = 1) by using the pull-up resistor setting register (RDR0). D07 to D00 = 1: Disabled when the port is set for output.
		AD00 to AD07		Serve as lower data I/O/lower address output (AD00 to AD07) pins in the external bus mode.
93 to 100	91 to 98	P10 to P17	D (CMOS)	General-purpose I/O ports. A pull-up resistor can be added (RD17 to RD10 = 1) by using the pull-up resistor setting register (RDR1). D17 to D10 = 1: Disabled when the port is set for output.
		AD08 to AD15		Serve as upper data I/O/middle address output (AD08 to AD15) pins in the 16-bit bus-width, external bus mode.
1 to 8	99,100, 1 to 6	P20 to P27	E (CMOS)	General-purpose I/O ports. This function is enabled either in single-chip mode or with the external address output control register set to “Port”.
		A16 to A23		External address bus A16 to A23 output pins. This function is enabled in an external-bus enabled mode with the external address output register set to “Address”.
9	7	P30	E (CMOS)	General-purpose I/O port. This function is enabled in single-chip mode.
		ALE		Address latch enable output pin. This function is enabled in an external-bus enabled mode.
10	8	P31	E (CMOS)	General-purpose I/O port. This function is enabled in single-chip mode.
		$\overline{RD}$		Read strobe output pin for the data bus. This function is enabled in an external-bus enabled mode.
12	10	P32	E (CMOS)	General-purpose I/O port. This function is enabled in single-chip mode.
		$\overline{WRL}$		Write strobe output pin for the lower eight bits of the data bus. This function is enabled in an external-bus enabled mode.
13	11	P33	E (CMOS)	General-purpose I/O port. This function is enabled in single-chip mode.
		$\overline{WRH}$		Write strobe output pin for the upper eight bits of the data bus. This function is enabled in an external-bus enabled mode.

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Pin no.		Pin name	Circuit type	Function
QFP	LQFP			
14	12	P34	E (CMOS)	General-purpose I/O port. This function is enabled in single-chip mode
		HRQ		Hold request input pin. This function is enabled in an external-bus enabled mode.
15	13	P35	E (CMOS)	General-purpose I/O port. This function is enabled in single-chip mode.
		$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled in an external-bus enabled mode.
16	14	P36	E (CMOS)	General-purpose I/O port. This function is enabled in single-chip mode.
		RDY		Ready signal input pin. This function is enabled in an external-bus enabled mode.
17	15	P37	E (CMOS)	General-purpose I/O port. This function is enabled in single-chip mode.
		CLK		CLK output pin. This function is enabled in an external-bus enabled mode.
18	16	P40	F (CMOS/H)	General-purpose I/O port. Serves as an open-drain output port (OD40 = 1) depending on the setting of the open-drain control setting register (ODR4). (D40 = 0: Disabled when the port is set for input.)
		SCK		UART serial clock I/O pin. This function is enabled with the UART clock output enabled.
19	17	P41	F (CMOS/H)	General-purpose I/O port. Serves as an open-drain output port (OD41 = 1) depending on the setting of the open-drain control setting register (ODR4). (D41 = 0: Disabled when the port is set for input.)
		SOT		UART serial data output pin. This function is enabled with the UART serial data output enabled.
20	18	P42	F (CMOS/H)	General-purpose I/O port. Serves as an open-drain output port (OD42 = 1) depending on the setting of the open-drain control setting register (ODR4). (D42 = 0: Disabled when the port is set for input.)
		SIN		UART serial data input pin. Since this input is used as required while the UART is operating for input, the output by any other function must be off unless used intentionally.
21	19	P43	F (CMOS/H)	General-purpose I/O port. Serves as an open-drain output port (OD43 = 1) depending on the setting of the open-drain control setting register (ODR4). (D43 = 0: Disabled when the port is set for input.)
		SCK1		Extended I/O serial clock I/O pin. This function is enabled with the extended I/O serial clock output enabled.

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Pin no.		Pin name	Circuit type	Function
QFP	LQFP			
22	20	P44	F (CMOS/H)	General-purpose I/O port. Serves as an open-drain output port (OD44 = 1) depending on the setting of the open-drain control setting register (ODR4). (D44 = 0: Disabled when the port is set for input.)
		SOT1		Extended I/O serial data output pin. This function is enabled with the extended I/O serial data output enabled.
24	22	P45	F (CMOS/H)	General-purpose I/O port. Serves as an open-drain output port (OD45 = 1) depending on the setting of the open-drain control setting register (ODR4). (D45 = 0: Disabled when the port is set for input.)
		SIN1		Extended I/O serial data input pin. Since this input is used as required while the extended I/O serial interface is operating for input, the output by any other function must be off unless used intentionally.
25	23	P46	F (CMOS/H)	General-purpose I/O port. Serves as an open-drain output port (OD46 = 1) depending on the setting of the open-drain control setting register (ODR4). (D46 = 0: Disabled when the port is set for input.)
		ADTG		A/D converter external trigger input pin. Since this input is used as required while the A/D converter is operating for input, the output by any other function must be off unless used intentionally.
26	24	P47	F (CMOS/H)	General-purpose I/O port. Serves as an open-drain output port (OD47 = 1) depending on the setting of the open-drain control setting register (ODR4). D47 = 0: Disabled when the port is set for input.
		SCK0		Extended I/O serial clock I/O pin. This function is enabled with the extended I/O serial clock output enabled.
27	25	C	—	Capacitance pin for regulating the power supply. Connect an external ceramic capacitor of about 0.1 μF.
28	26	P50	G (NchOD/H)	N-channel open-drain I/O port.
		SDA0		I^2C interface data I/O pin. This function is enabled with the I^2C interface enabled for operation. While the I^2C interface is operating, place the port output in the Hi-Z state (PDR = 1).
		SOT0		Extended I/O serial data output pin. This function is enabled with the extended I/O serial data output enabled.

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Pin no.		Pin name	Circuit type	Function
QFP	LQFP			
29	27	P51	G (NchOD/H)	N-channel open-drain I/O port.
		SCL0		I^2C interface clock I/O pin. This function is enabled with the I^2C interface enabled for operation. While the I^2C interface is operating, place the port output in the Hi-Z state (PDR = 1).
		SIN0		Extended I/O serial data input pin. Since this input is used as required while the extended I/O serial interface is operating for input, the output by any other function must be off unless used intentionally.
30,32	28,30	P52,P54	G (NchOD/H)	N-channel open-drain I/O ports.
		SDA1,SDA2		I^2C interface data I/O pins. This function is enabled with the I^2C interface enabled for operation. While the I^2C interface is operating, place the port output in the Hi-Z state (PDR = 1).
31,33	29,31	P53,P55	G (NchOD/H)	N-channel open-drain I/O ports.
		SCL1,SCL2		I^2C interface clock I/O pins. This function is enabled with the I^2C interface enabled for operation. While the I^2C interface is operating, place the port output in the Hi-Z state (PDR = 1).
38 to 41, 43 to 46	36 to 39, 41 to 44	P60 to P67	H (CMOS/H)	General-purpose I/O ports.
		AN0 to AN7		A/D converter analog input pin. This function is enabled with the analog input enabled.
47,48, 53 to 58	45,46, 51 to 56	P70 to P77	I (CMOS/H)	General-purpose I/O ports.
		IRQ0 to IRQ7		External interrupt request input pins. Since this input is used as required while external interrupts remain enabled, the output by any other function must be off unless used intentionally.
59,60	57,58	P80,P81	J (CMOS/H)	General-purpose I/O ports.
		TIN0,TIN1		Reload timer event input pins. Since this input is used as required while the reload timer is operating for input, the output by any other function must be off unless used intentionally.
61,62	59,60	P82,P83	J (CMOS/H)	General-purpose I/O ports.
		TOT0,TOT1		Reload timer output pins.This function is enabled with reload timer output enabled.
63 to 66	61 to 64	P84 to P87	J (CMOS/H)	General-purpose I/O ports.
		IN0 to IN3		Input capture trigger input pins. Since this input is used as required while the input capture unit is operating for input, the output by any other function must be off unless used intentionally.
67,68	65,66	P90,P91	J (CMOS/H)	General-purpose I/O ports.
		OUT0,OUT1		Output compare event output pins.

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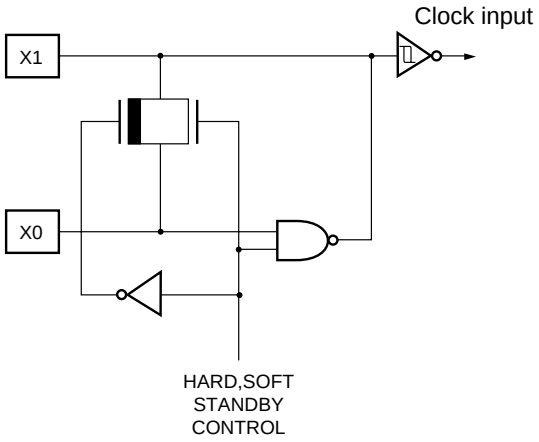
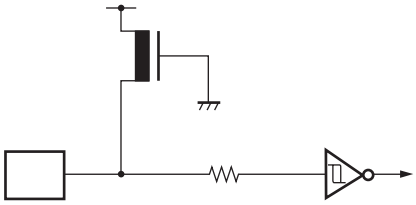
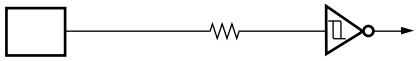
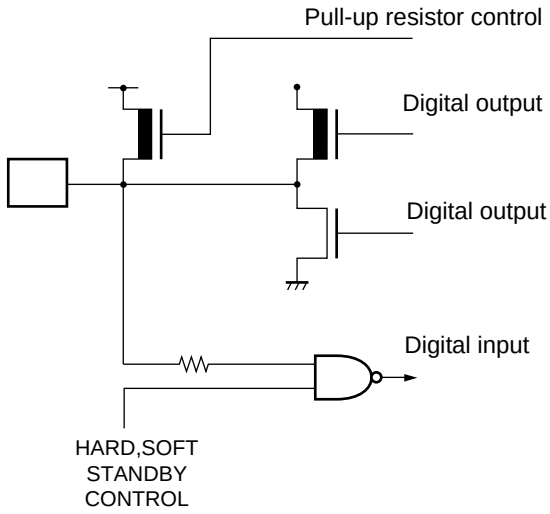
Pin no.		Pin name	Circuit type	Function
QFP	LQFP			
69 to 74	67 to 72	P92 to P97	J (CMOS/H)	General-purpose I/O ports.
		PPG0 to PPG5		PPG output pins. This function is enabled with the PPG output enabled.
75,76	73,74	PA0,PA1	J (CMOS/H)	General-purpose I/O ports.
		OUT2,OUT3		Output compare event output pins.
78,79	76,77	PA2,PA3	J (CMOS/H)	General-purpose I/O ports.
80	78	PA4	J (CMOS/H)	General-purpose I/O port.
		CKOT		Serves as the CKOT output while the CKOT is operating.
34	32	AV_{CC}	—	A/D converter power-supply pin.
35	33	AVRH	—	A/D converter external reference voltage source pin.
36	34	AVRL	—	A/D converter external reference voltage source pin.
37	35	AV_{SS}	—	A/D converter power-supply pin.
49,50	47,48	MD0,MD1	C	Operation mode setting input pins. Connect these pins directly to Vcc or Vss.
51	49	MD2	K	Operation mode setting input pin. Connect this pin directly to Vcc or Vss. (MB90552A/552B/553A/553B/V550A)
			C	Operation mode setting input pin. Connect this pin directly to Vcc or Vss. (MB90P553A/F553A)
23,84	21,82	V_{CC}	—	Power (5 V) input pins.
11,42, 81	9,40, 79	V_{SS}	—	Power (0 V) input pins.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• 3 MHz to 32 MHz • Oscillator recovery resistor approx. 1MΩ
B		• CMOS level hysteresis input • Pull-up resistor provided Resistor: About 50 kΩ
C		• CMOS level hysteresis input
D		• CMOS level output • CMOS level input • Standby control provided • Input pull-up resistor control provided Resistor: About 50 kΩ

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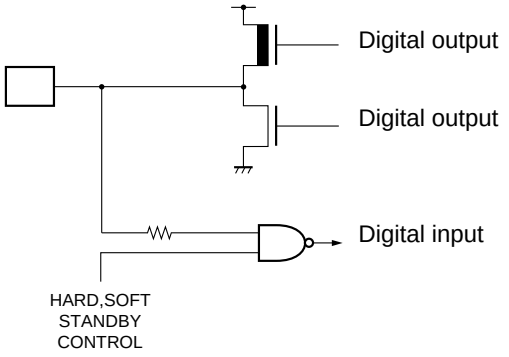
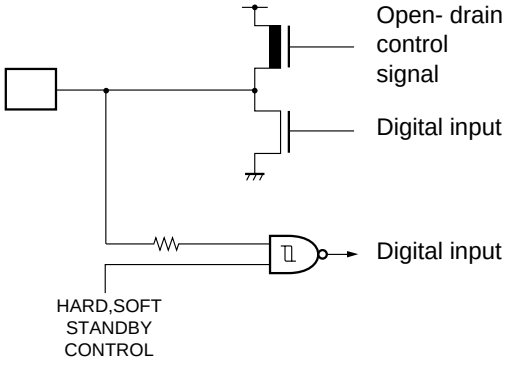
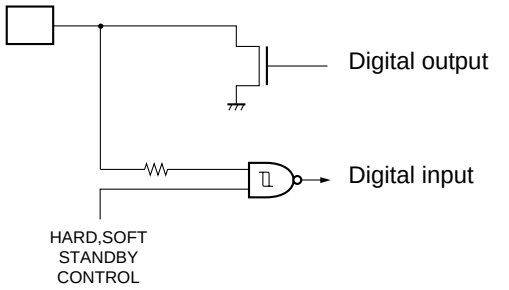
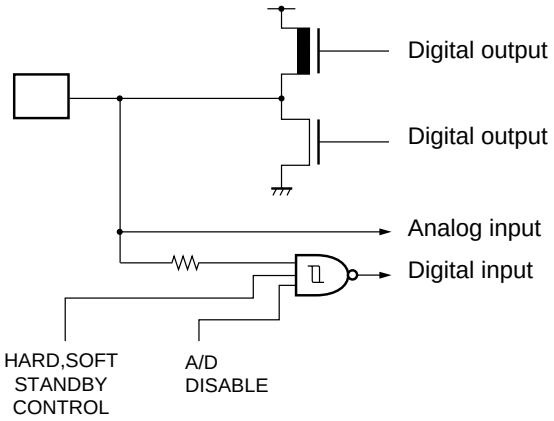
Type	Circuit	Remarks
E		• CMOS level output • CMOS level input • Standby control provided
F		• CMOS level output • CMOS level hysteresis input • Open-drain control provided
G		• N-channel open-drain output • CMOS level hysteresis input • Standby control provided Note: Unlike normal CMOS I/O pins, this pin is not provided with any P-channel transistor. Therefore the pin does not allow a current to flow to the Vcc side even when applied with a voltage from an external device with the IC's power supply left off.
H		• CMOS level output • CMOS level hysteresis input • Standby control provided • Analog input

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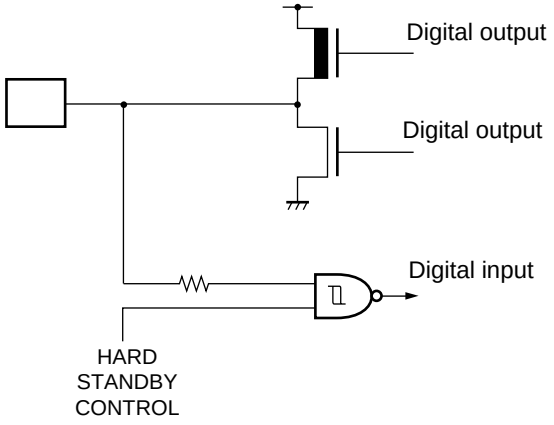
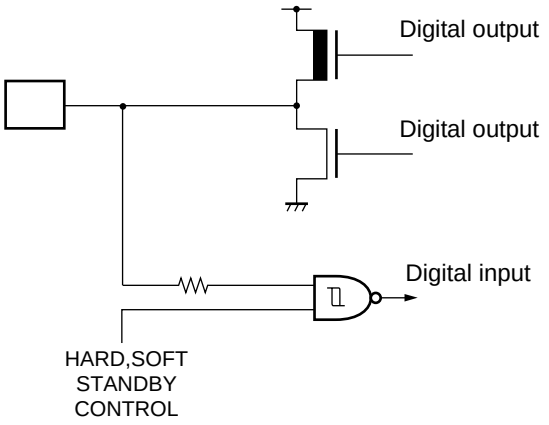
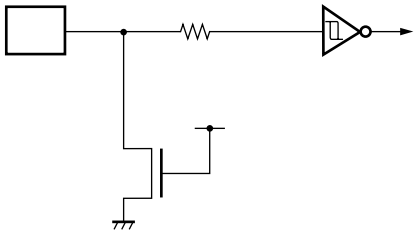
Type	Circuit	Remarks
I		• CMOS level output • CMOS level hysteresis input • Standby control provided
J		• CMOS level output • CMOS level hysteresis input • Standby control provided
K		• CMOS level hysteresis input • Pull-up resistor provided Resistor: About 50 kΩ

■ HANDLING DEVICES

1. Preventing Latchup

CMOS ICs may cause latchup in the following situations:

- When a voltage higher than Vcc or lower than Vss is applied to input or output pins.
- When a voltage exceeding the rating is applied between Vcc and Vss.
- When AVcc power is supplied prior to the Vcc voltage.

If latchup occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Use meticulous care not to let it occur.

For the same reason, also be careful not to let the analog power-supply voltage exceed the digital power-supply voltage.

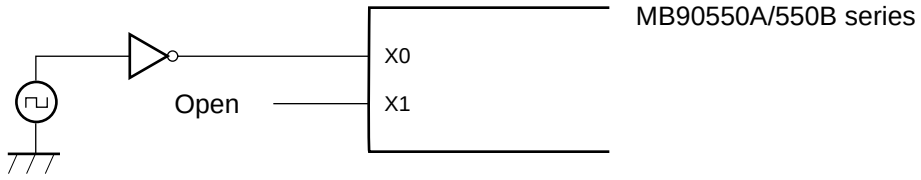
2. Handling unused input pins

Leaving unused input pins open may cause a malfunction or latch-up which leads to fatal damage to the device. Therefore they must be pulled up or pulled down through at least 2 kΩ resistance. Also, unused input/output pins should be left open in output state or handled in the same way as unused input pins.

3. Notes on Using External Clock

In using the external clock, drive X0 pin only and leave X1 pin open.

- **Using external clock**



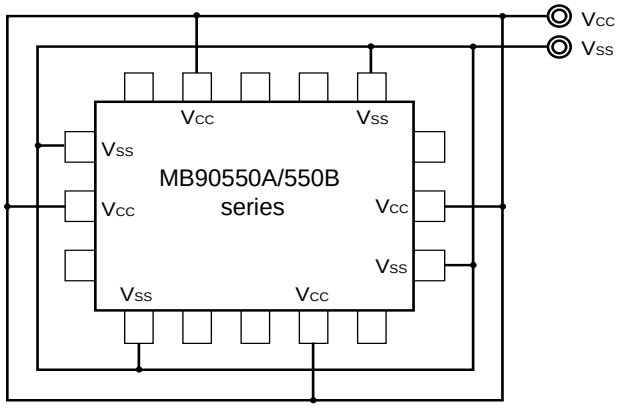
4. Power Supply Pins (V_{CC}/V_{SS})

In products with multiple V_{CC} or V_{SS} pins, the pins of a same potential are internally connected in the device to avoid abnormal operations including latch-up. However, the pins should be connected to external power and ground lines to lower the electro-magnetic emission level and abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.

Make sure to connect V_{CC} and V_{SS} pins via lowest impedance to power lines.

It is recommended that a bypass capacitor of around 0.1 µF be placed between the V_{CC} and V_{SS} pins near the device.

- **Using power supply pins**



5. Crystal Oscillator Circuit

Noise around X0 or X1 pins may cause abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure that lines of oscillation circuit do not cross the lines of other circuits.

A printed circuit board artwork surrounding the X0 and X1 pins with grand area for stabilizing the operation is highly recommended.

6. Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (AN0 to AN7) after turning-on the digital power supply (V_{CC}).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that AVRH does not exceed AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

7. Connection of Unused Pins of A/D Converter

Connect unused pin of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = AVRL = V_{SS}$.

8. N.C. Pin

The N.C. (internally connected) pin must be opened for use.

9. Notes on Energization

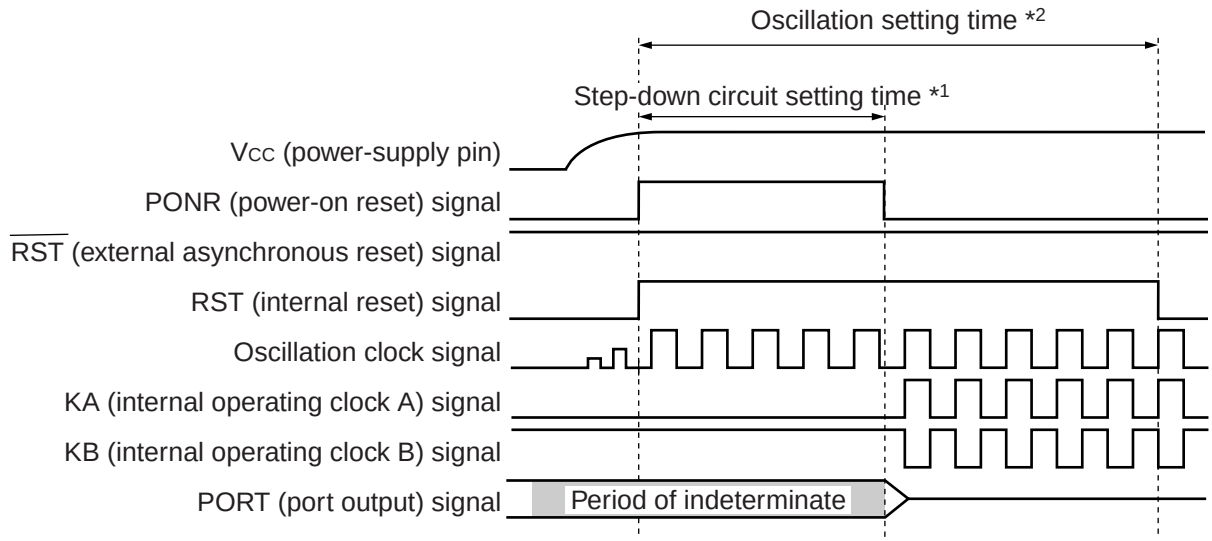
To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 µs or more.

10. Indeterminate outputs from ports 0 and 1

The outputs from ports 0 and 1 become indeterminate during oscillation setting time of step-down circuit (during a power-on reset) after the power is turned on. (MB90552A, MB90552B, MB90553A, MB90553B, MB90F553A, MB90V550A)

The series without built-in step-down circuit has no oscillation setting time of step-down circuit, so outputs should not become indeterminate. (MB90P553A)

Timing chart of indeterminate outputs from ports 0 and 1



*1: Step-down circuit setting time 2^{17}/oscillation clock frequency (oscillation clock frequency of 16 MHz: 8.19 ms)

*2: Oscillation setting time 2^{18}/oscillation clock frequency (oscillation clock frequency of 16 MHz: 16.38 ms)

11. Initialization

In the device, there are internal registers initialized only by a power-on reset. To initialize these registers, turn on the power again.

12. Return from standby state

If the power-supply voltage goes below the standby RAM holding voltage in the standby state, the device may fail to return from the standby state. In this case, reset the device via the external reset pin to return to the normal state.

13. Precautions for Use of “DIV A, Ri,” and “DIVW A, Ri” Instructions

The signed multiplication-division instructions “DIV A, Ri,” and “DIVW A, RWi” should be used when the corresponding bank registers (DTB, ADB, USB, SSB) are set to value “00_H.” If the corresponding bank registers (DTB, ADB, USB, SSB) are set to a value other than “00_H,” the remainder obtained after the execution of the instruction will not be placed in the instruction operand register.

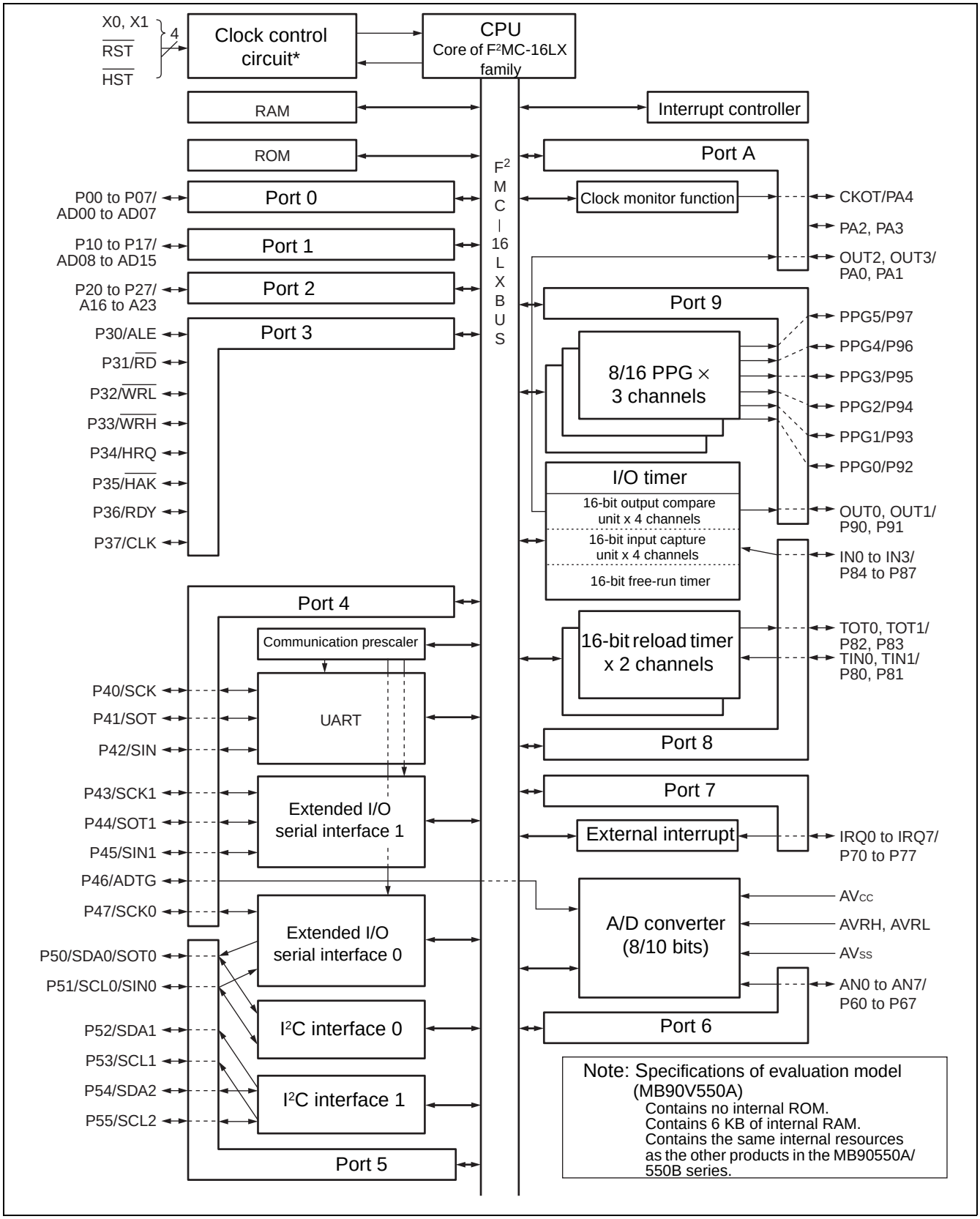
14. Using of REALOS

The extended intelligent I/O service (EI^{2}OS) cannot be used when using REALOS.

15. Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected in the microcontroller, it may attempt to continue the operation using the free-running frequency of the self oscillation circuit in the PLL circuitry even if the oscillator is out of place or the clock input is stopped.
Performance of this operation, however, cannot be guaranteed.

■ BLOCK DIAGRAM



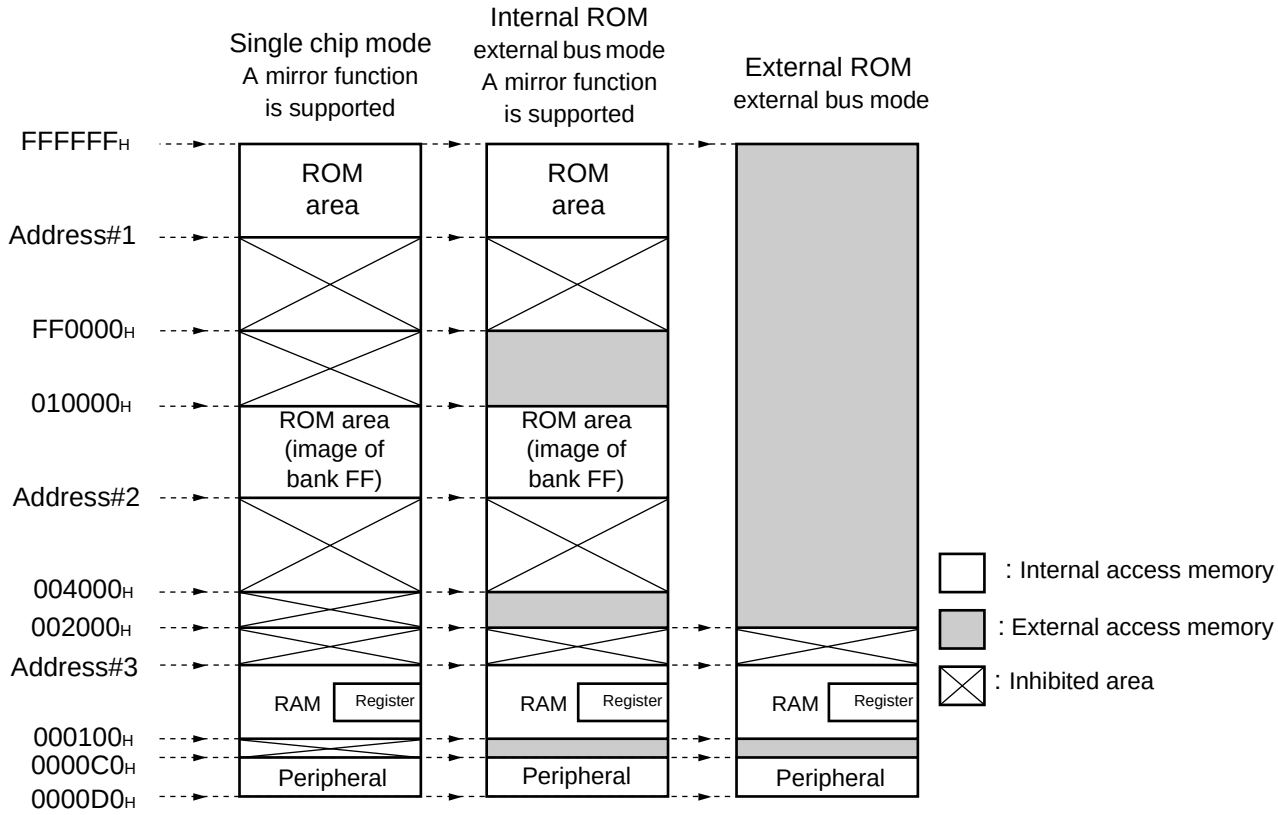
*: The clock control circuit contains a watchdog timer, time-base timer, and a low power consumption control circuit.

Note : P00 to P07 (8 pins): Input pull-up resistor setting register provided
P10 to P17 (8 pins): Input pull-up resistor setting register provided
P40 to P47 (8 pins): Open-drain control setting register provided
P50 to P55 (6 pins): N-channel open drain
Ports 0, 1, 2, 3, 4, 6, 7, 8, 9, and A are CMOS level input/output ports.

■ MEMORY MAP

The ROM data of bank FF is reflected in the upper address of bank 00, realizing effective use of the C compiler small model. The lower 16-bit of bank FF and the lower 16-bit of bank 00 are assigned to the same address, enabling reference of the table on the ROM without stating “far”.

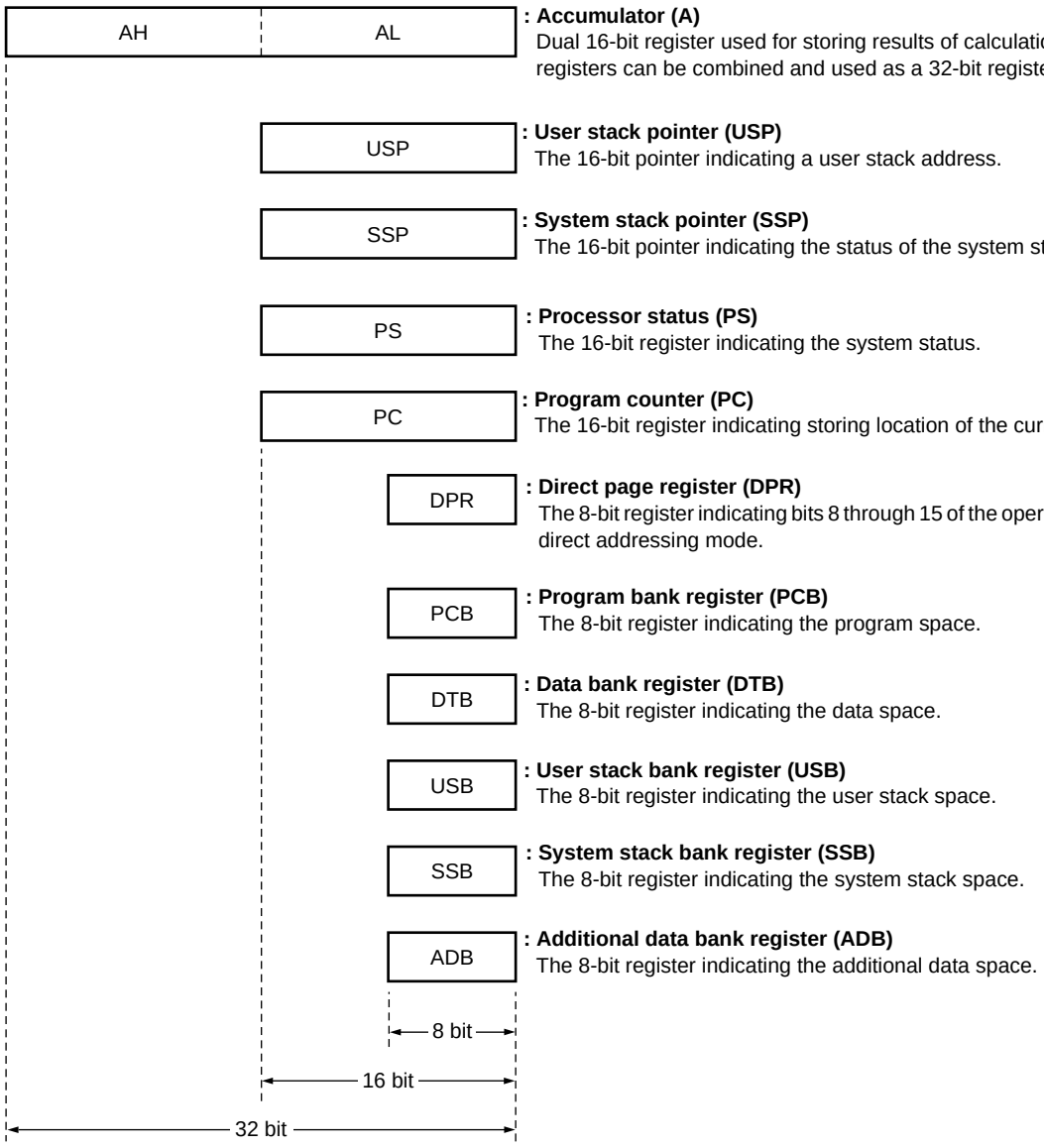
For example, if an attempt has been made to access 00C000H, the contents of the ROM at FFC000H are accessed. Since the ROM area of the FF bank exceeds 48 Kbytes, the whole area cannot be reflected in the image for the 00 bank. The ROM data at FF4000H to FFFFFFH looks, therefore, as if it were the image for 004000H to 00FFFFH. Thus, it is recommended that the ROM data table be stored in the area of FF4000H to FFFFFFH.



Parts No.	Address#1	Address#2	Address#3
MB90552A/552B	FF0000H	004000H	000900H
MB90553A/553B	FE0000H	004000H	001100H
MB90F553A	FE0000H	004000H	001100H
MB90P553A	FE0000H	004000H	001100H
MB90V550A	(FE0000H)	004000H	001900H

■ F²MC-16LX CPU PROGRAMMING MODEL

- Dedicated registers



■ I/O MAP

Address	Register name	Abbreviated register name	Read/write	Resource name	Initial value
00H	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXX
01H	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXX
02H	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXX
03H	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXX
04H	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXX
05H	Port 5 data register	PDR5	R/W	Port 5	_ _ 1 1 1 1 1 1
06H	Port 6 data register	PDR6	R/W	Port 6	XXXXXXXX
07H	Port 7 data register	PDR7	R/W	Port 7	XXXXXXXX
08H	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXX
09H	Port 9 data register	PDR9	R/W	Port 9	XXXXXXXX
0AH	Port A data register	PDRA	R/W	Port A	_ _ _XXXXX
0BH to 0FH	(Disabled)				
10H	Port 0 direction register	DDR0	R/W	Port 0	0 0 0 0 0 0 0 0
11H	Port 1 direction register	DDR1	R/W	Port 1	0 0 0 0 0 0 0 0
12H	Port 2 direction register	DDR2	R/W	Port 2	0 0 0 0 0 0 0 0
13H	Port 3 direction register	DDR3	R/W	Port 3	0 0 0 0 0 0 0 0
14H	Port 4 direction register	DDR4	R/W	Port 4	0 0 0 0 0 0 0 0
15H	(Disabled)				
16H	Port 6 direction register	DDR6	R/W	Port 6	0 0 0 0 0 0 0 0
17H	Port 7 direction register	DDR7	R/W	Port 7	0 0 0 0 0 0 0 0
18H	Port 8 direction register	DDR8	R/W	Port 8	0 0 0 0 0 0 0 0
19H	Port 9 direction register	DDR9	R/W	Port 9	0 0 0 0 0 0 0 0
1AH	Port A direction register	DDRA	R/W	Port A	_ _ _ 0 0 0 0 0
1BH	Port 4 output pin register	ODR4	R/W	Port 4	0 0 0 0 0 0 0 0
1CH	Port 0 resistor setting register	RDR0	R/W	Port 0	0 0 0 0 0 0 0 0
1DH	Port 1 resistor setting register	RDR1	R/W	Port 1	0 0 0 0 0 0 0 0
1EH	(Disabled)				
1FH	Analog input enable register	ADER	R/W	Port 6, A/D converter	1 1 1 1 1 1 1 1
20H	Serial mode register	SMR	R/W	UART	0 0 0 0 0 0 0 0
21H	Serial control register	SCR	R/W		0 0 0 0 0 10 0
22H	Serial input data register / serial output data register	SIDR/SODR	R/W		XXXXXXXX
23H	Serial status register	SSR	R/W		0 0 0 0 1 _ 0 0

(Continued)

Address	Register name	Abbreviated register name	Read/write	Resource name	Initial value
24H	Serial mode control status register 0	SMCS0	R/W	Extended I/O serial interface 0	_ _ _ _ 0 0 0 0
25H	Serial mode control status register 0		R/W!		0 0 0 0 0 0 1 0
26H	Serial data register 0	SDR0	R/W		XXXXXXXX
27H	Clock frequency-divider control register	CDCR	R/W	Communication prescaler	0 _ _ _ 1 1 1 1
28H	Serial mode control status register 1	SMCS1	R/W	Extended I/O serial interface 1	_ _ _ _ 0 0 0 0
29H	Serial mode control status register 1		R/W!		0 0 0 0 0 0 1 0
2AH	Serial data register 1	SDR1	R/W		XXXXXXXX
2BH	(Disabled)				
2CH	I²C bus status register 0	IBSR0	R	I²C interface 0	0 0 0 0 0 0 0 0
2DH	I²C bus control register 0	IBCR0	R/W		0 0 0 0 0 0 0 0
2EH	I²C bus clock select register 0	ICCR0	R/W		_ _ 0XXXXX
2FH	I²C bus address register 0	IADR0	R/W		_ XXXXXXX
30H	I²C bus data register 0	IDAR0	R/W		XXXXXXXX
31H	(Disabled)				
32H	I²C bus status register 1	IBSR1	R	I²C interface 1	0 0 0 0 0 0 0 0
33H	I²C bus control register 1	IBCR1	R/W		0 0 0 0 0 0 0 0
34H	I²C bus clock select register 1	ICCR1	R/W		_ _ 0XXXXX
35H	I²C bus address register 1	IADR1	R/W		_ XXXXXXX
36H	I²C bus data register 1	IDAR1	R/W		XXXXXXXX
37H	I²C bus port select register	ISEL	R/W		_ _ _ _ _ _ _ 0
38H	Interrupt/DTP enable register	ENIR	R/W	DTP/external interrupt	0 0 0 0 0 0 0 0
39H	Interrupt/DTP factor register	EIRR	R/W		XXXXXXXX
3AH	Request level setting register	ELVR	R/W		0 0 0 0 0 0 0 0
3BH					0 0 0 0 0 0 0 0
3CH	Control status register	ADCS0	R/W	A/D convertor	0 0 0 0 0 0 0 0
3DH		ADCS1	R/W!		0 0 0 0 0 0 0 0
3EH	Data register	ADCR0	R		XXXXXXXX
3FH		ADCR1	R/W!		0 0 0 0 1 _ XX

(Continued)

Address	Register name	Abbreviated register name	Read/write	Resource name	Initial value
40H	Reload register L (ch.0)	PRLL0	R/W	8/16-bit PPG0/1	XXXXXXXX
41H	Reload register H (ch.0)	PRLH0	R/W		XXXXXXXX
42H	Reload register L (ch.1)	PRLL1	R/W		XXXXXXXX
43H	Reload register H (ch.1)	PRLH1	R/W		XXXXXXXX
44H	PPG0 operating mode control register	PPGC0	R/W		0_000__1
45H	PPG1 operating mode control register	PPGC1	R/W		0_000001
46H	PPG0 and 1 output control register	PPGE1	R/W		00000000
47H	(Disabled)				
48H	Reload register L (ch.2)	PRLL2	R/W	8/16-bit PPG2/3	XXXXXXXX
49H	Reload register H (ch.2)	PRLH2	R/W		XXXXXXXX
4AH	Reload register L (ch.3)	PRLL3	R/W		XXXXXXXX
4BH	Reload register H (ch.3)	PRLH3	R/W		XXXXXXXX
4CH	PPG2 operating mode control register	PPGC2	R/W		0_000__1
4DH	PPG3 operating mode control register	PPGC3	R/W		0_000001
4EH	PPG2 and 3 output control register	PPGE2	R/W		00000000
4FH	(Disabled)				
50H	Reload register L (ch.4)	PRLL4	R/W	8/16-bit PPG4/5	XXXXXXXX
51H	Reload register H (ch.4)	PRLH4	R/W		XXXXXXXX
52H	Reload register L (ch.5)	PRLL5	R/W		XXXXXXXX
53H	Reload register H (ch.5)	PRLH5	R/W		XXXXXXXX
54H	PPG4 operating mode control register	PPGC4	R/W		0_000__1
55H	PPG5 operating mode control register	PPGC5	R/W		0_000001
56H	PPG4 and 5 output control register	PPGE3	R/W		00000000
57H	(Disabled)				
58H	Clock output enable register	CLKR	R/W	Clock monitor function	____0000
59H	(Disabled)				

(Continued)

Address	Register name	Abbreviated register name	Read/write	Resource name	Initial value
5A$_H$	Control status register 0	TMCSR0	R/W	16-bit reload timer 0	0 0 0 0 0 0 0 0
5B$_H$					_ _ _ _ 0 0 0 0
5C$_H$	16 bit timer register 0/ 16 bit reload register 0	TMR0/ TMRLR0	R/W		XXXXXXXX
5D$_H$					XXXXXXXX
5E$_H$	Control status register 1	TMCSR1	R/W	16-bit reload timer 1	0 0 0 0 0 0 0 0
5F$_H$					_ _ _ _ 0 0 0 0
60$_H$	16 bit timer register 1/ 16 bit reload register 1	TMR1/ TMRLR1	R/W		XXXXXXXX
61$_H$					XXXXXXXX
62$_H$	Input capture register, channel-0 lower bits	IPCP0	R	16-bit I/O timer Input capture (ch.0 to ch.3)	XXXXXXXX
63$_H$	Input capture register, channel-0 upper bits				XXXXXXXX
64$_H$	Input capture register, channel-1 lower bits	IPCP1	R		XXXXXXXX
65$_H$	Input capture register, channel-1 upper bits				XXXXXXXX
66$_H$	Input capture register, channel-2 lower bits	IPCP2	R		XXXXXXXX
67$_H$	Input capture register, channel-2 upper bits				XXXXXXXX
68$_H$	Input capture register, channel-3 lower bits	IPCP3	R		XXXXXXXX
69$_H$	Input capture register, channel-3 upper bits				XXXXXXXX
6A$_H$	Input capture control status register	ICS01	R/W		0 0 0 0 0 0 0 0
6B$_H$	Input capture control status register	ICS23	R/W		0 0 0 0 0 0 0 0
6C$_H$	Timer data register, lower bits	TCDT	R/W	16-bit I/O timer free run timer	0 0 0 0 0 0 0 0
6D$_H$	Timer data register, upper bits		R/W		0 0 0 0 0 0 0 0
6E$_H$	Timer control status register	TCCS	R/W		0 0 0 0 0 0 0 0
6F$_H$	ROM mirroring function selection register	ROMM	W	ROM mirroring function	_ _ _ _ _ _ _ 1

(Continued)

Address	Register name	Abbreviated register name	Read/write	Resource name	Initial value
70H	Compare register, channel-0 lower bits	OCCP0	R/W	16-bit I/O timer output compare (ch.0 to ch.3)	XXXXXXXX
71H	Compare register, channel-0 upper bits				XXXXXXXX
72H	Compare register, channel-1 lower bits	OCCP1	R/W		XXXXXXXX
73H	Compare register, channel-1 upper bits				XXXXXXXX
74H	Compare register, channel-2 lower bits	OCCP2	R/W		XXXXXXXX
75H	Compare register, channel-2 upper bits				XXXXXXXX
76H	Compare register, channel-3 lower bits	OCCP3	R/W		XXXXXXXX
77H	Compare register, channel-3 upper bits				XXXXXXXX
78H	Compare control status register, channel-0	OCS0	R/W		0000__00
79H	Compare control status register, channel-1	OCS1	R/W		___00000
7AH	Compare control status register, channel-2	OCS2	R/W		0000__00
7BH	Compare control status register, channel-3	OCS3	R/W		___00000
7CH to 9DH	(Disabled)				
9EH	Program address detection control register	PACSR	R/W	Address match detection function	00000000
9FH	Delayed interrupt factor generation/cancellation register	DIRR	R/W	Delayed interrupt	_______0
A0H	Low-power consumption mode control register	LPMCR	R/W!	Low power consumption control circuit	00011000
A1H	Clock select register	CKSCR	R/W!		11111100
A2H to A4H	(Disabled)				
A5H	Automatic ready function select register	ARSR	W	External bus pin control circuit	0011__00
A6H	External address output control register	HACR	W		00000000
A7H	Bus control signal select register	ECSR	W		0000000_

(Continued)

Address	Register name	Abbreviated register name	Read/write	Resource name	Initial value
A8H	Watchdog timer control register	WDTC	R/W!	Watchdog timer	XXXXX 1 1 1
A9H	Timebase timer control register	TBTC	R/W!	Timebase timer	1 _ _ 0 0 1 0 0
AAH to ADH	(Disabled)				
AEH	Flash memory control status register	FMCS	R/W	Flash memory interface circuit	0 0 0 0 0 _ _ 0
AFH	(Disabled)				
B0H	Interrupt control register 00	ICR00	R/W!	Interrupt controller	0 0 0 0 0 1 1 1
B1H	Interrupt control register 01	ICR01	R/W!		0 0 0 0 0 1 1 1
B2H	Interrupt control register 02	ICR02	R/W!		0 0 0 0 0 1 1 1
B3H	Interrupt control register 03	ICR03	R/W!		0 0 0 0 0 1 1 1
B4H	Interrupt control register 04	ICR04	R/W!		0 0 0 0 0 1 1 1
B5H	Interrupt control register 05	ICR05	R/W!		0 0 0 0 0 1 1 1
B6H	Interrupt control register 06	ICR06	R/W!		0 0 0 0 0 1 1 1
B7H	Interrupt control register 07	ICR07	R/W!		0 0 0 0 0 1 1 1
B8H	Interrupt control register 08	ICR08	R/W!		0 0 0 0 0 1 1 1
B9H	Interrupt control register 09	ICR09	R/W!		0 0 0 0 0 1 1 1
BAH	Interrupt control register 10	ICR10	R/W!		0 0 0 0 0 1 1 1
BBH	Interrupt control register 11	ICR11	R/W!		0 0 0 0 0 1 1 1
BCH	Interrupt control register 12	ICR12	R/W!		0 0 0 0 0 1 1 1
BDH	Interrupt control register 13	ICR13	R/W!		0 0 0 0 0 1 1 1
BEH	Interrupt control register 14	ICR14	R/W!		0 0 0 0 0 1 1 1
BFH	Interrupt control register 15	ICR15	R/W!		0 0 0 0 0 1 1 1
C0H to FFH	(External area)				
100H to #H	(RAM area)				
#H to 1FEFH	(Reserved area)				

(Continued)

(Continued)

Address	Register name	Abbreviated register name	Read/write	Resource name	Initial value
1FF0H	Program address detection register 0	PADR0	R/W	Address match detection function	XXXXXXXX
1FF1H	Program address detection register 1		R/W		XXXXXXXX
1FF2H	Program address detection register 2		R/W		XXXXXXXX
1FF3H	Program address detection register 3	PADR1	R/W		XXXXXXXX
1FF4H	Program address detection register 4		R/W		XXXXXXXX
1FF5H	Program address detection register 5		R/W		XXXXXXXX
1FF6H to 1FFFH	(Reserved area)				

- Initial value representations
  0: Initial value of 0
  1: Initial value of 1
  X: Initial value undefined
  _: Initial value undefined (none)
- Addresses that follow 00FFH are the reserved areas.
- The boundary #H between the RAM and reserved areas is different depending on each product.

Note : For writable bits, the initial value column contains the initial value to which the bit is initialized at a reset. Notice that it is not the value read from the bit.
The LPMCR, CKSCR, and WDTC registers may be initialized or not initialized, depending on the type of the reset. Their initial values in the above list are those to which the registers are initialized.
“R/W!” in the access column indicates that the register contains read-only or write-only bits.
If a read-modify-write instruction (such as a bit setting instruction) is used to access a register marked “R/W!”, or “W” in the access column, the bit focused on by the instruction is set to the desired value but a malfunction occurs if the other bits contain a write-only bit. Do not use such instructions to access those registers.

■ INTERRUPT FACTORS

INTERRUPT VECTORS, INTERRUPT CONTROL REGISTERS

Interrupt source	EI²OS support	Interrupt vectors		Interrupt control registers	
		Number	Address	ICR	Address
Reset	×	# 08	FFFFDC$_H$	—	—
INT9 instruction	×	# 09	FFFFD8$_H$	—	—
Exception	×	# 10	FFFFD4$_H$	—	—
A/D converter	○	# 11	FFFFD0$_H$	ICR00	0000B0$_H$
Timebase timer	×	# 12	FFFFCC$_H$		
DTP0 (external interrupt 0)	○	# 13	FFFFC8$_H$	ICR01	0000B1$_H$
DTP4/5 (external interrupt 4/5)	○	# 14	FFFFC4$_H$		
DTP1 (external interrupt 1)	○	# 15	FFFFC0$_H$	ICR02	0000B2$_H$
8/16-bit PPG timer0 counter borrow	×	# 16	FFFFBC$_H$		
DTP2 (external interrupt 2)	○	# 17	FFFFB8$_H$	ICR03	0000B3$_H$
8/16-bit PPG timer 1 counter borrow	×	# 18	FFFFB4$_H$		
DTP3 (external interrupt 3)	○	# 19	FFFFB0$_H$	ICR04	0000B4$_H$
8/16-bit PPG timer 2 counter borrow	×	# 20	FFFFAC$_H$		
Extended I/O serial interface 0	○	# 21	FFFFA8$_H$	ICR05	0000B5$_H$
8/16-bit PPG timer 3 counter borrow	×	# 22	FFFFA4$_H$		
Extended I/O serial interface 1	○	# 23	FFFFA0$_H$	ICR06	0000B6$_H$
16-bit free-run timer (I/O timer) overflow	○	# 24	FFFF9C$_H$		
16-bit re-load timer 0	○	# 25	FFFF98$_H$	ICR07	0000B7$_H$
DTP6/7 (external interrupt 6/7)	○	# 26	FFFF94$_H$		
16-bit re-load timer 1	○	# 27	FFFF90$_H$	ICR08	0000B8$_H$
8/16-bit PPG timer 4/5 counter borrow	×	# 28	FFFF8C$_H$		
Input capture (ch.0) include (I/O timer)	○	# 29	FFFF88$_H$	ICR09	0000B9$_H$
Input capture (ch.1) include (I/O timer)	○	# 30	FFFF84$_H$		
Input capture (ch.2) include (I/O timer)	○	# 31	FFFF80$_H$	ICR10	0000BA$_H$
Input capture (ch.3) include (I/O timer)	○	# 32	FFFF7C$_H$		
Output compare (ch.0) match (Output timer)	○	#33	FFFF78$_H$	ICR11	0000BB$_H$
Output compare (ch.1) match (Output timer)	○	# 34	FFFF74$_H$		
Output compare (ch.2) match (Output timer)	○	# 35	FFFF70$_H$	ICR12	0000BC$_H$
Output compare (ch.3) match (Output timer)	○	# 36	FFFF6C$_H$		
UART transmission complete	○	# 37	FFFF68$_H$	ICR13	0000BD$_H$
I²C interface 0	×	# 38	FFFF64$_H$		
UART0 reception complete	◎	# 39	FFFF60$_H$	ICR14	0000BE$_H$
I²C interface 1	×	# 40	FFFF5C$_H$		
Flash memory status	×	# 41	FFFF58$_H$	ICR15	0000BF$_H$
Delayed interrupt generation module	×	# 42	FFFF54$_H$		

◎ :The interrupt request flag is cleared by the EI²OS interrupt clear signal. The stop request is available.

○ :The interrupt request flag is cleared by the EI²OS interrupt clear signal.

× :The interrupt request flag is not cleared by the EI²OS interrupt clear signal.

Note: On using the EI²OS Function with Extended I/O Serial Interface 2

If a resource has two interrupt sources for the same interrupt number, both of the interrupt request flags are cleared by the EI²OS interrupt clear signal. When the EI²OS function is used for one of the two interrupt sources, therefore, the other interrupt function cannot be used. Set the interrupt request enable bit for the relevant resource to “0” for software polling processing.

Interrupt source	Interrupt No.	Interrupt control register	Resource interrupt request
Extended I/O serial interface 1	# 23	ICR06	Enabled
16-bit free-run timer (I/O timer) overflow	# 24		Disabled

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$V_{CC} \geq AV_{CC}$ *1
	AVRH	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq AVRH \geq AVRL$
	AVRL	V_{SS} – 0.3	V_{SS} + 6.0	V	
Input voltage	V_I	V_{SS} – 0.3	V_{SS} + 6.0	V	*5
Output voltage	V_O	V_{SS} – 0.3	V_{SS} + 6.0	V	*5
Maximum clamp current	I_{CLAMP}	– 2.0	+ 2.0	mA	MB90552A/2B/3A/3B*6
		– 200	+ 200	µA	MB90F553A*6
Total maximum clamp current	$\Sigma\lvert I_{CLAMP} \rvert$	—	20	mA	MB90552A/2B/3A/3B*6
		—	2	mA	MB90F553A*6
“L” level maximum output current *2	I_{OL1}	—	10	mA	Other than P20 to P27
	I_{OL2}	—	20	mA	P20 to P27
“L” level average output current	I_{OLAV1}	—	4	mA	Other than P20 to P27
	I_{OLAV2}	—	12	mA	P20 to P27
“L” level total maximum output current	ΣI_{OL}	—	150	mA	
“L” level total average output current	ΣI_{OLAV}	—	80	mA	
“H” level maximum output current *2	I_{OH}	—	–15	mA	
“H” level average output current *3	I_{OHAV}	—	–4	mA	
“H” level total maximum output current	ΣI_{OH}	—	–100	mA	
“H” level total average output current *4	ΣI_{OHAV}	—	–50	mA	
Power consumption	P_D	—	550	mW	MB90P553A
			450	mW	MB90F553A
			200	mW	MB90553A/553B
			180	mW	MB90552A/552B
Operating temperature	T_A	–40	+85	°C	
Storage temperature	T_{STG}	–55	+150	°C	

*1 : Care must be taken that AVcc, AVRH, AVRL do not exceed Vcc.
Also, care must be taken that AVRH and AVRL do not exceed AVCC, and AVRL does not exceed AVRH.

*2 : The maximum output current is a peak value for a corresponding pin.

*3 : Average output current is an average current value observed for a 100 ms period for a corresponding pin.

*4 : Total average current is an average current value observed for a 100 ms period for all corresponding pins.

*5 : V_I and V_O should not exceed V_{CC} + 0.3V.

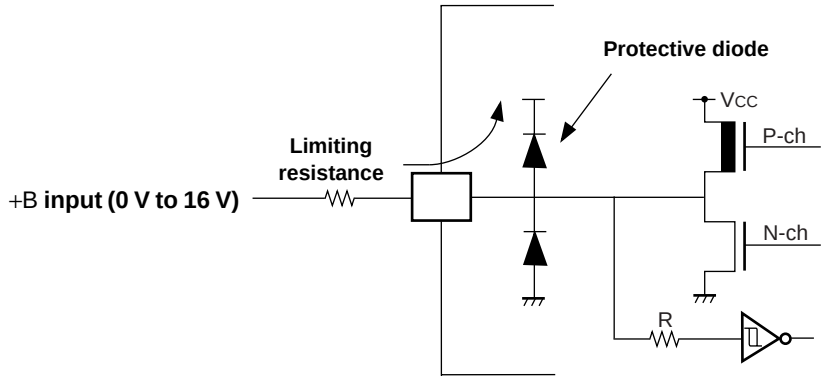
*6 : • Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA4

(Continued)

(Continued)

- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
- Set the value of the limiting resistance as the current to be input to the microcontroller at +B input is below the rated value, either instantaneously or for the prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller current is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that is the +B input is applied during power-on, the power supply is provided from the pins and resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits :

• Input/output equivalent circuits



Note: Average output current = operating current × operating efficiency

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

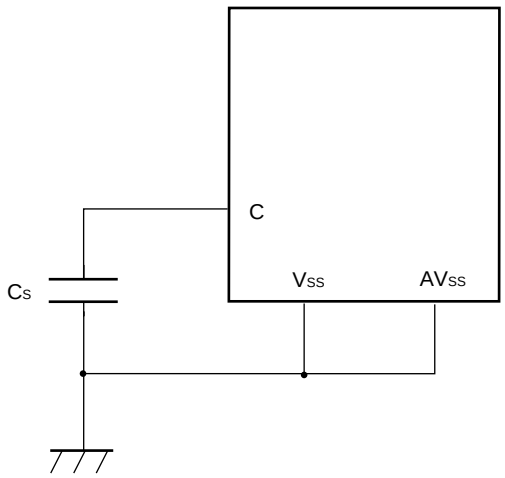
2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC} AV_{CC}	4.5	5.5	V	Normal operation (MB90F553A, MB90P553A, MB90V550A)
		3.5	5.5	V	Normal operation (MB90553A, MB90553B, MB90552A, MB90552B)
		3.5	5.5	V	Retains status at the time of operation stop
Smoothing capacitor	C_S	0.1	1.0	µF	*
Operating temperature	T_A	–40	+85	°C	

* : Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The smoothing capacitor to be connected to the V_{CC} pin must have a capacitance value higher than C_S.
For connecting smoothing capacitor C_S, see the diagram below:

• **C pin connection circuit**



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

(V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	CMOS input pin	—	0.7V_{CC}	—	V_{CC}+0.3	V	*1
	V_{IHS}	CMOS hysteresys input pin	—	0.8V_{CC}	—	V_{CC}+0.3	V	*2
	V_{IHM}	MD pin input	—	V_{CC} – 0.3	—	V_{CC}+0.3	V	*3
"L" level input voltage	V_{IL}	CMOS input pin	—	V_{SS} – 0.3	—	0.3V_{CC}	V	*1
	V_{ILS}	CMOS hysteresys input pin	—	V_{SS} – 0.3	—	0.2V_{CC}	V	*2
	V_{ILM}	MD pin input	—	V_{SS} – 0.3	—	V_{SS} +0.3	V	*3
Open-drain output pin voltage	V_D	P50 to P55	—	V_{SS} – 0.3	—	V_{SS} + 6.0	V	
"H" level output voltage	V_{OH}	Other than P50 to P55	V_{CC} = 4.5V, I_{OH} = –4.0mA	V_{CC} – 0.5	—	—	V	
"L" level output voltage 1	V_{OL1}	Other than P20 to P27	V_{CC} = 4.5V, I_{OL} = 4.0mA	—	—	0.4	V	
"L" level output voltage 2	V_{OL2}	P20 to P27	V_{CC} = 4.5V, I_{OL} = 12.0mA	—	—	0.4	V	
Input leakage current	I_{IL}	All output pins	V_{CC} = 5.5V, V_{SS} < V_I < V_{CC}	–5	—	5	µA	
Power supply current *4	I_{CC}	V_{CC}	Internal operation at 16 MHz V_{CC} = 5.5 V Normal operation	—	30	40	mA	MB90V550A
				—	80	110	mA	MB90P553A
				—	60	90	mA	MB90F553A
				—	30	40	mA	MB90553A/B
				—	25	35	mA	MB90552A/B
			When data written in flash mode	—	100	150	mA	MB90F553A
	I_{CCS}		Internal operation at 16 MHz V_{CC} = 5.5 V In sleep mode	—	7	10	mA	MB90V550A
				—	25	30	mA	MB90P553A
				—	10	20	mA	MB90F553A
				—	7	10	mA	MB90553A/B
				—	7	10	mA	MB90552A/B
	I_{CCH}		V_{CC} = 5.5V, T_A = +25°C In stop mode	—	5	20	µA	MB90V550A
				—	0.1	10	µA	MB90P553A
				—	5	20	µA	MB90F553A
				—	5	20	µA	MB90553A/B
				—	5	20	µA	MB90552A/B
Input capacitance	C_{IN}	Other than AV_{CC}, AV_{SS}, C, V_{CC} and V_{SS}	—	—	10	—	pF	
Open-drain output leakage current	I_{leak}	P50 to P55	—	—	0.1	5	µA	
Pull-up resistance	R_{UP}	P00 to P07 and P10 to P17 (In pull-up setting), $\overline{RST}$	—	25	50	100	kΩ	Other than MB90V550A
				20	40	100	kΩ	MB90V550A
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	kΩ	Only for mask ROM product

*1 : P00 to P07, P10 to P17, P20 to P27, P30 to P37

*2 : X0, $\overline{\text{HST}}$, $\overline{\text{RST}}$, P40 to P47, P50 to P55, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA4

*3 : MD0, MD1 and MD2

*4 : The current value is preliminary value and may be subject to change for enhanced characteristics without previous notice. The power supply current is measured with an external clock.

4. AC Characteristics

(1) Clock Timing

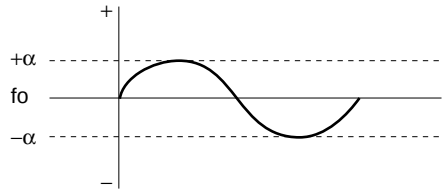
(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value			Unit	Unit
			Min	Typ	Max		
Oscillation clock frequency	F_C	X0, X1	3	—	16	MHz	
Oscillation clock cycle time	t_C	X0, X1	62.5	—	333	ns	
Frequency fluctuation rate locked*	Δf	—	—	—	5	%	
Input clock pulse width	P_{WH} P_{WL}	X0	10	—	—	ns	Recommended duty ratio of 40% to 60%
Input clock rising/falling time	t_{CR}, t_{CF}	X0	—	—	5	ns	External clock operation
Internal operating clock frequency	F_{CP}	—	8.0	—	16	MHz	PLL operation
			1.5	—	16	MHz	Main clock operation
Internal operating clock cycle time	t_{CP}	—	62.5	—	125	ns	PLL operation
			62.5	—	666	ns	Main clock operation

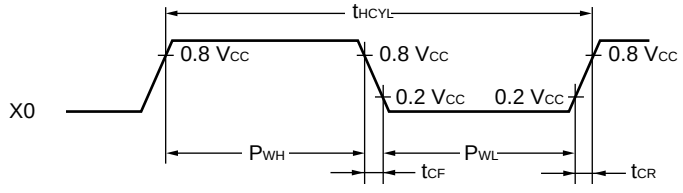
* : The frequency fluctuation rate is the maximum deviation rate of the preset center frequency when the multiplied PLL signal is locked.

$$\Delta f = \frac{|\alpha|}{fo} \times 100\ (\%)$$

Center frequency

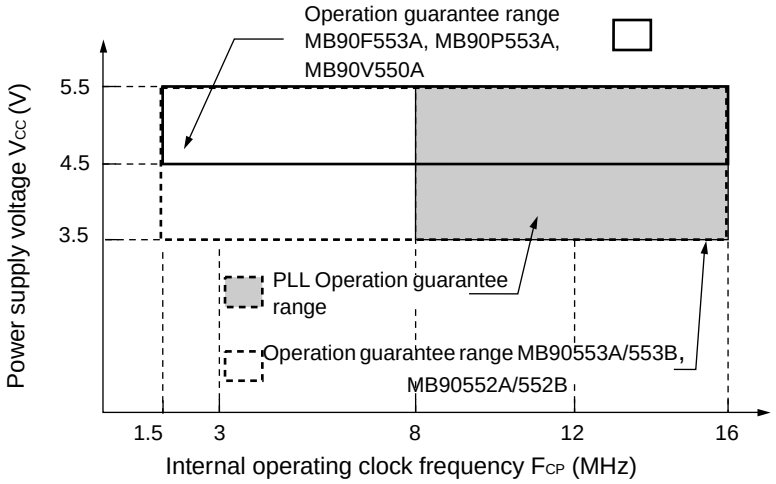


- **X0, X1 clock timing**

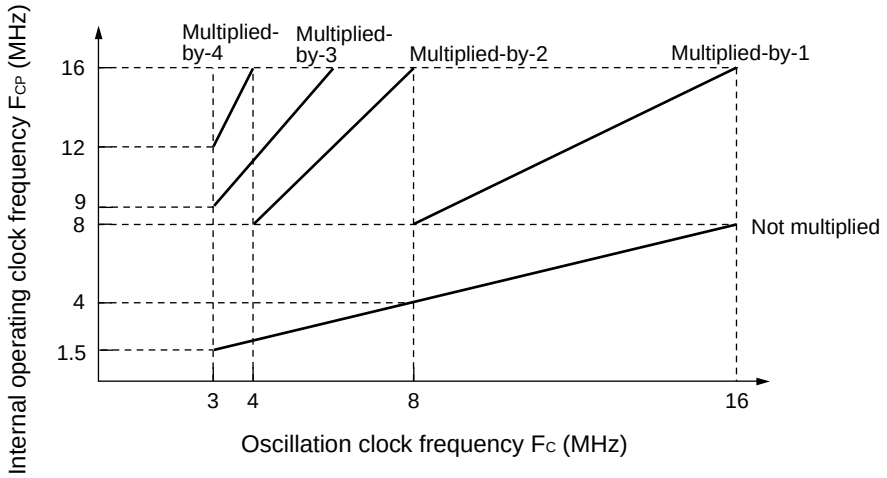


- **PLL operation guarantee range**

Relationship between internal operating clock frequency and power supply voltage



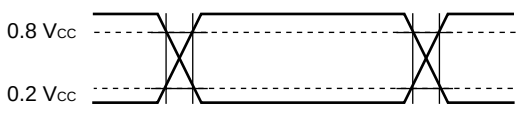
Relationship between oscillation clock frequency and internal operating clock frequency



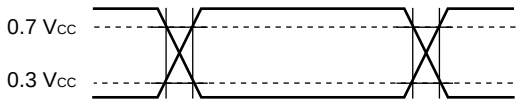
The AC ratings are measured for the following measurement reference voltages.

- **Input signal waveform**

Hystheresis input pin

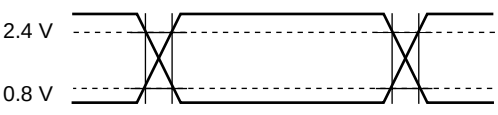


Pins other than hystheresis input / MD input



- **Output signal waveform**

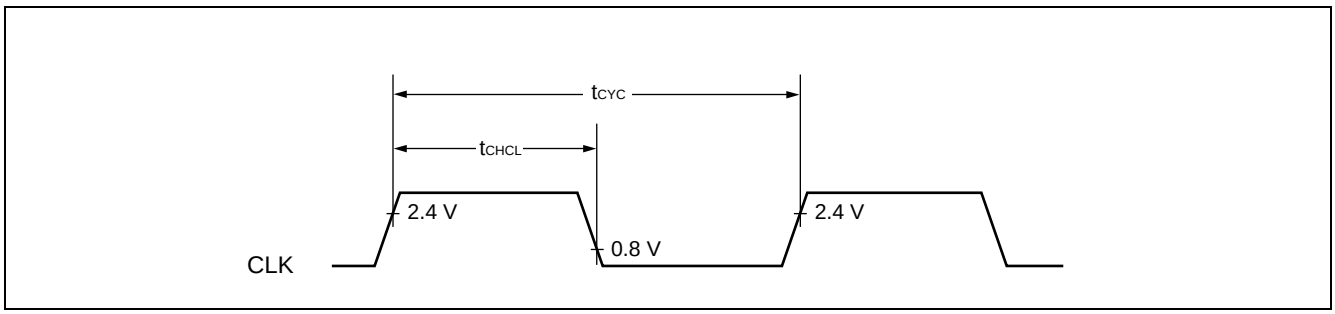
Output pin



(2) Clock Output Timing

(V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Cycle time	t_{CYC}	CLK	62.5	—	ns	
CLK ↑ → CLK ↓ time	t_{CHCL}		$t_{CP}/2 - 20$	$t_{CP}/2+20$	ns	



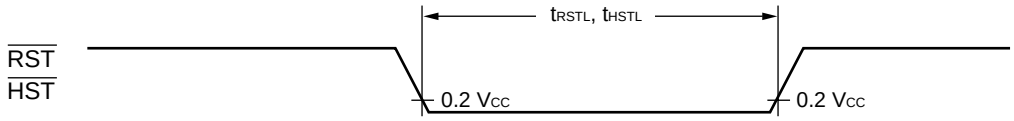
(3) Reset, Hardware Standby Input Timing

(V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

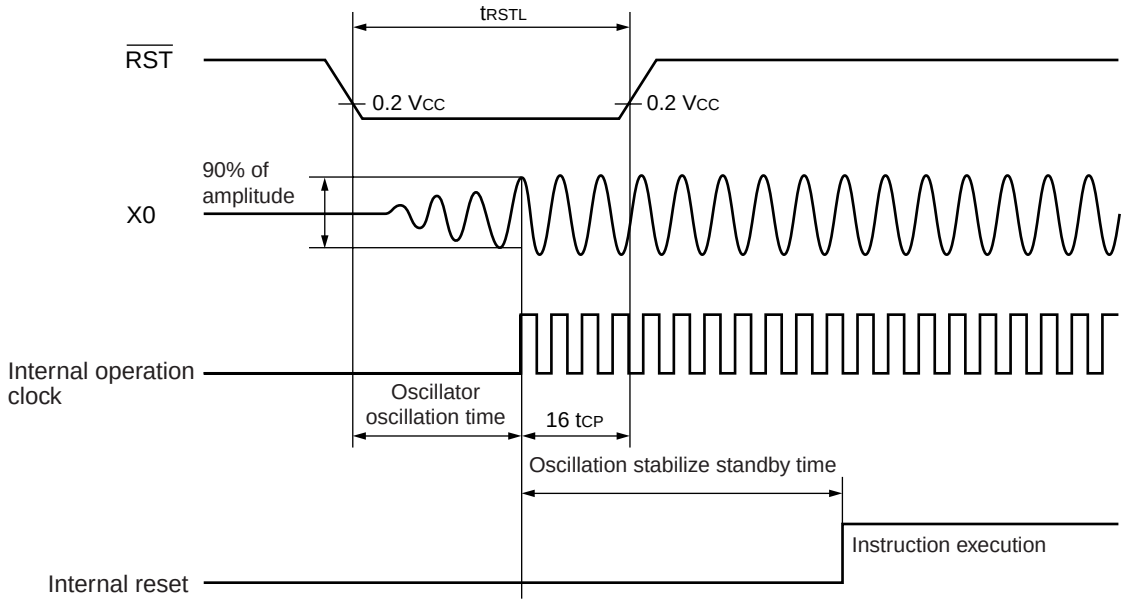
Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	16 t_{CP}	—	ns	Under normal operation
			Oscillation time of oscillator* + 16 t_{CP}	—	ms	In stop mode
Hardware standby input time	t_{HSTL}	$\overline{HST}$	16 t_{CP}	—	ns	Under normal operation

* : Oscillation time of oscillator is time that the amplitude reached the 90 %.
In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of µs to several ms. In the external clock, the oscillation time is 0 ms.

- **Under normal operation**



- **In stop mode**

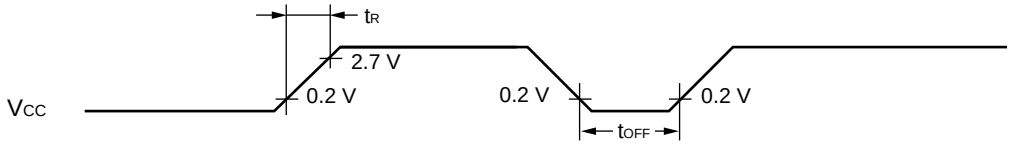


(4) Specification for Power-on Reset

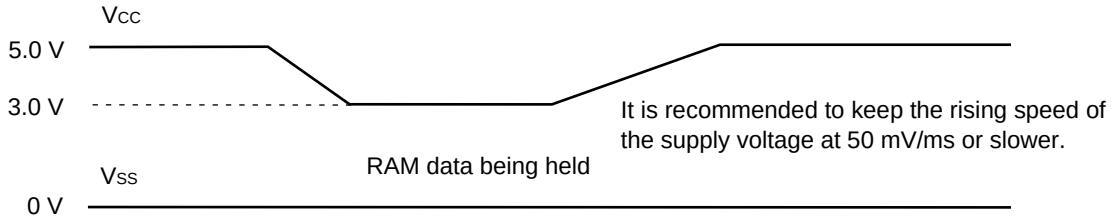
(V_{CC} = 5.0 V ± 10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	V_{CC}	0.05	30	ms	
Power-supply start voltage	V_{OFF}		—	0.2	V	
Power-supply end voltage	V_{ON}		2.7	—	V	
Power supply cut-off time	t_{OFF}		4	—	ms	Due to repeated operations

Notes:
- V_{CC} must be kept lower than 0.2 V before power-on.
- The above values are used for creating a power-on reset.
- Some registers in the device are initialized only upon a power-on reset. To initialize these register, turn on the power supply using the above values.



Sudden changes in the power supply voltage may cause a power-on reset.
To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below.
In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 V or fewer per second, however, you can use the PLL clock.

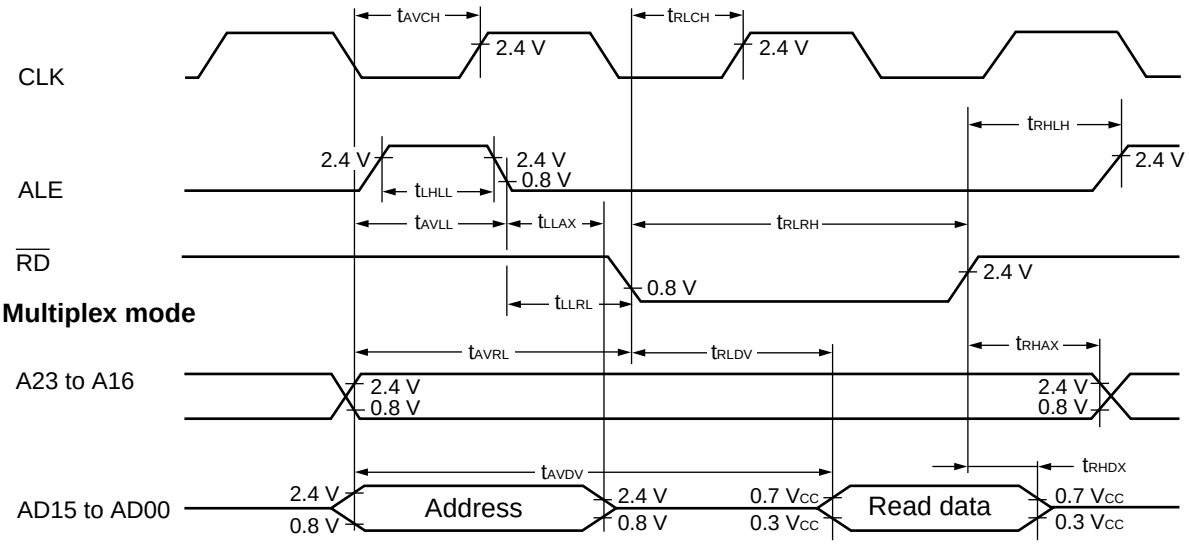


(5) Bus Read Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
ALE pulse width	t_{LHLL}	ALE	$t_{CP}/2 - 20$	—	ns	
Effective address → ALE ↓ time	t_{AVLL}	ALE, A23 to A16, AD15 to AD00	$t_{CP}/2 - 20$	—	ns	
ALE ↓ → address effective time	t_{LLAX}	ALE, AD15 to AD00	$t_{CP}/2 - 15$	—	ns	
Effective address → $\overline{RD}$ ↓ time	t_{AVRL}	A23 to A16, AD15 to AD00, $\overline{RD}$	$t_{CP} - 15$	—	ns	
Effective address → valid data input	t_{AVDV}	A23 to A16, AD15 to AD00	—	$5\ t_{CP}/2 - 60$	ns	
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$	$3\ t_{CP}/2 - 20$	—	ns	
$\overline{RD}$ ↓ → valid data input	t_{RLDV}	$\overline{RD}$, AD15 to AD00	—	$3\ t_{CP}/2 - 60$	ns	
$\overline{RD}$ ↑ → data hold time	t_{RHDX}	$\overline{RD}$, AD15 to AD00	0	—	ns	
$\overline{RD}$ ↑ → ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE	$t_{CP}/2 - 15$	—	ns	
$\overline{RD}$ ↑ → address effective time	t_{RHAX}	$\overline{ALE}$, A23 to A16	$t_{CP}/2 - 10$	—	ns	
Effective address → CLK ↑ time	t_{AVCH}	A23 to A16, AD15 to AD00, CLK	$t_{CP}/2 - 20$	—	ns	
$\overline{RD}$ ↓ → CLK ↑ time	t_{RLCH}	$\overline{RD}$, CLK	$t_{CP}/2 - 20$	—	ns	
ALE ↓ → $\overline{RD}$ ↓ time	t_{LLRL}	ALE, $\overline{RD}$	$t_{CP}/2 - 15$	—	ns	

- **Bus read timing**



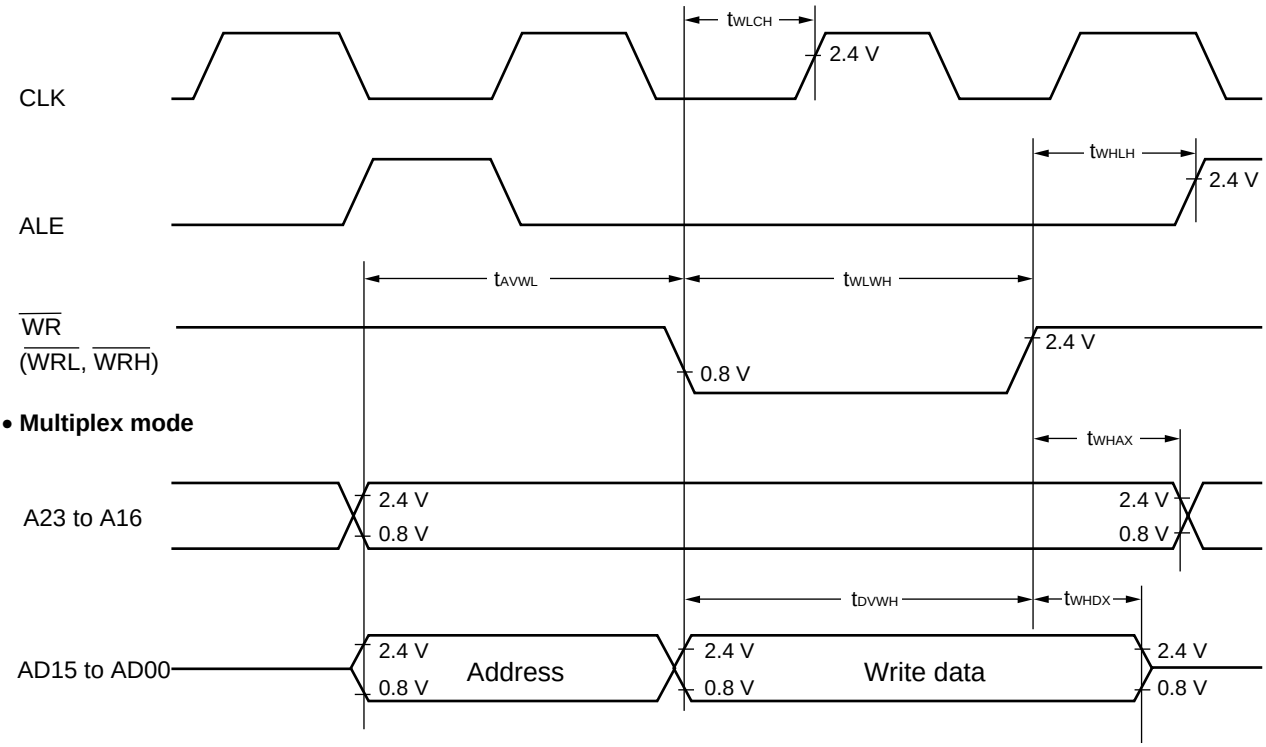
- **Multiplex mode**

(6) Bus Write Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Effective address → $\overline{WR}$ ↓ time	t_{AVWL}	A23 to A16, AD15 to AD00, $\overline{WRH}$, $\overline{WRL}$	t_{CP} – 15	—	ns	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WRH}$, $\overline{WRL}$	3 t_{CP}/2 – 20	—	ns	
valid data output→ $\overline{WR}$ ↑ time	t_{DVWH}	AD15 to AD00, $\overline{WRH}$, $\overline{WRL}$	3 t_{CP}/2 – 20	—	ns	
$\overline{WR}$ ↑ → data hold time	t_{WHDX}	AD15 to AD00, $\overline{WRH}$, $\overline{WRL}$	20	—	ns	Multiplex mode
$\overline{WR}$ ↑ → address effective time	t_{WHAX}	A23 to A16, $\overline{WRH}$, $\overline{WRL}$	t_{CP}/2 – 10	—	ns	
$\overline{WR}$ ↑ → ALE ↑ time	t_{WHLH}	$\overline{WRH}$, $\overline{WRL}$, ALE	t_{CP}/2 – 15	—	ns	
$\overline{WR}$ ↓ → CLK ↑ time	t_{WLCH}	$\overline{WRH}$, $\overline{WRL}$, CLK	t_{CP}/2 – 20	—	ns	

- **Bus write timing**



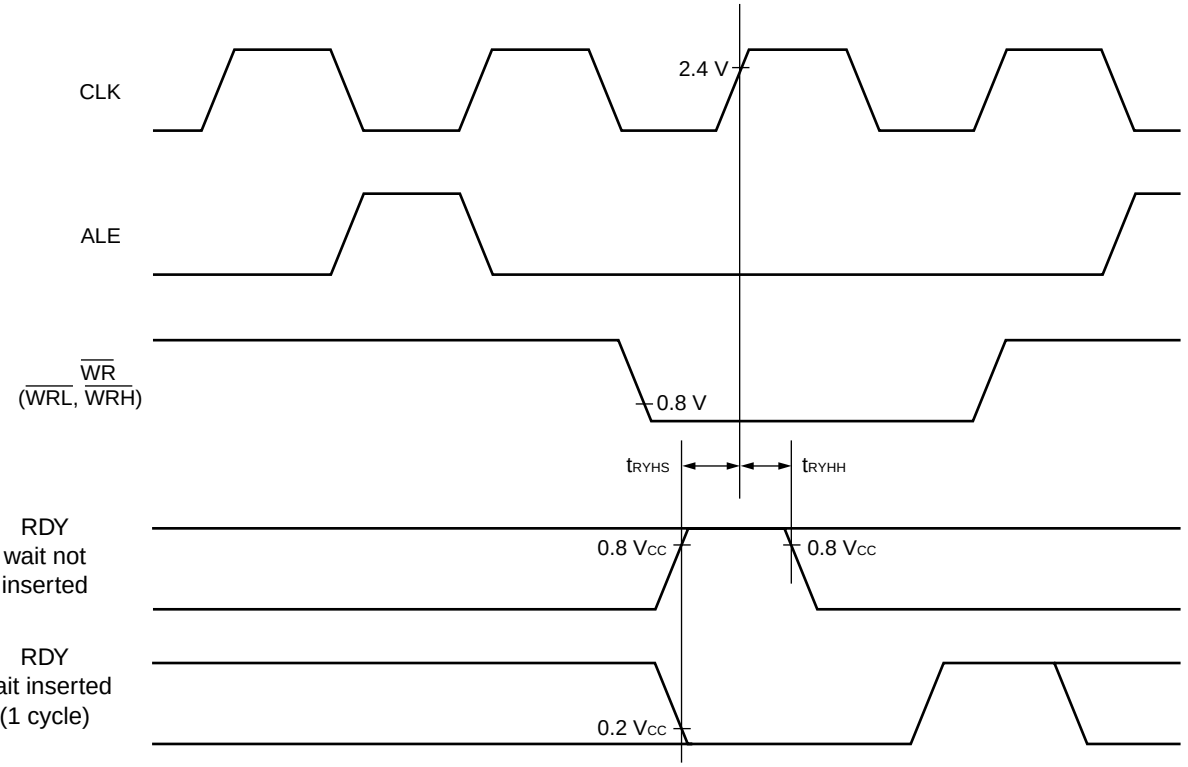
(7) Ready Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
RDY setup time	t_{RYHS}	RDY CLK	45	—	ns	
RDY hold time	t_{RYHH}		0	—	ns	

Note : Use the automatic ready function when the setup time for the rising edge of the RDY signal is not sufficient.

- **Ready input timing**



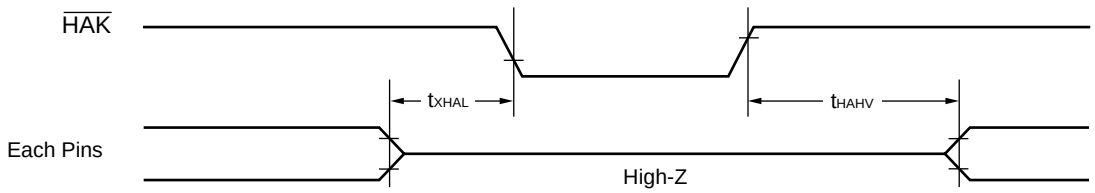
(8) Hold Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Pins in floating status → $\overline{HAK}$ ↓ time	t_{XHAL}	$\overline{HAK}$	30	t_{CP}	ns	
$\overline{HAK}$ ↑ → pin valid time	t_{HAHV}		t_{CP}	2 t_{CP}	ns	

Note : More than 1 machine cycle is needed before $\overline{HAK}$ changes after HRQ pin is fetched.

- **Hold timing**



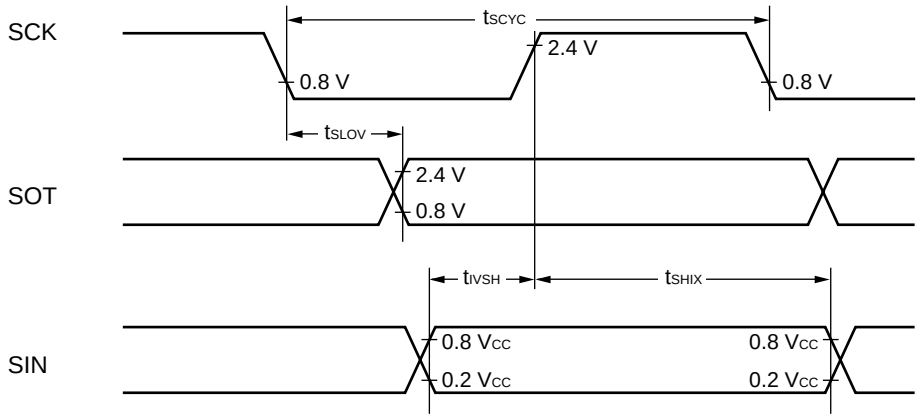
(9) UART, Extended I/O Serial 0, 1 Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

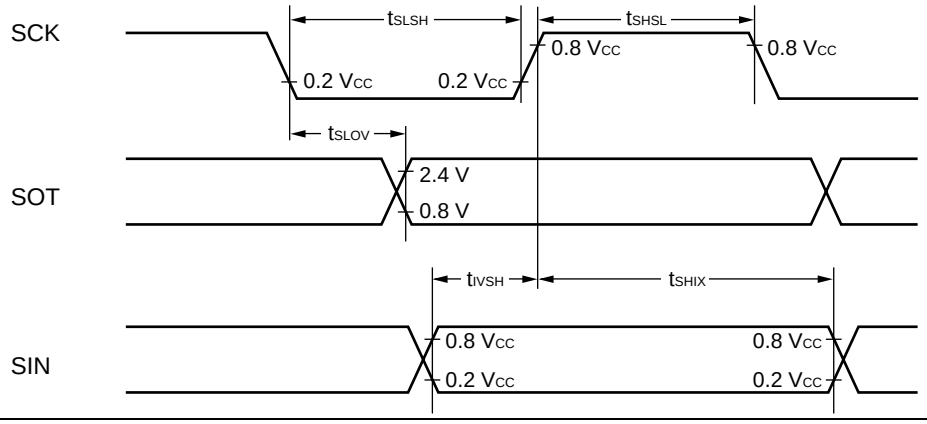
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK2	Internal shift clock mode C_L = 80 pF + 1 TTL for an output pin	8 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		–80	80	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		100	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		t_{CP}	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK2	External shift clock mode C_L = 80 pF + 1 TTL for an output pin	4 t_{CP}	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK2		4 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		—	150	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	

Notes: • These are AC ratings in the CLK synchronous mode.
• C_L is the load capacitance value connected to pins while testing.

- **Internal shift clock mode**



- **External shift clock mode**

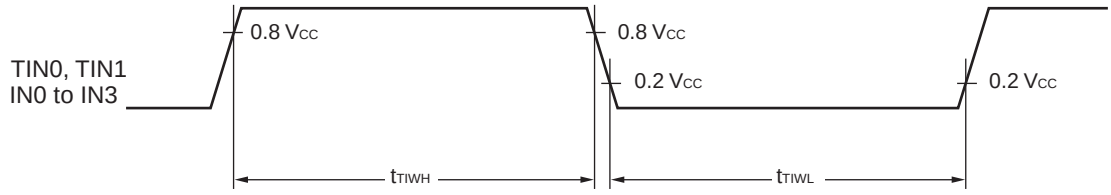


(10) Timer Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	TIN0, TIN1 IN0 to IN3	4 t_{CP}	—	ns	

- **Timer input timing**

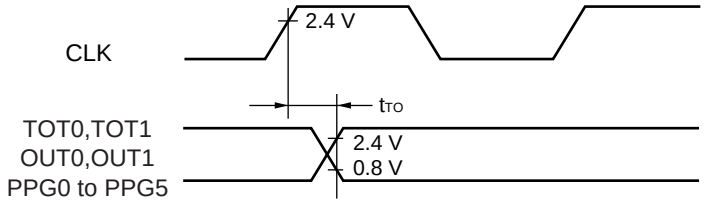


(11) Timer Output Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
CLK ↑ → T_{OUT} transition time	t_{TO}	TOT0,TOT1,OUT0, OUT1,PPG0 to PPG5	30	—	ns	

- **Timer output timing**

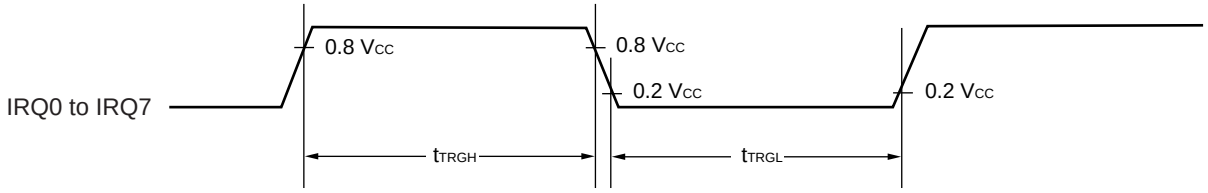


(12) Trigger Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	IRQ0 to IRQ7	5 t_{CP}	—	ns	Under normal operation
			1	—	µs	In stop mode

- **Trigger input timing**



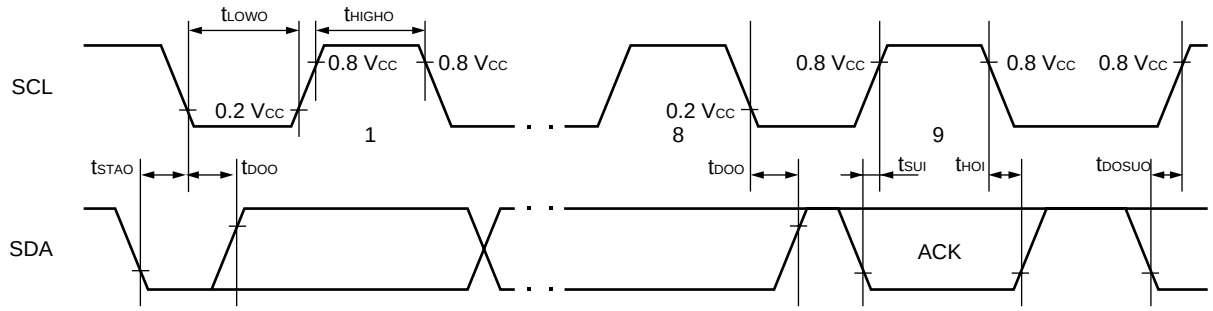
(13) I²C Interface

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

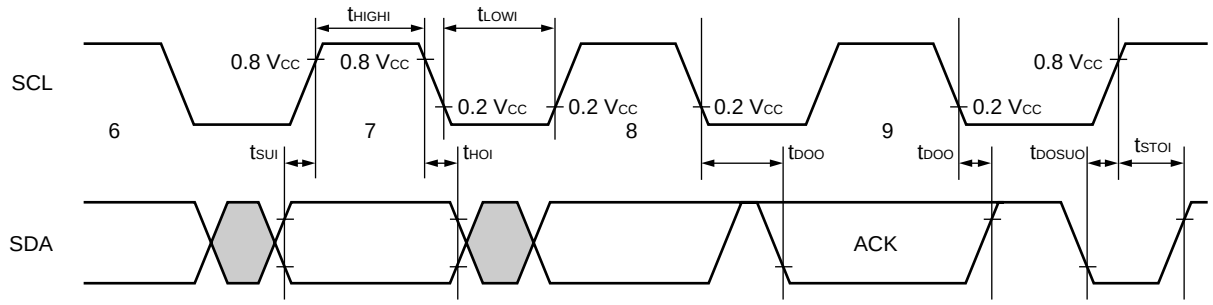
Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Internal clock cycle time	t_{CP}	—	62.5	666	ns	All products
Start condition output	t_{STAO}	SDA0 to SDA2 SCL0 toSCL2	$t_{CP} \times m \times n/2 - 20$	$t_{CP} \times m \times n/2 + 20$	ns	Only as master
Stop condition output	t_{STOO}		$t_{CP}(m \times n/2 + 4) - 20$	$t_{CP}(m \times n/2 + 4) + 20$	ns	
Start condition detection	t_{STAI}		$3\ t_{CP} + 40$	—	ns	Only as slave
Stop condition detection	t_{STOI}		$3\ t_{CP} + 40$	—	ns	
SCL output “L” width	t_{LOWO}	SCL0 to SCL2	$t_{CP} \times m \times n/2 - 20$	$t_{CP} \times m \times n/2 + 20$	ns	Only as master
SCL output “H” width	t_{HIGHO}		$t_{CP}(m \times n/2 + 4) - 20$	$t_{CP}(m \times n/2 + 4) + 20$	ns	
SDA output delay time	t_{DOO}	SDA0 to SDA2 SCL0 to SCL2	$2\ t_{CP} - 20$	$2\ t_{CP} + 20$	ns	
Setup after SDA output interrupt period	t_{DOSUO}		$4\ t_{CP} - 20$	—	ns	
SCL input “L” width	t_{LOWI}	SCL0 to SCL2	$3\ t_{CP} + 40$	—	ns	
SCL input “H” width	t_{HIGHI}		$t_{CP} + 40$	—	ns	
SDA input setup time	t_{SUI}	SDA0 to SDA2 SCL0 to SCL2	40	—	ns	
SDA input hold time	t_{HOI}		0	—	ns	

Notes: • “m” and “n” in the above table represent the values of shift clock frequency setting bits (CS4 to CS0) in the clock control register “ICCR”. For details, refer to the register description in the hardware manual.
• t_{DOSUO} represents the minimum value when the interrupt period is equal to or greater than the SCL “L” width.
• The SDA and SCL output values indicate that that rise time is 0 ns.

- **I²C interface [data transmitter (master/slave)]**



- **I²C interface [data receiver (master/slave)]**



5. A/D Converter

(1)Electrical Characteristics

(4.5 V ≤ AVRH – AVRL, V_{CC} = AV_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	10	—	bit	
Total error	—	—	—	—	±5.0	LSB	
Non-linearity error	—	—	—	—	±2.5	LSB	
Differential linearity error	—	—	—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AVRL–3.5LSB	AVRL+0.5LSB	AVRL+4.5LSB	V	1LSB= (AVRH–AVRL) /1024
Full-scale transition voltage	V_{FST}	AN0 to AN7	AVRH–6.5LSB	AVRH–1.5LSB	AVRH+1.5LSB	V	
Sampling period	t_{SMP}	—	64	—	4096	t_{CP}	
Compare time	t_{CMP}	—	22	—	—	µs	*1
A/D Conversion time	t_{CNV}	—	26.3	—	—	µs	*2
Analog port input current	I_{AIN}	AN0 to AN7	—	—	10	µA	
Analog input voltage	V_{AIN}	AN0 to AN7	AVRL	—	AVRH	V	
Reference voltage	—	AVRH	AVRL + 4.5	—	AV_{CC}	V	
	—	AVRL	0	—	AVRH – 4.5	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.0	mA	
	I_{AH}		—	—	5	µA	*3
Reference voltage supply current	I_R	AVRH	—	300	500	µA	
	I_{RH}		—	—	5	µA	*3
Offset between channels	—	AN0 to AN7	—	—	4	LSB	

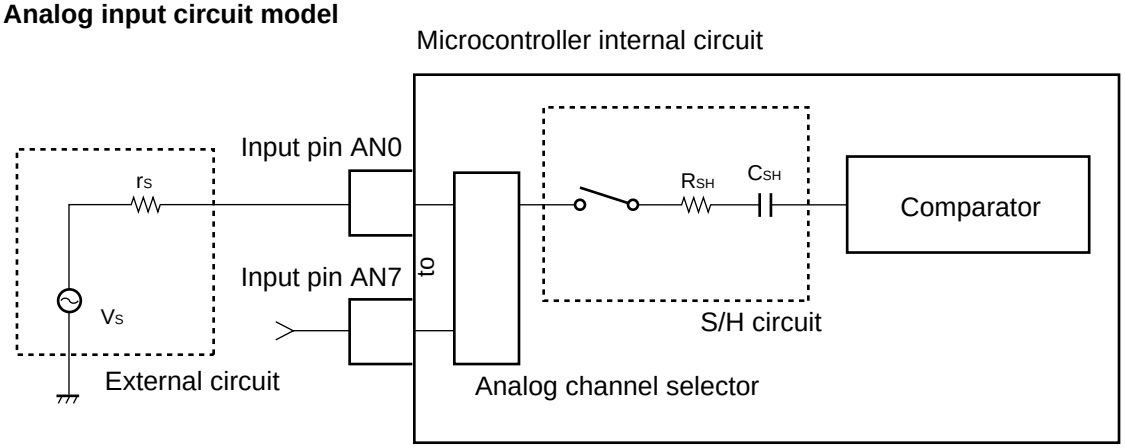
*1: When F_{CP} = 8 MHz, t_{CMP} = 176 × t_{CP}. When F_{CP} = 16 MHz, t_{CMP} = 352 × t_{CP}.

*2: Equivalent to the time for conversion per channel if "t_{SMP} = 64 × t_{CP}" or "t_{CMP} = 352 × t_{CP}" is selected when F_{CP} = 16 MHz.

*3: Specifies the power-supply current (Vcc = AVcc = AVRH = 5.0 V) when the A/D converter is inactive and the CPU has been stopped.

Notes:
- The error becomes larger relatively as |AVRH-AVRL| becomes smaller.
- Use the output impedance r_S of the external circuit for analog input under the following condition: External circuit output impedance r_S = 10 kΩ Max.
- If the output impedance of the external circuit is too high, the analog voltage sampling time may be insufficient.
- If you insert a DC-blocking capacitor between the external circuit and the input pin, select a capacitance that is about several thousands times the sampling capacitance C_{SH} in the chip to suppress the effect of capacity potential division with C_{SH}.

- **Analog input circuit model**



<Recommended/reference values for device parameters>

r_S = 10 kΩ or less

R_{SH} = About 3 kΩ

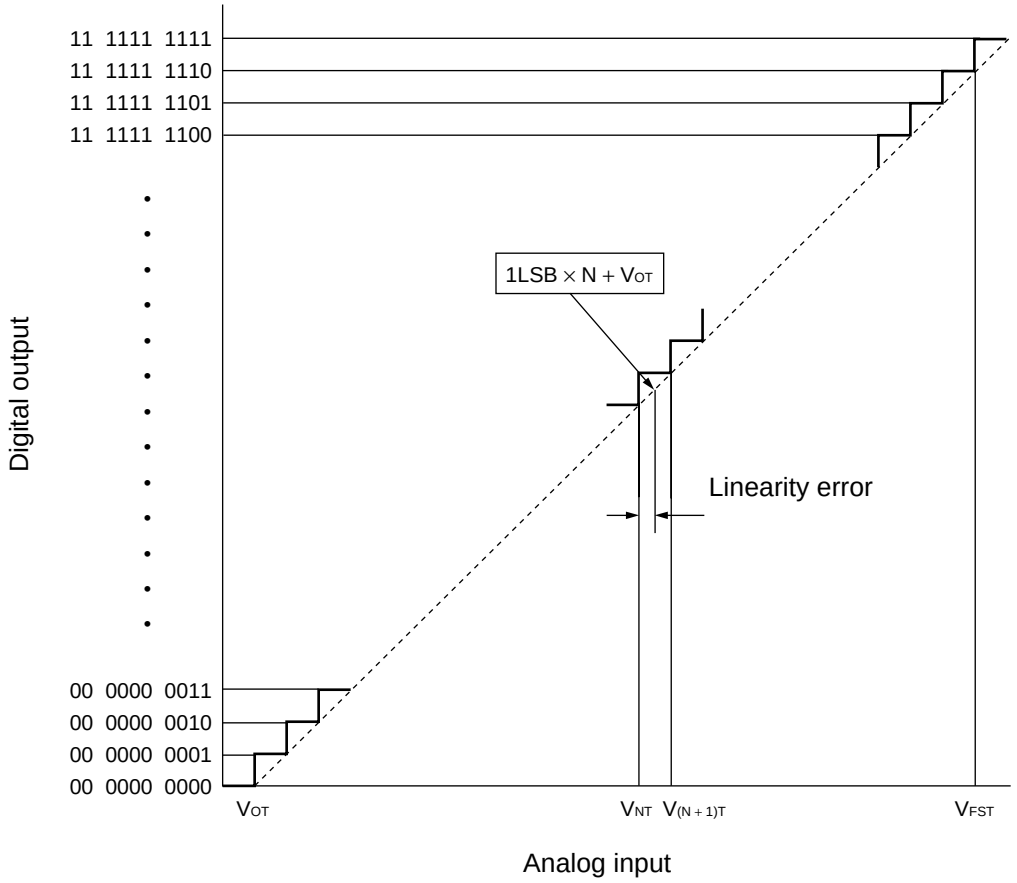
C_{SH} = About 25 pF

Note: Device parameter values are provided as reference values for design purposes; they are not guaranteed.

(2) Definitions of Terms

- Resolution: Analog transition identifiable by the A/D converter.
  Analog voltage can be divided into 1024 (2^{10}) components at 10-bit resolution.
- Total error: Difference between actual and logical values. This error is the sum of an offset error, gain error, non-linearity error and an error caused by noise.
- Linearity error: Deviation of the straight line drawn between the zero transition point (00 0000 0000 <-> 00 0000 0001) and the full-scale transition point (11 1111 1110 <-> 11 1111 1111) of the device from actual conversion characteristics
- Differential linearity error: Deviation from the ideal input voltage required to shift output code by one LSB

- **10-bit A/D converter conversion characteristics**



$$1LSB = \frac{V_{FST} - V_{OT}}{1022}$$

$$\text{Linearity error} = \frac{V_{NT} - (1LSB \times N + V_{OT})}{1LSB} \text{ [LSB]}$$

$$\text{Differential linearity error} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

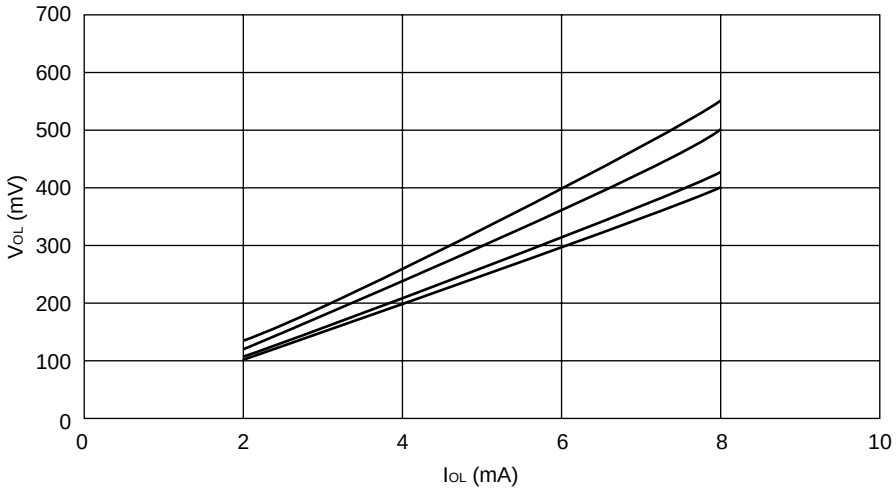
6. Flash Memory Program/Erase Characteristics

Parameter	Condition	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = + 25 °C V_{CC} = 5.0 V	—	1.5	30	s	Excludes 00H programming prior erasure
Chip erase time		—	10.5	—	s	Excludes 00H programming prior erasure
Word (16-bit width) programming time		—	16	500	µs	Excludes system-level overhead
Program/Erase cycle	—	100,000	—	—	cycle	Guaranteed 100,000 cycles
		10,000	—	—	cycle	Guaranteed 10,000 cycles
Data hold time	—	100,000	—	—	h	

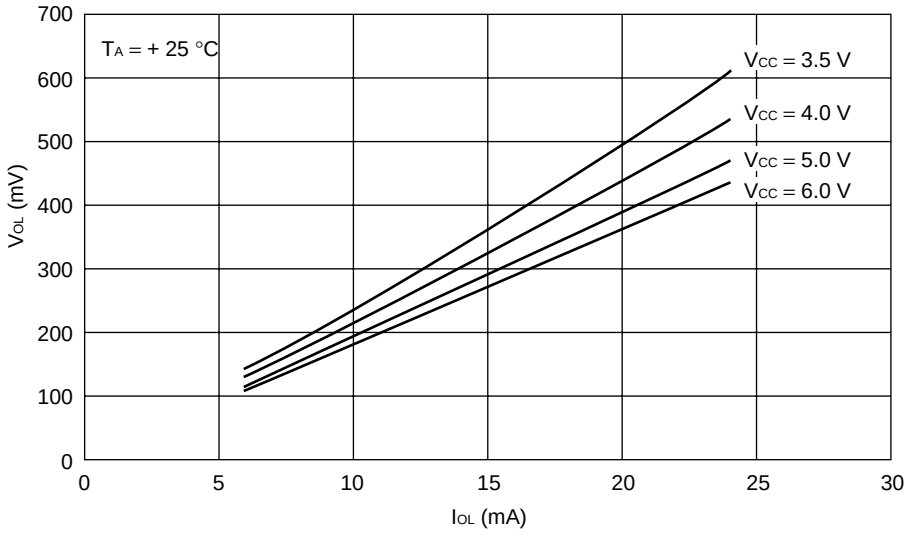
■ EXAMPLE CHARACTERISTICS

1. “L” level output voltage

V_{OL} – I_{OL}
Other than P20 to P27

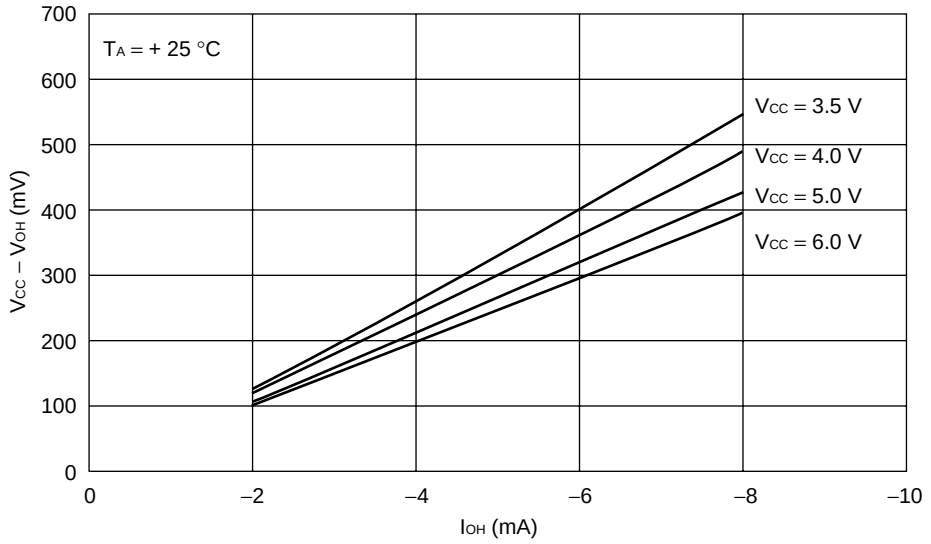


V_{OL} – I_{OL}
P20 to P27



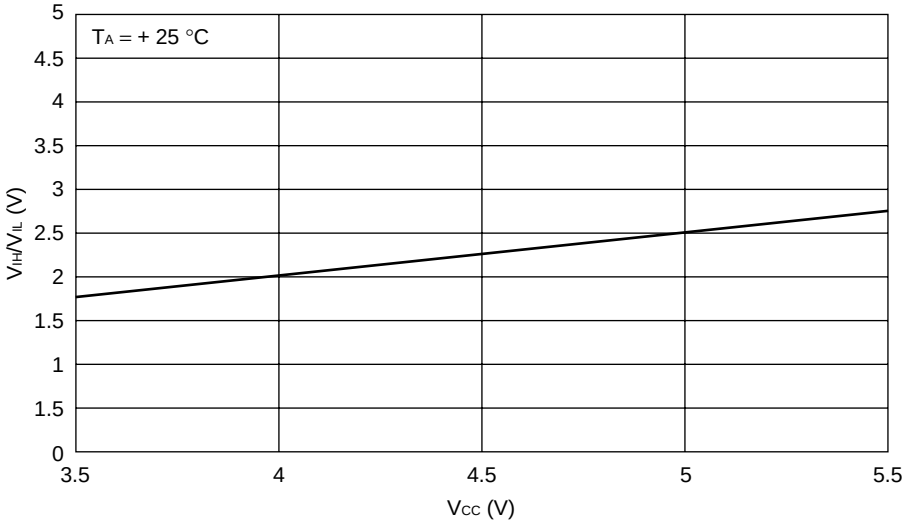
2. “H” level output voltage

$(V_{CC} - V_{OH}) - I_{OH}$
Other than P50 to P55

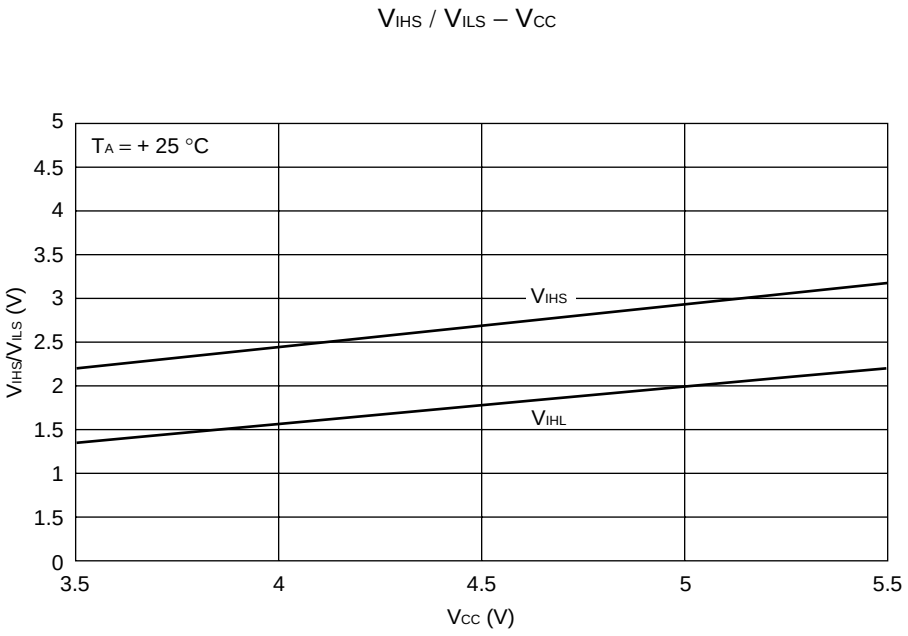


3. “H” level input voltage / “L” level input voltage (CMOS input)

$V_{IH} / V_{IL} - V_{CC}$



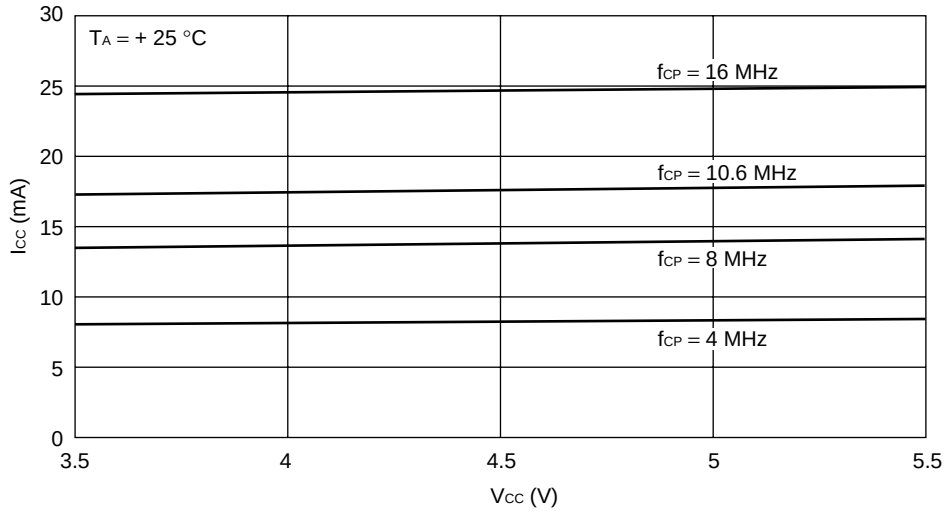
4. “H” level input voltage / “L” level input voltage (CMOS hysteresis input)



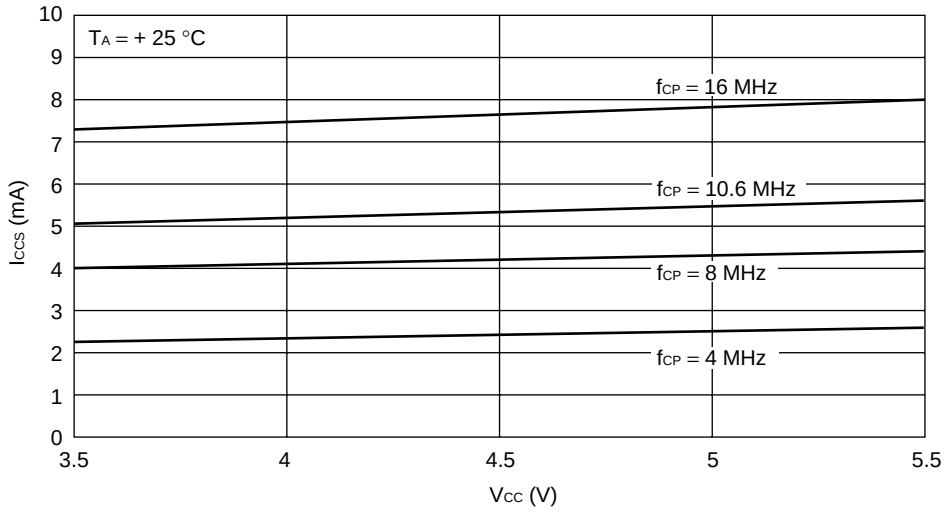
5. Power supply current
(f_{CP} = internal operating clock frequency)

- MB90552A/B
- Measurement conditions: External clock mode, ROM read loop operation, without resource operation, Typ sample, internal operating frequency = 4MHz (external rectangular wave clock at 8MHz), T_A = + 25 °C

I_{CC} – V_{CC}



I_{CCS} – V_{CC}

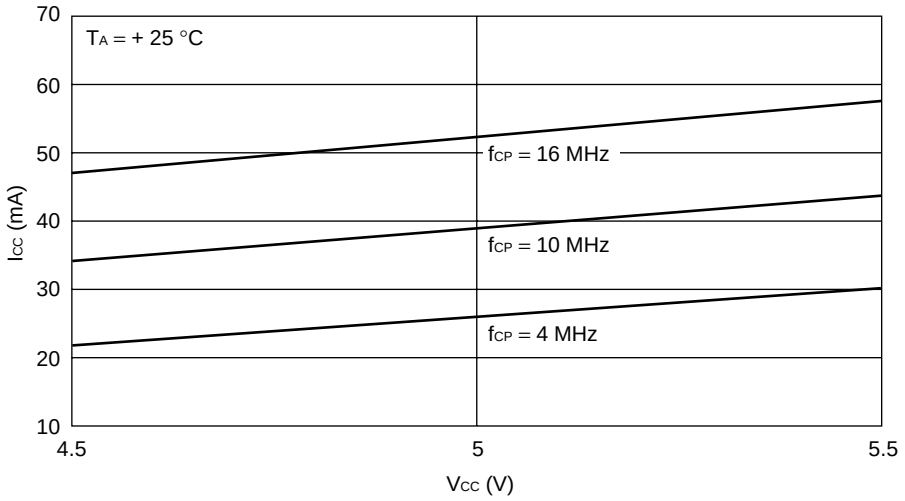


(Continued)

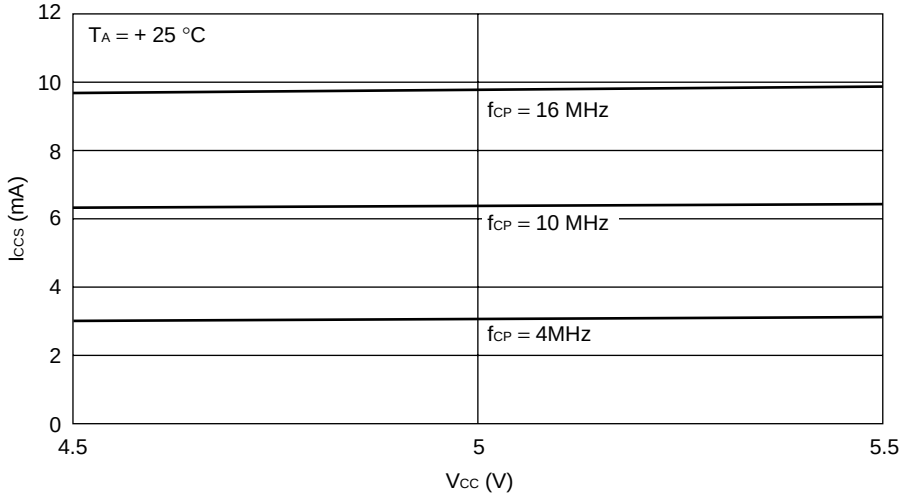
(Continued)

- MB90F553A
- Measurement conditions: External clock mode, ROM read loop operation, without resource operation, Typ sample, internal operating frequency = 4MHz (external rectangular wave clock at 8MHz), T_A = +25 °C

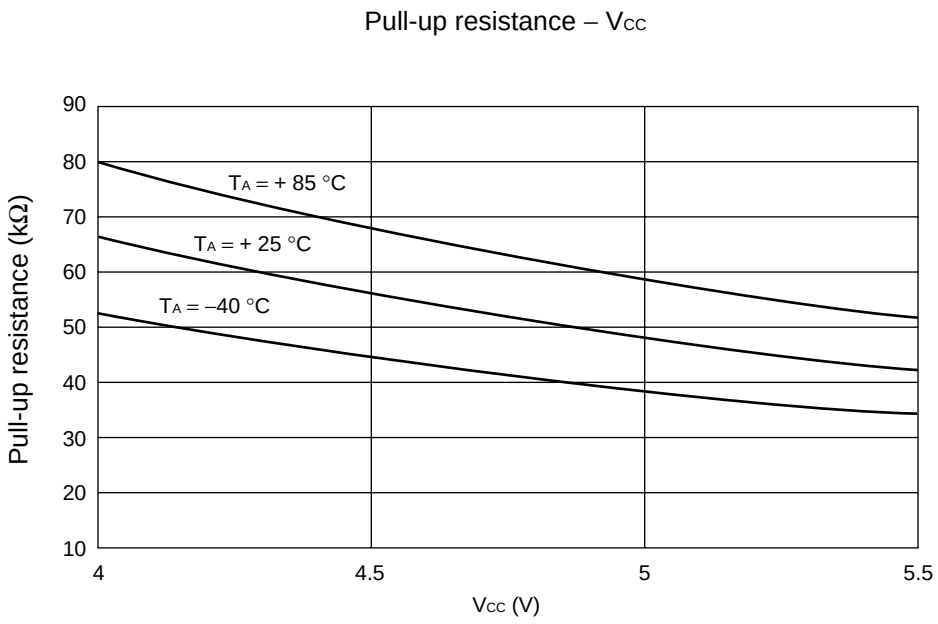
I_{CC} – V_{CC}



I_{CCS} – V_{CC}



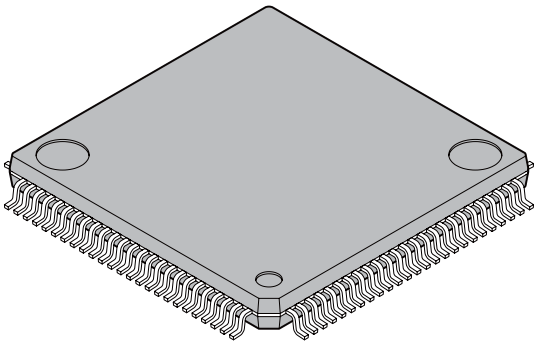
6. Pull-up resistance



■ ORDERING INFORMATION

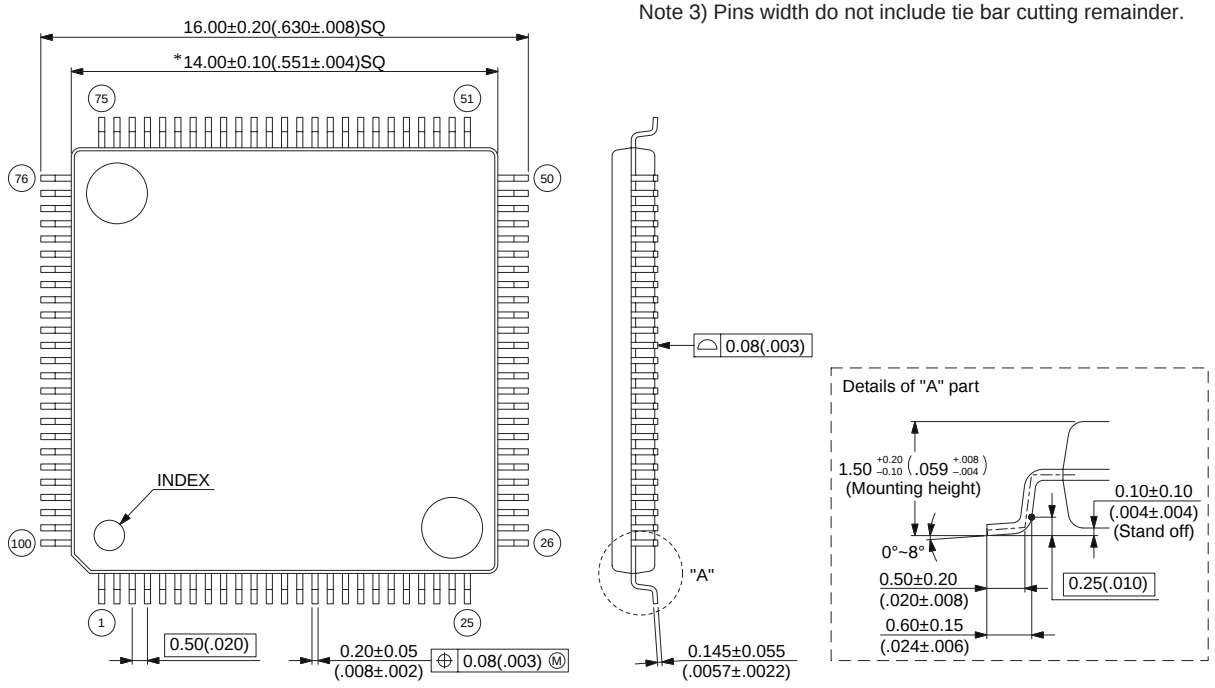
Part number	Package	Remarks
MB90552APF MB90552BPF MB90553APF MB90553BPF MB90T552APF MB90T553APF MB90F553APF MB90P553APF	100-pin plastic QFP (FPT-100P-M06)	
MB90552APMC MB90552BPMC MB90553APMC MB90553BPMC MB90T552APMC MB90T553APMC MB90F553APMC MB90P553APMC	100-pin plastic LQFP (FPT-100P-M20)	

■ PACKAGE DIMENSIONS

100-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	14.0 mm × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.65 g
(FPT-100P-M20)	Code (Reference)	P-LFQFP100-14×14-0.50

100-pin plastic LQFP
(FPT-100P-M20)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

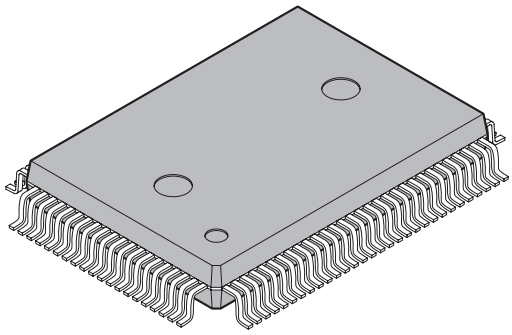


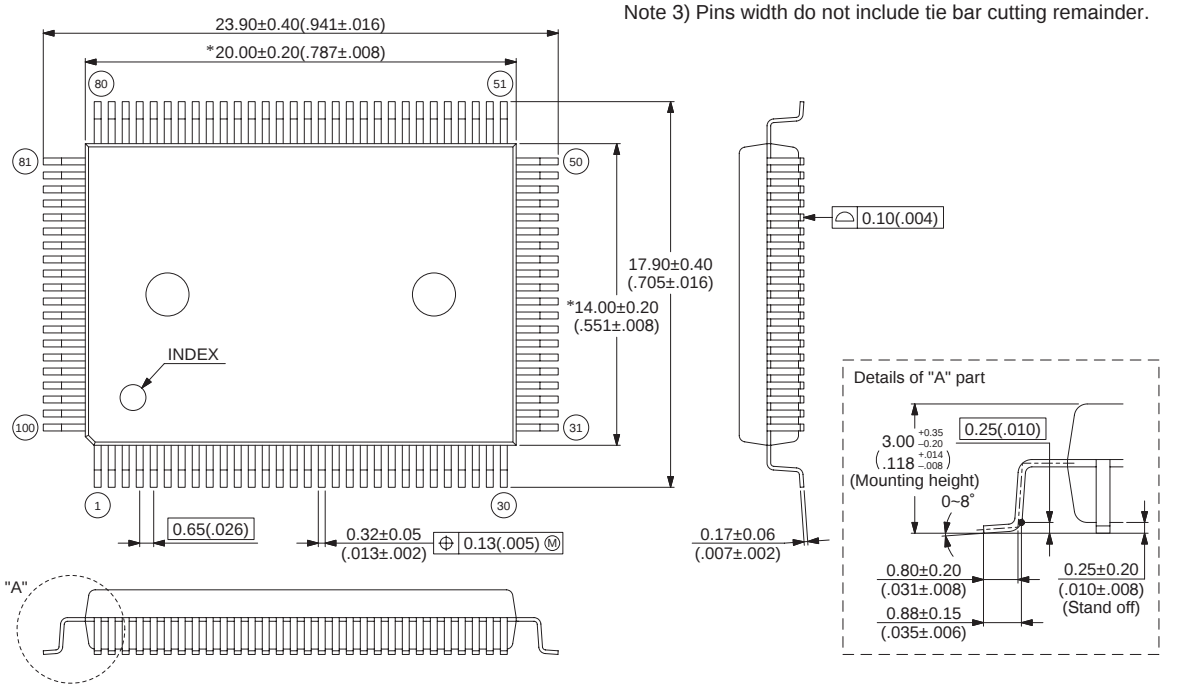
Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

(Continued)

(Continued)

100-pin plastic QFP		
 (FPT-100P-M06)	Lead pitch	0.65 mm
	Package width × package length	14.00 × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14×20-0.65



Please confirm the latest Package dimension by following URL.
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■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
—	—	The package code is changed. (FPT-100P-M05 → FPT-100P-M20)
59	■ ORDERING INFORMATION	Order informations are changed. (MB90552APFV → MB90552APMC MB90552BPFV → MB90552BPMC MB90553APFV → MB90553APMC MB90553BPFV → MB90553BPMC MB90T552APFV → MB90T552APMC MB90T553APFV → MB90T553APMC MB90F553APFV → MB90F553APMC MB90P553APFV → MB90P553APMC)
60	■ PACKAGE DIMENSIONS	The package figure is changed. (FPT-100P-M05 → FPT-100P-M20)

The vertical lines marked in the left side of the page show the changes.

MEMO

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