SP6139

Wide Input, 1.3MHz Synchronous PWM Step Down Controller

January 2009 Rev. 2.0.0

GENERAL DESCRIPTION

The SP6139 is a 1300kHz constant frequency, voltage mode, synchronous PWM step down controller optimized for high efficiency.

The SP6139 is adequately suited for split plane applications utilizing a low power 5V rail to power the controller circuitry, minimizing power dissipation. Its wide input voltage range of 3V to 15V allows for conversions from the standard 3.3V, 5V, 9.6V and 12V power rails to an output voltage adjustable down to 0.8V. Developed around a wide bandwidth internal amplifier, the SP6139 can accommodate type II and type III compensation schemes.

Protection features include a programmable UVLO, thermal shutdown and output short circuit protection.

The SP6139 is part of a larger family of step down controllers operating at various switching frequencies up to 1300kHz and input voltages up to 28V. Refer to Exar's SP6132, SP6132H, SP6134, SP6134H and SP6137 for complete details.

The SP6139 is available in lead free, RoHS compliant, space saving 10-pin MSOP package.

APPLICATIONS

- **DSL Modems**
- **Set-Top Boxes**
- **12V V_{IN} Point of Load Applications**

FEATURES

- **2.5V to 20V Step Down Achieved Using Dual Input**
- **On-Board 1.5Ω sink (2Ω source) NFET Drivers**
- **Up to 7A Output Capability**
- **UVLO Detects Both VCC and VIN**
- **Short-Circuit Protection with Auto-Restart**
- **Supports Type II or III Compensation**
- **Programmable Soft Start**
- **Fast Transient Response**
- **High Efficiency: Greater than 94%**
- **Non-synchronous Start-Up**
- **Small 10-Pin MSOP Package**
- **U.S. Patent #6,922,041**

TYPICAL APPLICATION DIAGRAM

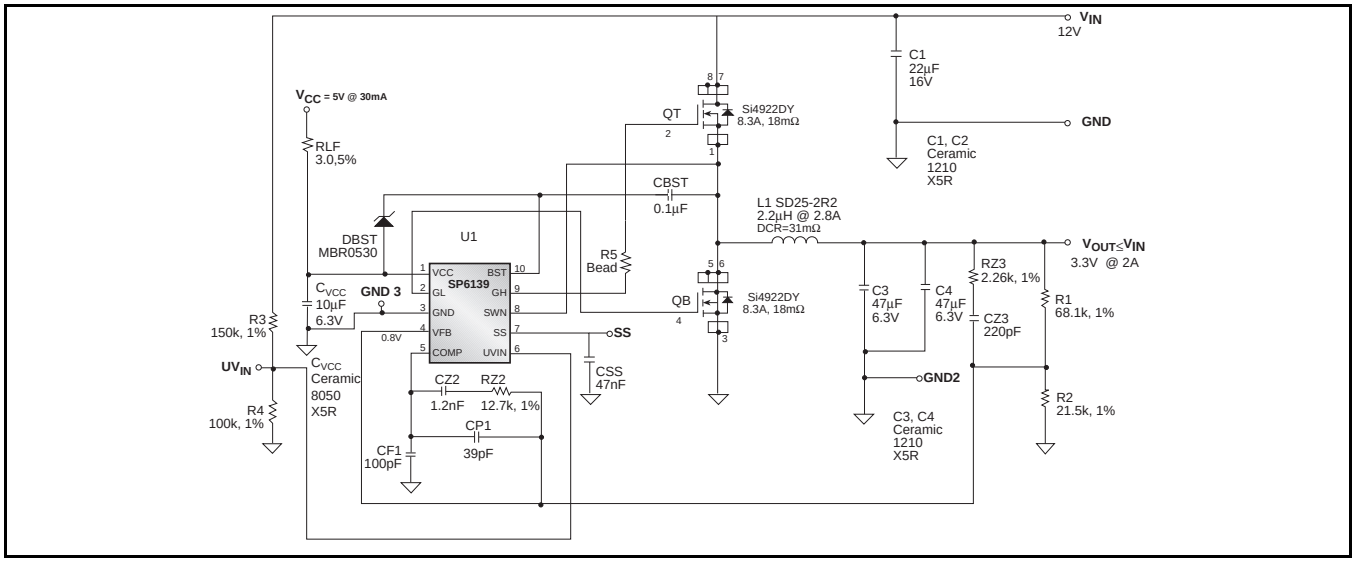


Fig. 1: SP6139 Application Diagram

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{cc} 7V
BST 27V
BST-SWN .....-0.3 to 7V
SWN .....-1V to 20V
GH..... -0.3V to BST+0.3V
GH-SWN..... 7V
All other pins ..... -0.3V to V_{CC}+0.3V

GH, GL peak output current <10us.....2A
Storage Temperature .....-65°C to 150°C
Power Dissipation.....Internally Limited
ESD Rating BST Pin (HBM - Human Body Model)..... 1.5kV
ESD Rating All Other Pins (HBM)..... 2kV
Thermal Resistance θ_{JA} .....41.9°C/W
Operating Voltage Range .....2.5V to 20V

ELECTRICAL SPECIFICATIONS

Specifications with standard type are for an Operating Junction Temperature of T_J = 25°C only; limits applying over the full Operating Junction Temperature range are denoted by a "•". Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise indicated, V_{cc} = 4.5V to 5.5V, BST= V_{cc}, SWN=GND=0V, UVIN=3V, CV_{cc} = 10µF, C_{COMP}=0.1uF, CGH=CGL=3.3nF, C_{SS}=50nF, T_A= –40°C to 85°C.

Parameter	Min.	Typ.	Max.	Units		Conditions
V_{CC} Supply Current		1.5	3	mA		VFB =0.9V (No switching)
BST Supply Current		0.2	0.4	mA	•	VFB =0.9V (No switching)
V_{CC} UVLO Start Threshold	4.00	4.25	4.50	V	•	
V_{CC} UVLO Hysteresis	100	200	300	mV		
UVIN Start Threshold	2.30	2.50	2.65	V	•	
UVIN Hysteresis	260	300	390	mV		
UVIN Input Current			1	uA		UVIN=3.0V
Error Amplifier Reference	0.792	0.800	0.808	V		2X Gain Config., Measure VFB, V_{CC}=5V, T=25°C
Error Amplifier Reference Over Line and Temperature	0.788	0.800	0.812	V	•	
Error Amplifier Transconductance		6		mS		
Error Amplifier Gain		60		dB		No Load
COMP Sink Current		150		uA		VFB=0.9V, COMP=0.9V
COMP Source Current		150		uA		VFB=0.7V, COMP=2.2V
VFB Input Bias Current		50	200	nA	•	VFB=0.8V
Internal Pole		4		MHz		
COMP Clamp		2.5		V		VFB=0.7V, TA = 25°C
COMP Clamp Temp. Coefficient		-2		mV/°C		
Ramp Amplitude	0.92	1.10	1.28	V	•	
RAMP Offset		1.1		V		TA = 25°C, RAMP COMP until GH starts switching
RAMP Offset Temp. Coefficient		-2		mV/°C		
GH Minimum Pulse Width		90	180	ns	•	
Maximum Controllable Duty Ratio	92	97		%	•	Maximum Duty Ratio Measured just before pulse skipping begins
Maximum Duty Ratio	100			%		Valid for 20 Cycles
Internal Oscillator Frequency	1.1	1.3	1.5	MHz	•	
SS Charge Current:		10		uA		

Parameter	Min.	Typ.	Max.	Units		Conditions
SS Discharge Current:	1			mA	•	Fault Present, SS = 0.2V
Short Circuit Threshold Voltage	0.20	0.25	0.30	V	•	Measured VREF (0.8V) - VFB
Hiccup Timeout		50		ms		VFB = 0.5V
Number of Allowable Clock Cycles at 100% Duty Cycle		20		Cycles		VFB = 0.7V
Minimum GL Pulse After 20 Cycles		0.5		Cycle		VFB = 0.7V
Thermal Shutdown Temperature		145		°C		
Thermal Hysteresis		10		°C		
GH & GL Rise Times		35	50	ns	•	Measured 10% to 90%
GH & GL Fall Times		30	40	ns	•	Measured 90% to 10%
GL to GH Non Overlap Time		45	70	ns	•	GH & GL Measured at 2.0V
SWN to GL Non Overlap Time		25	40	ns	•	Measured SWN = 100mV to GL = 2.0V
GH & GL Pull Down Resistance		50		Ω		
Driver Pull Down Resistance		1.5		Ω		
Driver Pull Up Resistance		2.5		Ω		

BLOCK DIAGRAM

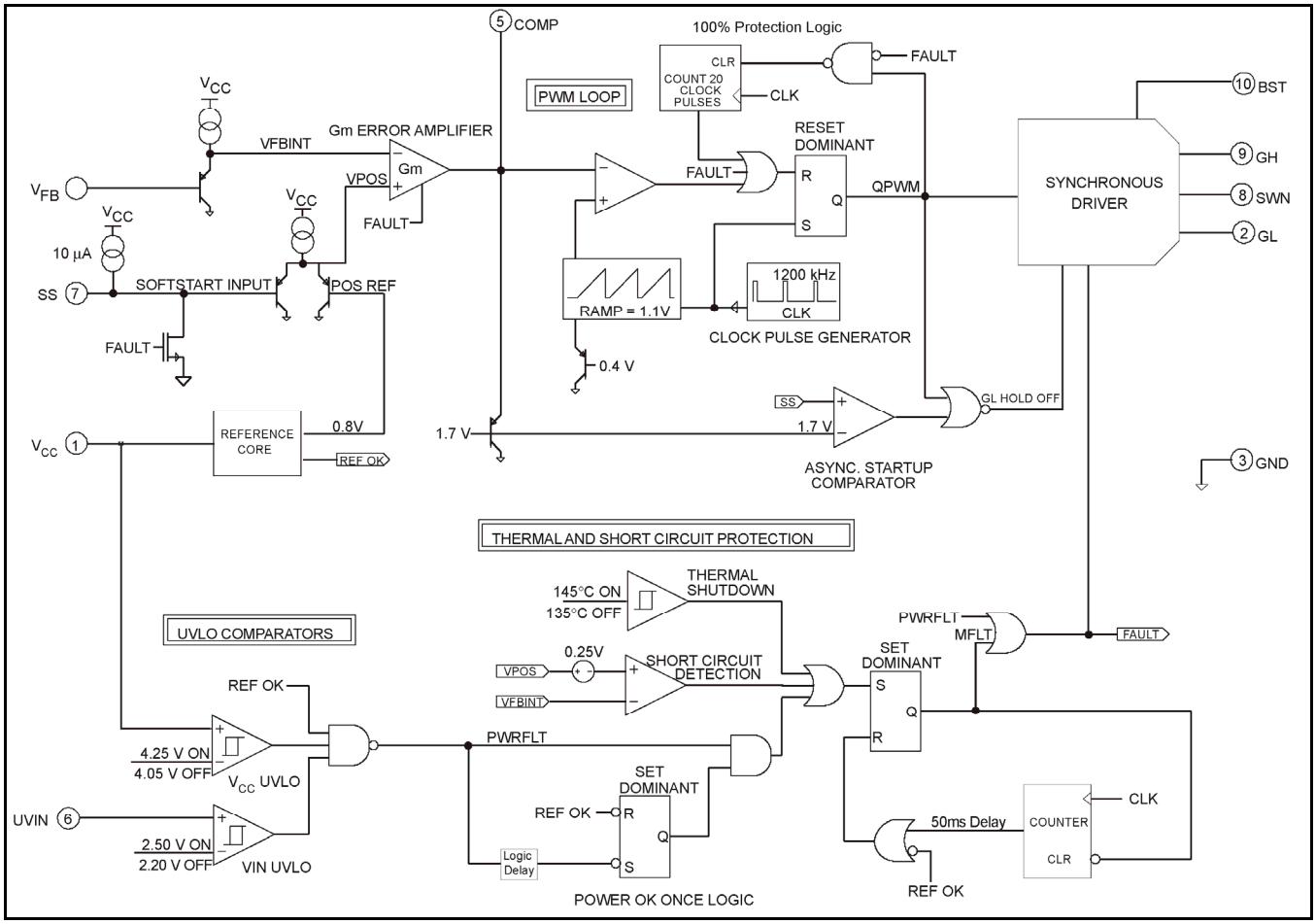


Fig. 2:SP6139 Block Diagram

PIN ASSIGNEMENT

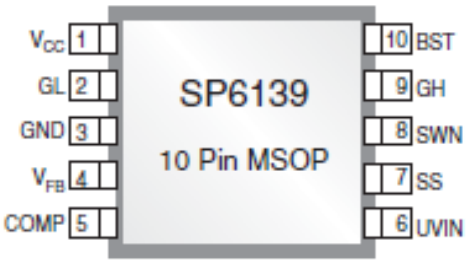


Fig. 3: SP6139 Pin Assignment

PIN DESCRIPTION

Name	Pin Number	Description
V_{CC}	1	Bias Supply Input. Connect to external 5V supply. Used to power internal circuits and low side gate driver.
GL	2	High current driver output for the low side NFET switch. It is always low if GH is high or during a fault. Resistor pull down ensure low state at low voltage.
GND	3	Ground Pin. The control circuitry of the IC and lower power driver are referenced to this pin. Return separately from other ground traces to the (-) terminal of COUT.
VFB	4	Feedback Voltage and Short Circuit Detection pin. It is the inverting input of the Error Amplifier and serves as the output voltage feedback point for the Buck Converter. The output voltage is sensed and can be adjusted through an external resistor divider. Whenever VFB drops 0.25V below the positive reference, a short circuit fault is detected and the IC enters hiccup mode.
COMP	5	Output of the Error Amplifier. It is internally connected to the inverting input of the PWM comparator. An optimal filter combination is chosen and connected to this pin and either ground or VFB to stabilize the voltage mode loop.
UVIN	6	UVLO input for VIN voltage. Connect a resistor divider between VIN and UVIN to set minimum operating voltage.
SS	7	Soft Start. Connect an external capacitor between SS and GND to set the soft start rate based on the 10µA source current. The SS pin is held low via a 1mA (min) current during all fault conditions.
SWN	8	Lower supply rail for the GH high-side gate driver. Connect this pin to the switching node at the junction between the two external power MOSFET transistors.
GH	9	High current driver output for the high side NFET switch. It is always low if GL is high or during a fault. Resistor pull down ensure low state at low voltage.
BST	10	High side driver supply pin. Connect BST to the external boost diode and capacitor as shown in the Typical Application Circuit on page 1. High side driver is connected between BST pin and SWN pin.

ORDERING INFORMATION

Part Number	Temperature Range	Marking	Package	Packing Quantity	Note 1	Note 2
SP6139EU-L	-40°C≤T_A≤+85°C	SP6139EU EXXX YWW	10 Pin MSOP	Bulk	Lead free	
SP6139EU-L/TR	-40°C≤T_A≤+85°C	SP6139EU EXXX YWW	10 Pin MSOP	Tape & Reel	Lead free	

"YY" = Year – "WW" = Work Week – "XXX" = Lot Number

THEORY OF OPERATION

GENERAL OVERVIEW

The SP6139 is a fixed frequency, voltage mode, synchronous PWM controller optimized for high efficiency. The part has been designed to be especially attractive for split plane applications utilizing 5V to power the controller and 3V to 15V for step down conversion. The heart of the SP6139 is a wide bandwidth transconductance amplifier designed to accommodate Type II and Type III compensation schemes. A precision 0.8V reference present on the positive terminal of the error amplifier permits the programming of the output voltage down to 0.8V via the VFB pin. The output of the error amplifier, COMP, compared to a 1.1V peak-to-peak ramp is responsible for trailing edge PWM control. This voltage ramp and PWM control logic are governed by the internal oscillator that accurately sets the PWM frequency to 300kHz. The SP6139 contains two unique control features that are very powerful in distributed applications. First, Non-synchronous driver control is enabled during start up to prohibit the low side NFET from pulling down the output until the high side NFET has attempted to turn on. Second, a 100% duty cycle timeout ensures that the low side NFET is periodically enhanced during extended periods at 100% duty cycle. This guarantees the synchronized refreshing of the BST capacitor during very large duty ratios. The SP6139 also contains a number of valuable protection features. A programmable input (VIN) UVLO allows a user to set the exact value at which the conversion voltage is at a safe point to begin down conversion, and an internal VCC UVLO ensures that the controller itself has enough voltage to properly operate. Other protection features include thermal shutdown and short-circuit detection. In the event that either a thermal, short-circuit, or UVLO fault is detected, the SP6139 is forced into an idle state where the output drivers are held off for a finite period before a re-start is attempted.

SOFT START

"Soft Start" is achieved when a power converter ramps up the output voltage while controlling the magnitude of the input supply source current. In a modern step down converter, ramping up the positive terminal of the error amplifier controls soft start. As a result, excess source current can be defined as the current required to charge the output capacitor.

$$IV_{IN} = C_{OUT} * DV_{OUT} / DTSoft\text{-}start$$

The SP6139 provides the user with the option to program the soft start rate by tying a capacitor from the SS pin to GND. The selection of this capacitor is based on the 10uA pull up current present at the SS pin and the 0.8V reference voltage. Therefore, the excess source can be redefined as:

$$IV_{IN} = C_{OUT} * DV_{OUT} * 10\mu A / (C_{SS} * 0.8V)$$

UNDER VOLTAGE LOCK OUT (UVLO)

The SP6139 contains two separate UVLO comparators to monitor the bias (VCC) and conversion (VIN) voltages independently. The VCC UVLO threshold is internally set to 4.25V, whereas the VIN UVLO threshold is programmable through the UVIN pin. When the UVIN pin is greater than 2.5V, the SP6139 is permitted to start up pending the removal of all other faults. Both the VCC and VIN UVLO comparators have been designed with hysteresis to prevent noise from resetting a fault.

THERMAL AND SHORT-CIRCUIT PROTECTION

Because the SP6139 is designed to drive large NFETs running at high current, there is a chance that either the controller or power converter will become too hot. Therefore, an internal thermal shutdown (145°C) has been included to prevent the IC from malfunctioning at extreme temperatures.

A short-circuit detection comparator has also been included in the SP6139 to protect against the accidental short or sever build up of current at the output of the power converter. This comparator constantly monitors the

positive and negative terminals of the error amplifier, and if the VFB pin ever falls more than 250mV (typical) below the positive reference, a short-circuit fault is set. Because the SS pin overrides the internal 0.8V reference during soft start, the SP6139 is capable of detecting short-circuit faults throughout the duration of soft start as well as in regular operation.

HANDLING OF FAULTS

Upon the detection of power (UVLO), thermal, or short-circuit faults, the SP6139 is forced into an idle state where the SS and COMP pins are pulled low and the gate drivers are held off. In the event of UVLO fault, the SP6139 remains in this idle state until the UVLO fault is removed. Upon the detection of a thermal or short-circuit fault, an internal 200ms (typical) timer is activated. In the event of a short-circuit fault, a restart is attempted immediately after the 200ms timeout expires. Whereas, when a thermal fault is detected the 200ms delay continuously recycles and a restart cannot be attempted until the thermal fault is removed and the timer expires.

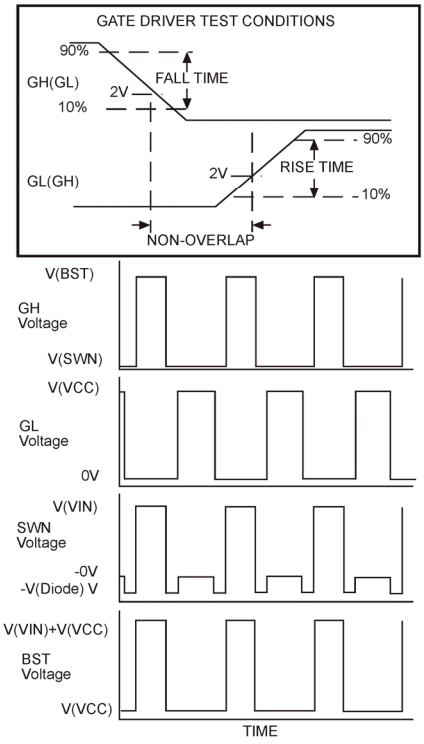
ERROR AMPLIFIER AND VOLTAGE LOOP

As stated before, the heart of the SP6139 voltage error loop is a high performance, wide bandwidth transconductance amplifier. Because of the amplifier's current limited (±150µA) transconductance, there are many ways to compensate the voltage loop or to control the COMP pin externally. A simple, single pole, single zero compensation can be a RC to ground. However Exar recommends a Type II or Type III compensation which eliminates the g_m of the amplifier from the control loop equations. The amplifier has enough bandwidth (45° at 4 MHz) and enough gain (60dB) to run Type III compensation schemes with adequate gain and phase margins at cross over frequencies greater than 50kHz.

The common mode output of the error amplifier is 0.9V to 2.2V. Therefore, the PWM voltage ramp has been set between 1.1V and 2.2V to ensure proper 0% to 100% duty cycle capability. The voltage loop also includes two other very important features. One is an Non-synchronous start up mode. Basically, the GL driver can not turn on unless the GH driver has attempted to turn on or the SS pin has exceeded 1.7V. This feature prevents the controller from "dragging down" the output voltage during startup or in fault modes. The second feature is a 100% duty cycle timeout that ensures synchronized refreshing of the BST capacitor at very high duty ratios. In the event that the GH driver is on for 20 continuous clock cycles, a reset is given to the PWM flip flop half way through the 21st cycle. This forces GL to rise for the remainder of the cycle, in turn refreshing the BST capacitor.

GATE DRIVERS

The SP6139 contains a pair of powerful 2Ω SOURCE and 1.5Ω SINK drivers. These state of the art drivers are designed to drive external NFETs capable of handling up to 30A. Rise, fall, and non-overlap times have all been minimized to achieve maximum efficiency. All drive pins GH, GL & SWN are monitored continuously to ensure that only one external NFET is ever on at any given time.



APPLICATIONS INFORMATION

INDUCTOR SELECTION

There are many factors to consider in selecting the inductor including cost, efficiency, size and EMI. In a typical SP6139 circuit, the inductor is chosen primarily for value, saturation current and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response. Low inductor values provide the smallest size, but cause large ripple currents, poor efficiency and more output capacitance to smooth out the larger ripple current. The inductor must also be able to handle the peak current at the switching frequency without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss. A good compromise between size, loss and cost is to set the inductor ripple current to be within 20% to 40% of the maximum output current.

The switching frequency and the inductor operating point determine the inductor value as follows:

$$L = \frac{V_{OUT}\left(V_{IN(\max)} - V_{OUT}\right)}{V_{IN(\max)} F_S K_r I_{OUT(\max)}}$$

where:

Fs = switching frequency Kr = ratio of the ac inductor ripple current to the maximum output current

The peak to peak inductor ripple current is:

$$L = \frac{V_{OUT}\left(V_{IN(\max)} - V_{OUT}\right)}{V_{IN(\max)} F_S L}$$

$$I_{PEAK} = I_{OUT(\max)} + \frac{I_{PP}}{2}$$

Once the required inductor value is selected, the proper selection of core material is based on peak inductor current and efficiency requirements. The core must be large enough not to saturate at the peak inductor current and provide low core loss at the high switching frequency. Low cost powdered iron cores have a gradual saturation characteristic but can introduce considerable ac core loss, especially when the inductor value is relatively low and the ripple current is high. Ferrite materials, on the other hand, are more expensive and have an abrupt saturation characteristic with the inductance dropping sharply when the peak design current is exceeded. Nevertheless, they are preferred at high switching frequencies because they present very low core loss and the design only needs to prevent saturation. In general, ferrite or molypermalloy materials are better choice for all but the most cost sensitive applications. The power dissipated in the inductor is equal to the sum of the core and copper losses. To minimize copper losses, the winding resistance needs to be minimized, but this usually comes at the expense of a larger inductor. Core losses have a more significant contribution at low output current where the copper losses are at a minimum, and can typically be neglected at higher output currents where the copper losses dominate. Core loss information is usually available from the magnetic vendor.

The copper loss in the inductor can be calculated using the following equation:

$$P_{L(Cu)} = I^2{}_{L(RMS)} R_{WINDING}$$

where IL(RMS) is the RMS inductor current that can be calculated as follows:

$$I_{L(RMS)} - I_{OUT(\max)} \sqrt{1 + \frac{1}{3}\left(\frac{I_{PP}}{I_{OUT(\max)}}\right)^2}$$

OUTPUT CAPACITOR SELECTION

The required ESR (Equivalent Series Resistance) and capacitance drive the selection of the type and quantity of the output capacitors. The ESR must be small enough that both the resistive voltage deviation due to a step change in the load current and the output ripple voltage do not

exceed the tolerance limits expected on the output voltage. During an output load transient, the output capacitor must supply all the additional current demanded by the load until the SP6139CU adjusts the inductor current to the new value.

Therefore the capacitance must be large enough so that the output voltage is help up while the inductor current ramps up or down to the value corresponding to the new load current. Additionally, the ESR in the output capacitor causes a step in the output voltage equal to the current. Because of the fast transient response and inherent 100% and 0% duty cycle capability provided by the SP6139CU when exposed to output load transient, the output capacitor is typically chosen for ESR, not for capacitance value.

The output capacitor's ESR, combined with the inductor ripple current, is typically the main contributor to output voltage ripple. The maximum allowable ESR required to maintain a specified output voltage ripple can be calculated by:

$$R_{ESR} \le \frac{\Delta V_{OUT}}{I_{PP}}$$

ΔV_{OUT} = Peak to Peak Output Voltage Ripple

I_{PP} = Peak to Peak Inductor Ripple Current

The total output ripple is a combination of the ESR and the output capacitance value and can be calculated as follows:

$$\Delta V_{OUT} = \sqrt{\left(\frac{I_{PP}(1-D)}{C_{OUT}F_S}\right)^2 + (I_{PP}R_{ESR})^2}$$

Where:

FS = Switching Frequency

D = Duty Cycle

C_{OUT} = Output Capacitance Value

INPUT CAPACITOR SELECTION

The input capacitor should be selected for ripple current rating, capacitance and voltage rating. The input capacitor must meet the ripple current requirement imposed by the switching current. In continuous conduction mode, the source current of the high-side MOSFET is approximately a square wave of duty cycle VOUT/VIN. Most of this current is supplied by the input bypass capacitors. The RMS value of input capacitor current is determined at the maximum output current and under the assumption that the peak to peak inductor ripple current is low, it is given by:

$$I_{CIN(rms)} = I_{OUT(\max)}\sqrt{D(1-D)}$$

The worse case occurs when the duty cycle D is 50% and gives an RMS current value equal to $I_{OUT}/2$.

Select input capacitors with adequate ripple current rating to ensure reliable operation. The power dissipated in the input capacitor is:

$$P_{CIN} = I^2_{CIN(rms)}R_{ESR(CIN)}$$

This can become a significant part of power losses in a converter and hurt the overall energy transfer efficiency. The input voltage ripple primarily depends on the input capacitor ESR and capacitance. Ignoring the inductor ripple current, the input voltage ripple can be determined by:

$$\Delta V_{IN} = I_{OUT(\max)}R_{ESR(CIN)} + \frac{I_{OUT(\max)}V_{OUT}(V_{IN}-V_{OUT})}{F_S C_{IN} V_{IN}^2}$$

The capacitor type suitable for the output capacitors can also be used for the input capacitors. However, exercise extra caution when tantalum capacitors are considered. Tantalum capacitors are known for catastrophic failure when exposed to surge current, and input capacitors are prone to such surge current when power supplies are connected "live" to low impedance power sources.

MOSFET SELECTION

The losses associated with MOSFETs can be divided into conduction and switching losses. Conduction losses are related to the on resistance of MOSFETs, and increase with the load current. Switching losses occur on each on/off transition when the MOSFETs experience both high current and voltage. Since the bottom MOSFET switches current from/to a paralleled diode (either its own body diode or a Schottky diode), the voltage across the MOSFET is no more than 1V during switching transition. As a result, its switching losses are negligible. The switching losses are difficult to quantify due to all the variables affecting turn on/ off time. However, the following equation provides an approximation on the switching losses associated with the top MOSFET driven by SP6139.

$$P_{SH(\max)} = 12 C_{rss} V_{IN(\max)} I_{OUT(\max)} F_S$$

where

Crss = reverse transfer capacitance of the top MOSFET

Switching losses need to be taken into account for high switching frequency, since they are directly proportional to switching frequency. The conduction losses associated with top and bottom MOSFETs are determined by:

$$P_{CH(\max)} = R_{DS(ON)} I_{OUT(\max)}{}^2 D$$

$$P_{CL(\max)} = R_{DS(ON)} I_{OUT(\max)}{}^2 (1 - D)$$

where

PCH(max) = conduction losses of the high side MOSFET

PCL(max) = conduction losses of the low side MOSFET

RDS(ON) = drain to source on resistance.

The total power losses of the top MOSFET are the sum of switching and conduction losses. For synchronous buck converters of efficiency over 90%, allow no more than 4% power losses for high or low side MOSFETs. For input voltages of 3.3V and 5V, conduction losses often dominate switching losses. Therefore, lowering the RDS(ON) of the MOSFETs always improves efficiency even though it gives rise to higher switching losses due to increased Crss.

Top and bottom MOSFETs experience unequal conduction losses if their on time is unequal. For applications running at large or small duty cycle, it makes sense to use different top and bottom MOSFETs. Alternatively, parallel multiple MOSFETs to conduct large duty factor.

RDS(ON) varies greatly with the gate driver voltage. The MOSFET vendors often specify RDS(ON) on multiple gate to source voltages (VGS), as well as provide typical curve of RDS(ON) versus VGS. For 5V input, use the RDS(ON) specified at 4.5V VGS. At the time of this publication, vendors, such as Fairchild, Siliconix and International Rectifier, have started to specify RDS(ON) at VGS less than 3V. This has provided necessary data for designs in which these MOSFETs are driven with 3.3V and made it possible to use SP6139 in 3.3V only applications.

Thermal calculation must be conducted to ensure the MOSFET can handle the maximum load current. The junction temperature of the MOSFET, determined as follows, must stay below the maximum rating.

$$T_{J(\max)} = T_{A(\max)} + \frac{P_{MOSFET(\max)}}{R_{\theta JA}}$$

where

TA(max) = maximum ambient temperature

PMOSFET(max) = maximum power dissipation of the MOSFET

RΘJA = junction to ambient thermal resistance.

RΘJA of the device depends greatly on the board layout, as well as device package. Significant thermal improvement can be achieved in the maximum power dissipation through the proper design of copper mounting pads on the circuit board. For example, in a SO-8 package, placing two 0.04 square inches

copper pad directly under the package, without occupying additional board space, can increase the maximum power from approximately 1 to 1.2W. For DPAK package, enlarging the tap mounting pad to 1 square inches reduces the RΘJA from 96°C/W to 40°C/W.

SCHOTTKY DIODE SELECTION

When paralleled with the bottom MOSFET, an optional Schottky diode can improve efficiency and reduce noises. Without this Schottky diode, the body diode of the bottom MOSFET conducts the current during the non-overlap time when both MOSFETs are turned off. Unfortunately, the body diode has high forward voltage and reverse recovery problem. The reverse recovery of the body diode causes additional switching noises when the diode turns off. The Schottky diode alleviates these noises and additionally improves efficiency thanks to its low forward voltage. The reverse voltage across the diode is equal to input voltage, and the diode must be able to handle the peak current equal to the maximum load current.

The power dissipation of the Schottky diode is determined by

$$P_{Diode} = 2V_F I_{OUT} T_{NOL} F_S$$

where

TNOL = non-overlap time between GH and GL.

VF = forward voltage of the Schottky diode.

LOOP COMPENSATION DESIGN

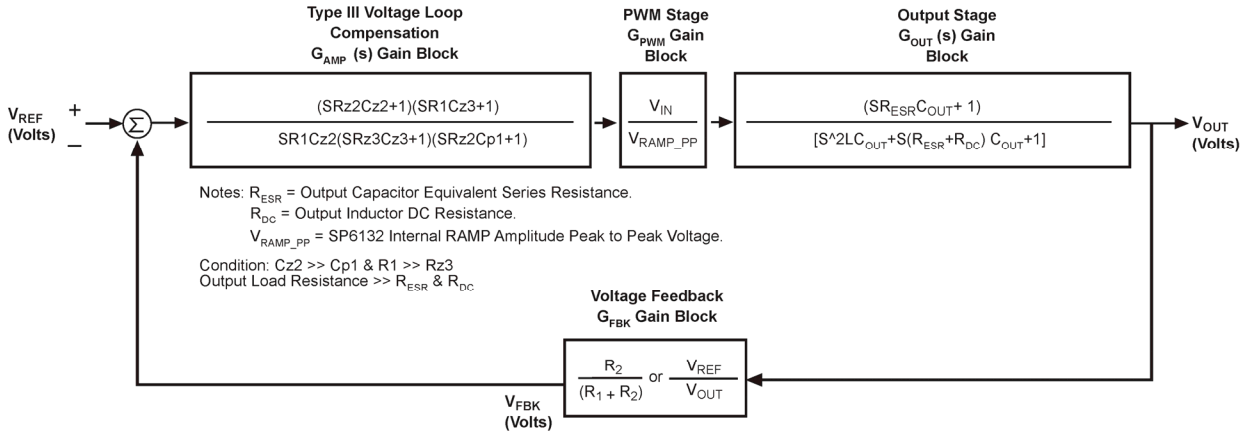
The open loop gain of the whole system can be divided into the gain of the error amplifier, PWM modulator, buck converter output stage, and feedback resistor divider. In order to crossover at the selected frequency FCO, the gain of the error amplifier has to compensate for the attenuation caused by the rest of the loop at this frequency. The goal of loop compensation is to manipulate loop frequency response such that its gain crosses over 0db at a slope of -20db/dec. The first step of compensation design is to pick the loop crossover frequency. High crossover frequency is desirable for fast transient response, but often jeopardizes the system stability. Crossover frequency should be higher than the ESR zero but less than 1/5 of the switching frequency. The ESR zero is contributed by the ESR associated with the output capacitors and can be determined by:

$$f_{Z(ESR)} = \frac{1}{2\pi C_{OUT} R_{ESR}}$$

The next step is to calculated the complex conjugate poles contributed by the LC output filter,

$$f_{P(LC)} = \frac{1}{2\pi\sqrt{LC}}$$

When the output capacitors are of a Ceramic Type, the SP6139CU Evaluation Board requires a Type III compensation circuit to give a phase boost of 180° in order to counteract the effects of an under damped resonance of the output filter at the double pole frequency.



SP6139 Voltage Mode Control Loop with Loop Dynamic

Definitions:

Resr = Output Capacitor Equivalent Series Resistance

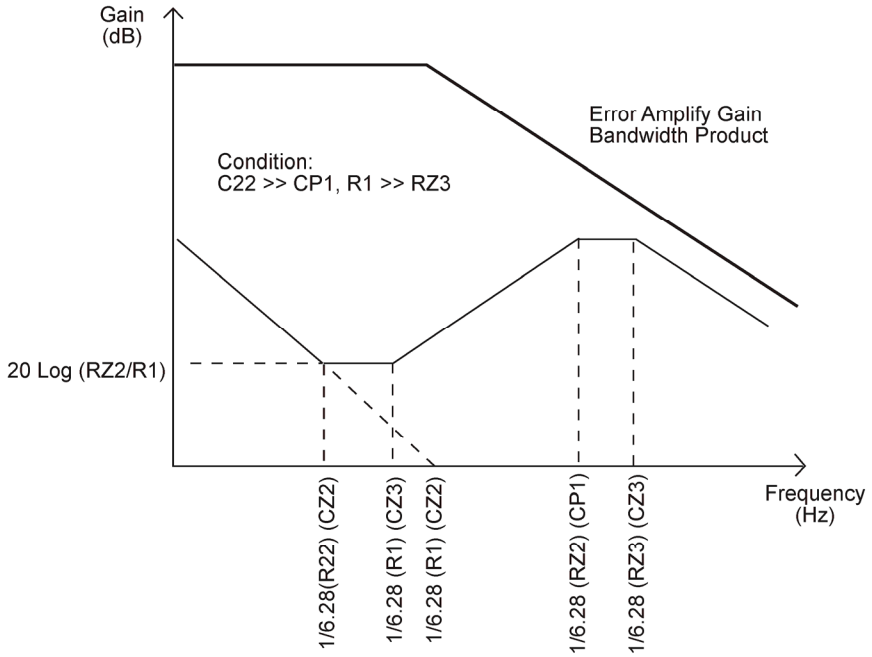
Rdc = Output Inductor DC Resistance

Vramp_pp = SP6139 internal RAMP Amplitude Peak to Peak Voltage

Conditions:

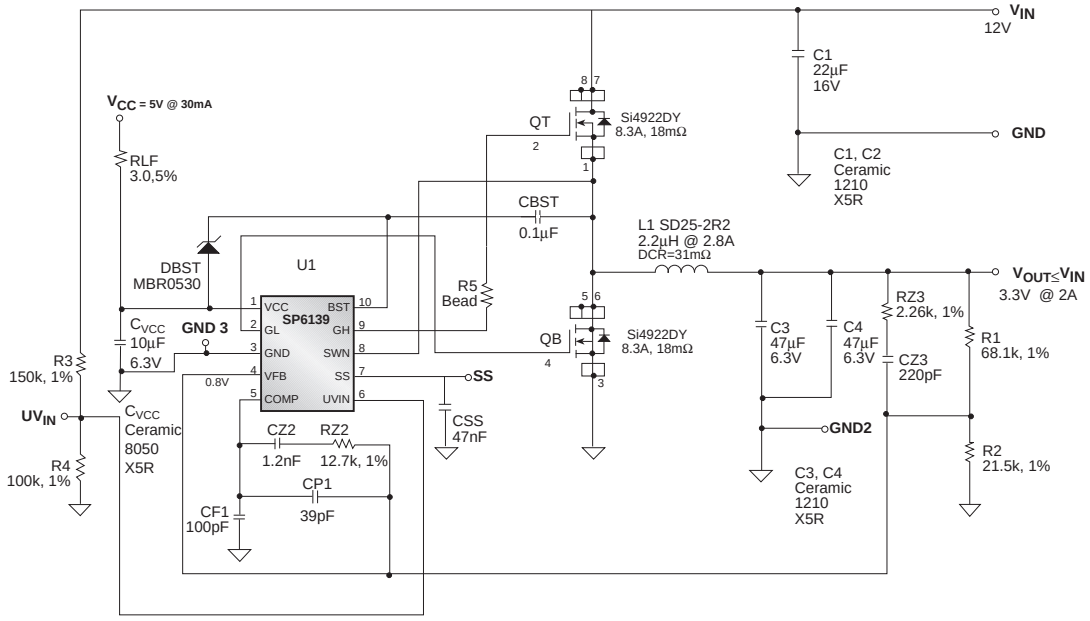
Cz2 >> Cp1 and R1 >> Rz3

Output Load Resistance >> Resr and Rdc



Bode Plot of Type III Error Amplifier Compensation.

TYPICAL APPLICATION DIAGRAM



INDUCTORS - SURFACE MOUNT							
Inductor Specification							
Inductance (uH)	Manufacturer/Part No.	Series R mΩ	I_{SAT} (a)	Size LxW(mm)	Size Ht.(mm)	Inductor Type	Manufacturer Website
2.7	**Easy Magnet SC5018-2R7M**	**4.30**	**12.0**	**12.6x12.6**	**4.5**	**Shielded Ferrite Core**	inter-technical.com
2.7	TDK RLF 12560T-2R7N110	4.50	12.2	12.5x12.8	6.0	Shielded Ferrite Core	tdk.com
3.3	Coilcraft DO5010P-332HC	8.60	17.0	14.7x15.2	8.0	Unshielded Ferrite Core	coilcraft.com
1.2	Easy Magnet SC5018-1R2M	1.96	20.0	12.6x12.6	4.5	Shielded Ferrite Core	inter-technical.com
1.2	Inter-Technical SC4015-1R2M	4.37	17.0	10.0x10.0	3.8	Shielded Ferrite Core	inter-technical.com
1.5	Coilcraft DO5010P-152HC	4.00	25.0	14.7x15.2	8.0	Unshielded Ferrite Core	coilcraft.com
1.9	TDK RLF 12560T-1R9N120	3.60	13.2	12.5x12.8	6.0	Shielded Ferrite Core	tdk.com

CAPACITORS -SURFACE MOUNT								
Capacitance (uF)	Manufacturer/Part No.	ESR Ω (max)	Ripple Current (A)@45°C	Size LxW(mm)	Size Ht.(mm)	Voltage (V)	Capacitor Type	Manufacturer Website
22	**TDK C3225X5R1C226M**	**0.002**	**4.00**	**3.2x2.5**	**2.0**	**16.0**	**X5R Ceramic**	tdk.com
47	**TDK C3225X5ROJ476M**	**0.002**	**4.00**	**3.2x2.5**	**2.5**	**6.3**	**X5R Ceramic**	tdk.com

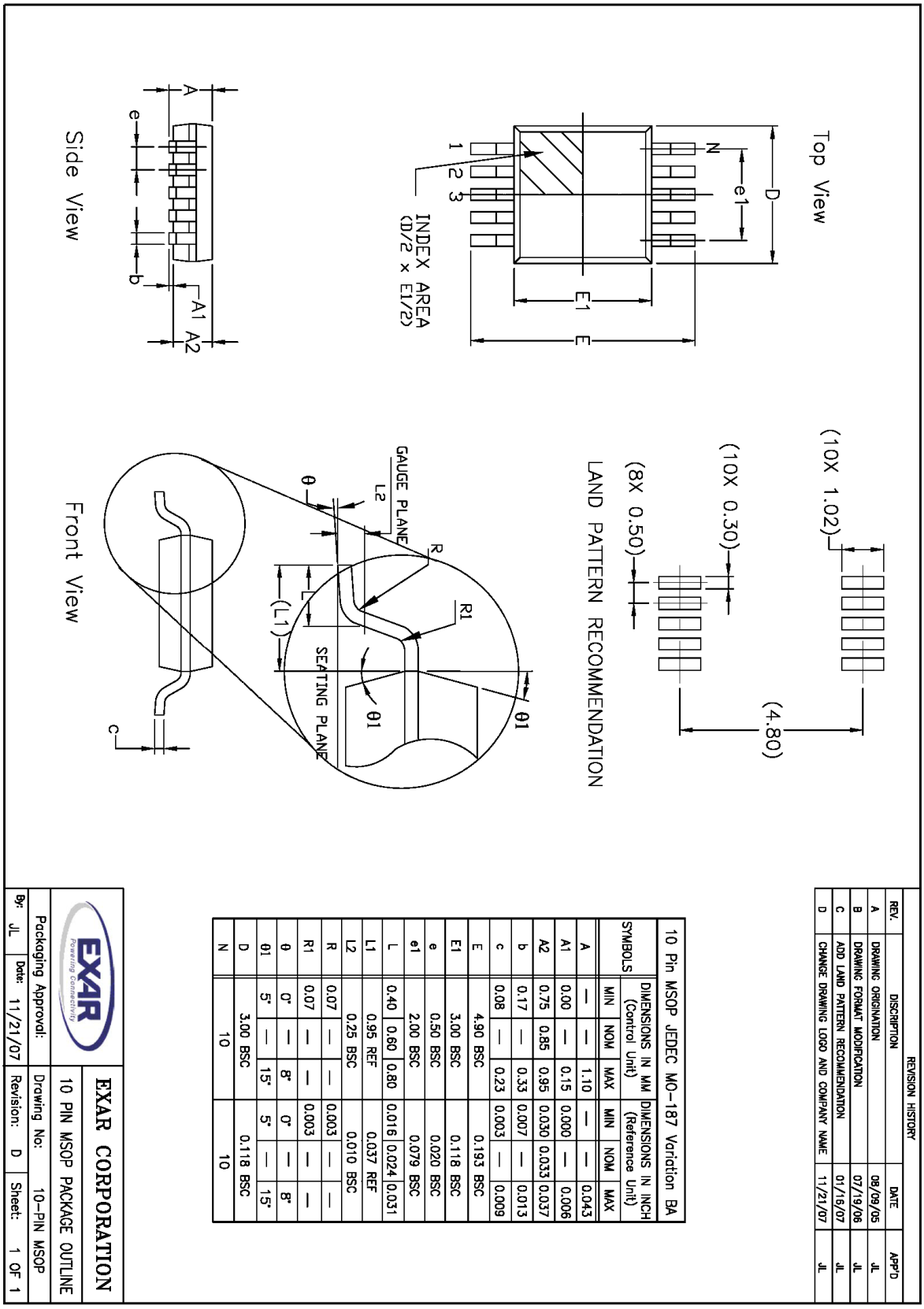
MOSFET - Surface Mount								
MOSFET	Manufacturer/Part No.	RDS (on) Ω (max)	ID Current (A)	Qg nC(Typ)	Qg nC(Max)	Voltage (V)	Foot Print	Manufacturer Website
N-Channel	**Fairchild Semi FDS6676S**	**0.006**	**14.50**	**43**	**60.0**	**30.0**	SO-8	fairchildsemi.com
N-Channel	Fairchild Semi FD7088N3	0.005	21.10	37	48.0	30.0	SO-8	fairchildsemi.com
N-Channel	Vishay Si4336DY	0.004	25.0	32	50.0	30.0	SO-8	vishay.com

Note: Components highlighted in bold are those used on the SP6139 Evaluation Board.

Table 1. Input and Output Stage Components Selection Charts.

PACKAGE SPECIFICATION

MSOP-10



REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	08/09/05	JL
B	DRAWING FORMAT MODIFICATION	07/19/06	JL
C	ADD LAND PATTERN RECOMMENDATION	01/16/07	JL
D	CHANGE DRAWING LOGO AND COMPANY NAME	11/21/07	JL

10 Pin MSOP JEDEC MO-187 Variation BA

SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.10	—	—	0.043
A1	0.00	—	0.15	0.000	—	0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.17	—	0.33	0.007	—	0.013
c	0.08	—	0.23	0.003	—	0.009
E	4.90 BSC			0.193 BSC		
E1	3.00 BSC			0.118 BSC		
e	0.50 BSC			0.020 BSC		
e1	2.00 BSC			0.079 BSC		
L	0.40	0.60	0.80	0.016	0.024	0.031
L1	0.95 REF			0.037 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	8°	15°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
D	3.00 BSC			0.118 BSC		
N	10			10		

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10 PIN MSOP PACKAGE OUTLINE

Packaging Approval:	Drawing No:	10-PIN MSOP
By: JL Date: 11/21/07	Revision: D	Sheet: 1 OF 1

REVISION HISTORY – TO BE DELETED PRIOR TO PUBLICATION -

Revision	Date	Description
0.1		Initial Data Sheet
1.0		Approved and first release of data sheet
1.1 Shahin	12/16/2008	Converted datasheet to new format ESD rating: 1.5kV BST pin, 2kV all other pins In Electrical Specifications changed Temperature range to -40C to +85C Added VCC supply current Max spec Removed VCC UVLO Stop Threshold Removed UVIN Stop Threshold UVIN Hysteresis changed to 260mV Typ, 390mV Max Removed thermal recovery temp Added driver pull-up and pull-down resistance specs
1.2 Jon	1/13/2009	Added operating input voltage range Changed wording regarding type II/III compensation and gm of amp Changed "12" to operating voltage range at start of applications section Updated block diagram Changed Asynchronous to non-synchronous throughout
2.0	1/15/2009	Released Datasheet

FOR FURTHER ASSISTANCE

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EXAR CORPORATION

HEADQUARTERS AND SALES OFFICES

48720 Kato Road

Fremont, CA 94538 – USA

Tel.: +1 (510) 668-7000

Fax: +1 (510) 668-7030

www.exar.com

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