8 Pin SIL 5 Tap TTL Compatible Active Delay Lines

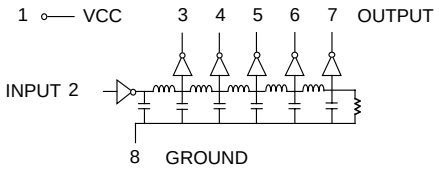
TAP DELAYS ±5% or ±2 nS†	TOTAL DELAYS ±5% or ±2 nS†	Part Number Pkg. A	Part Number Pkg. B	TAP DELAYS ±5% or ±2 nS†	TOTAL DELAYS ±5% or ±2 nS†	Part Number Pkg. A	Part Number Pkg. B
1.0 ± 0.5	*4 ± 0.5	EP9677-4	EP9733-4	15	75	EP9677-75	EP9733-75
1.5 ± 0.5	*6 ± 0.5	EP9677-6	EP9733-6	20	100	EP9677-100	EP9733-100
2.0 ± 1	*8 ± 1.0	EP9677-8	EP9733-8	25	125	EP9677-125	EP9733-125
2.5 ± 1	*10	EP9677-10	EP9733-10	30	150	EP9677-150	EP9733-150
3.0 ± 1	*12	EP9677-12	EP9733-12	35	175	EP9677-175	EP9733-175
4.0 ± 1.5	*16	EP9677-16	EP9733-16	40	200	EP9677-200	EP9733-200
5.0	*20	EP9677-20	EP9733-20	50	250	EP9677-250	EP9733-250
6.0	30	EP9677-30	EP9733-30	60	300	EP9677-300	EP9733-300
7.0	35	EP9677-35	EP9733-35	70	350	EP9677-350	EP9733-350
8.0	40	EP9677-40	EP9733-40	80	400	EP9677-400	EP9733-400
9.0	45	EP9677-45	EP9733-45	90	450	EP9677-450	EP9733-450
10.0	50	EP9677-50	EP9733-50	100	500	EP9677-500	EP9733-500
12.0	60	EP9677-60	EP9733-60				

†Whichever is greater. Delay times referenced from input to leading edges at 25°C, 5.0V, with no load.
**Delay times referenced from 1st tap*
1st tap is the inherent delay: approx. 7 nS

DC Electrical Characteristics

	Parameter	Test Conditions	Min	Max	Unit
V_{OH}	High-Level Output Voltage	V_{CC} = min. V_{IL} = max. I_{OH} = max	2.7		V
V_{OL}	Low-Level Output Voltage	V_{CC} = min. V_{IH} = min. I_{OL} = max		0.5	V
V_{IK}	Input Clamp Voltage	V_{CC} = min. I_I = II_K		-1.2V	V
I_{IH}	High-Level Input Current	V_{CC} = max. V_{IN} = 2.7V		50	µA
		V_{CC} = max. V_{IN} = 5.25V		1.0	mA
I_{IL}	Low-Level Input Current	V_{CC} = max. V_{IN} = 0.5V		-2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = max. V_{OUT} = 0. (One output at a time)	-40	-100	mA
I_{CCH}	High-Level Supply Current	V_{CC} = max. V_{IN} = OPEN		115	mA
I_{CCL}	Low-Level Supply Current	V_{CC} = max. V_{IN} = 0		115	mA
T_{RO}	Output Rise Time	Td ≤ 500 nS (0.75 to 2.4 Volts)		4	nS
N_H	Fanout High-Level Output	V_{CC} = max. V_{OH} = 2.7V		20 TTL LOAD	
N_L	Fanout Low-Level Output	V_{CC} = max. V_{OL} = 0.5V		10 TTL LOAD	

Schematic



Recommended Operating Conditions

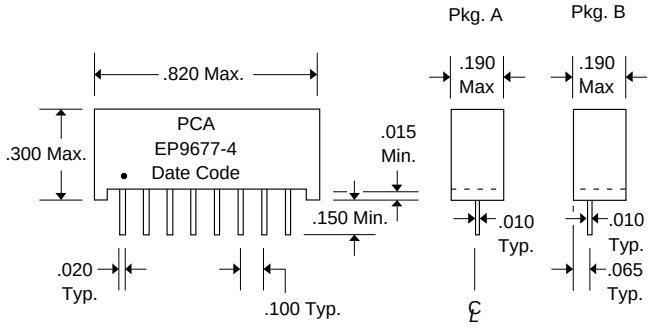
		Min	Max	Unit
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IH}	High-Level Input Voltage	2.0		V
V_{IL}	Low-Level Input Voltage		0.8	V
I_{IK}	Input Clamp Current		-18	mA
I_{OH}	High-Level Output Current		-1.0	mA
I_{OL}	Low-Level Output Current		20	mA
P_W*	Pulse Width of Total Delay	40		%
d*	Duty Cycle		40	%
T_A	Operating Free-Air Temperature	0	+70	°C

**These two values are inter-dependent.*

Input Pulse Test Conditions @ 25° C

			Unit
E_{IN}	Pulse Input Voltage	3.2	Volts
P_W	Pulse Width % of Total Delay	110	%
T_{RI}	Pulse Rise Time (0.75 - 2.4 Volts)	2.0	nS
P_{RR}	Pulse Repetition Rate @ Td ≤ 200 nS	1.0	MHz
	Pulse Repetition Rate @ Td > 200 nS	100	KHz
V_{CC}	Supply Voltage	5.0	Volts

Package Dimensions



DSD9677 Rev. A 2/5/96

QAF-CSO1 Rev. B 8/25/94

Unless Otherwise Noted Dimensions in Inches
Tolerances:
Fractional = ± 1/32
.XX = ± .030 .XXX = ± .010

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