TriQuint SEMICONDUCTOR

AGR18030EF
30 W, 1.805 GHz—1.880 GHz, LDMOS RF Power Transistor

Introduction

The AGR18030EF is a high-voltage, gold-metallized, laterally diffused metal oxide semiconductor (LDMOS) RF power field effect transistor (FET) suitable for global system for mobile communication (GSM), enhanced data for global evolution (EDGE), and multicarrier class AB power amplifier applications. This device is manufactured using advanced LDMOS technology offering state-of-the-art performance and reliability. It is packaged in an industry-standard package and is capable of delivering a minimum output power of 30 W, which makes it ideally suited for today's RF power amplifier applications.

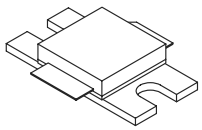


Figure 1. Available (flanged) Packages

Features

Typical performance ratings for GSM EDGE (f = 1.840 GHz, P_{OUT} = 10 W)
- — Error vector magnitude (EVM): 1.6%
- — Power gain: 15 dB
- — Drain efficiency: 30%
- — Modulation spectrum:
  - @ ±400 kHz = –64 dBc.
  - @ ±600 kHz = –71 dBc.

Typical continuous wave (CW) performance over entire digital communication system (DCS) band:
- — P1dB: 33 W typical (typ).
- — Power gain: @ P1dB = 14 dB.
- — Efficiency: @ P1dB = 51% typ.
- — Return loss: –12 dB.

High-reliability, gold-metallization process.

Low hot carrier injection (HCI) induced bias drift over 20 years.

Internally matched.

High gain, efficiency, and linearity.

Integrated ESD protection.

30 W minimum output power.

Device can withstand 10:1 voltage standing wave ratio (VSWR) at 26 Vdc, 1.840 GHz, 30 W CW output power.

Large signal impedance parameters available.

Table 1. Thermal Characteristics

Parameter	Sym	Value	Unit
Thermal Resistance, Junction to Case	$R_{I\ JC}$	2.0	°C/W

Table 2. Absolute Maximum Ratings*

Parameter	Sym	Value	Unit
Drain-source Voltage	V_{DSS}	65	Vdc
Gate-source Voltage	V_{GS}	–0.5, 15	Vdc
Drain Current Continuous	I_D		Adc
Total Dissipation at T_C = 25 °C	P_D	87.5	W
Derate Above 25 °C	—	0.5	W/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{STG}	–65, 150	°C

* Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 3. ESD Rating*

AGR18030EF	Minimum (V)	Class
HBM	500	1B
MM	50	A
CDM	1500	4

* Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD and electrical overstress (EOS) during all handling, assembly, and test operations. PEAK Devices employs a human-body model (HBM), a machine model (MM), and a charged-device model (CDM) qualification requirement in order to determine ESD-susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114B (HBM), JESD22-A115A (MM), and JESD22-C101A (CDM) standards.

Caution: MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Electrical Characteristics

Recommended operating conditions apply unless otherwise specified: T_C = 30 °C.

Table 4. dc Characteristics

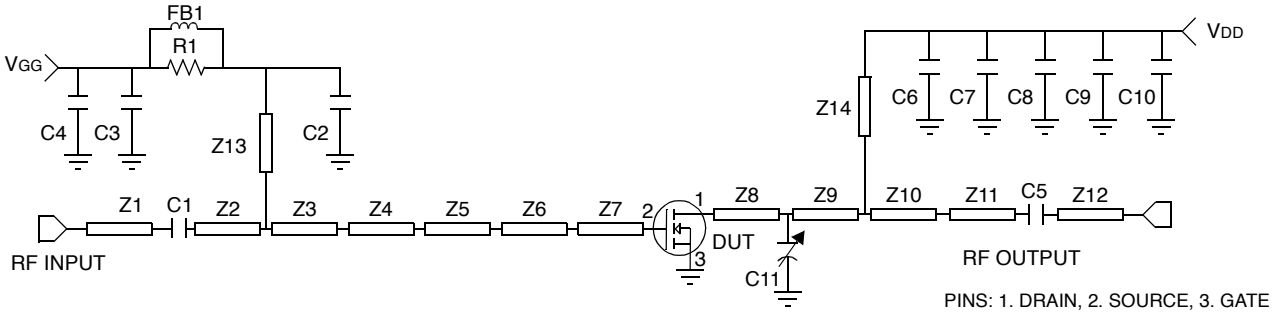
Parameter	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-source Breakdown Voltage (V_{GS} = 0 V, I_D = 150μA	$V_{(BR)DSS}$	65	—	—	Vdc
Gate-source Leakage Current (V_{GS} = 5 V, V_{DS} = 0 V)	I_{GSS}	—	—	1	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 26 V, V_{GS} = 0 V)	I_{DSS}	—	—	50	μAdc
On Characteristics					
Forward Transconductance (V_{DS} = 10 V, I_D = 0.4 A)	G_{FS}	—	2.4	—	S
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 μA)	$V_{GS(TH)}$	2.8	3.4	4.0	Vdc
Gate Quiescent Voltage (V_{DS} = 26 V, I_D = 300 mA)	$V_{GS(Q)}$	3.0	3.8	4.6	Vdc
Drain-source On-voltage (V_{GS} = 10 V, I_D = 0.4 A)	$V_{DS(ON)}$	—	0.30	—	Vdc

Table 5. RF Characteristics

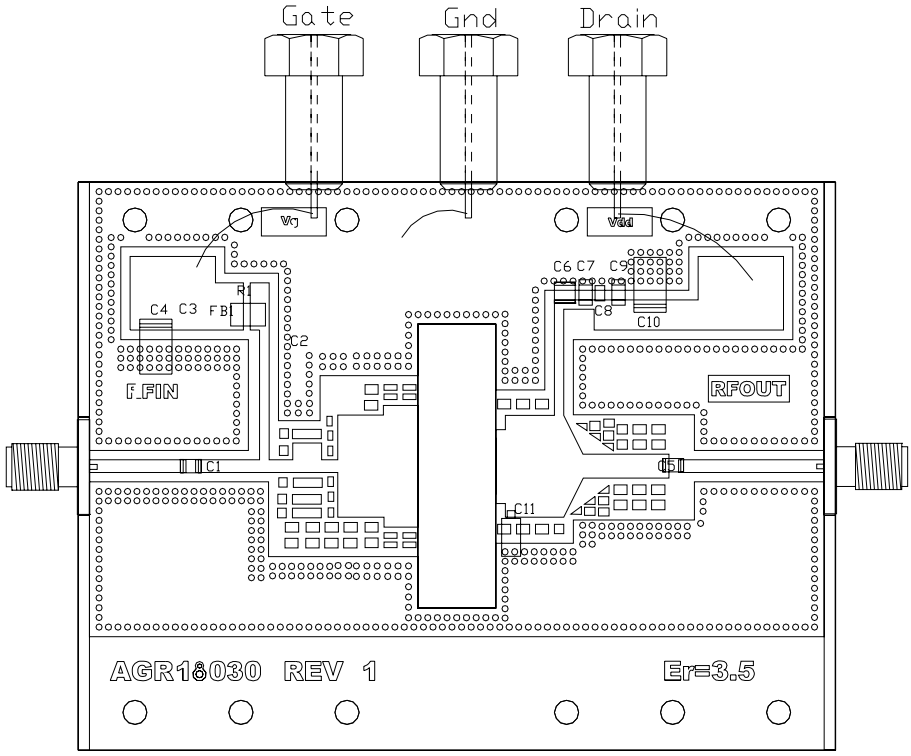
Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Characteristics					
Drain-to-gate Capacitance (V_{DS} = 26 V, V_{GS} = 0 V, f = 1 MHz)	C_{RSS}	—	0.8	—	pF
Functional Tests* (in Supplied Test Fixture)					
Power Gain (V_{DS} = 26 V, P_{OUT} = 15 W, I_{DQ} = 300 mA)	G_L	—	15	—	dB
Drain Efficiency (V_{DS} = 26 V, P_{OUT} = 15 W, I_{DQ} = 300 mA)	ˇ	—	30	—	%
EDGE Linearity Characterization (P_{OUT} = 10 W, f = 1.840 GHz, V_{DS} = 26 V, I_{DQ} = 300 mA)					
Modulation spectrum @ ±400 kHz		—	–64	—	dBc
Modulation spectrum @ ±600 kHz		—	–71	—	dBc
Output Power (V_{DS} = 26 V, 1 dB gain compression, I_{DQ} = 300 mA)	P1dB	—	33	—	W
Input Return Loss	IRL	—	–12	—	dB
Ruggedness (V_{DS} = 26 V, P_{OUT} = 30 W, I_{DQ} = 300 mA, VSWR = 10:1 [all angles])		No degradation in output power.			

* Across full DCS band, 1.805 GHz—1.880 GHz.

Test Circuit Illustrations for AGR18030EF



A. Schematic



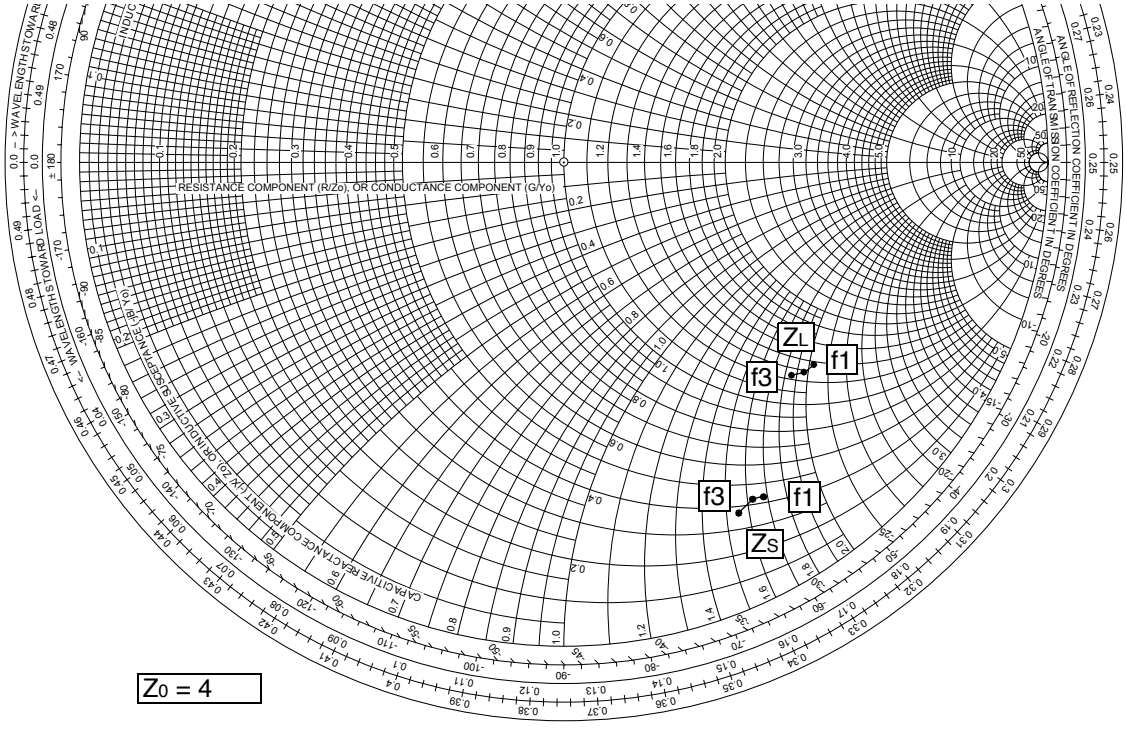
Parts List:

Microstrip line: Z1 0.510 in. x 0.066 in.; Z2 0.364 in. x 0.066 in.; Z3 0.151 in. x 0.066 in.; Z4 0.151 in. x 0.155 in.; Z5 0.085 in. x 0.066 in.; Z6 0.245 in. x 0.540 in.; Z7 0.182 in. x 0.644 in.; Z8 0.052 in. x 0.390 in.; Z9 0.309 in. x 0.539 in.; Z10 0.102 in. x 0.539 in. to 0.125 in. taper; Z11 0.454 in. x 0.125 in.; Z12 0.769 in. x 0.066 in.; Z13 0.050 in. x 0.560 in.; Z14 0.050 in. x 0.560 in.
ATC® chip capacitors: C1, C9: 8.2 pF, 100B8R2JW500X; C2, C6: 6.8 pF, 100B6R8JW500X.
Vitramon® chip capacitors: C3, C7: 22,000 pF.
Sprague® tantalum surface-mount chip capacitors: C4, C10: 22 μF, 35 V.
Murata® chip capacitor: C8: 0.01 μF, GRM40X7R103K100AL.
Kemet® 1206 chip capacitor: C9: 0.1 μF, C1206104K5RAC7800.
Johanson-GigaTrim® capacitor: C11: 0.4 pF—2.5 pF, 27281SL.
Fair-Rite® ferrite bead: FB1: 2743019447.
Resistor: R1: 12 .
Taconic® ORCER RF-35: board material, 1 oz. copper, 30 mil thickness, r = 3.5.

B. Component Layout

Figure 2. AGR18030EF Test Circuit

Typical Performance Characteristics



GHz (f)	ZS (Complex Source Impedance)	ZL (Complex Optimum Load Impedance)
1.805 (f1)	1.67 – j6.77	5.57 – j8.18
1.843 (f2)	1.64 – j6.41	5.19 – j7.83
1.880 (f3)	1.58 – j6.15	4.86 – j7.58

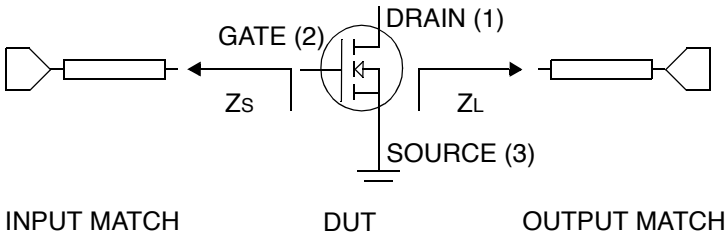
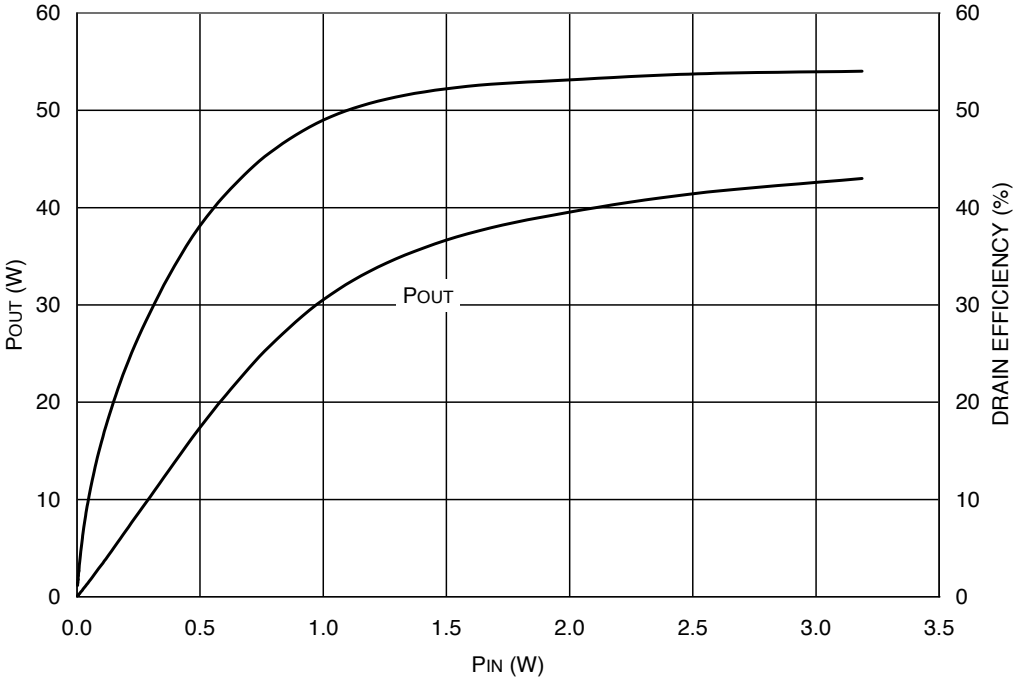


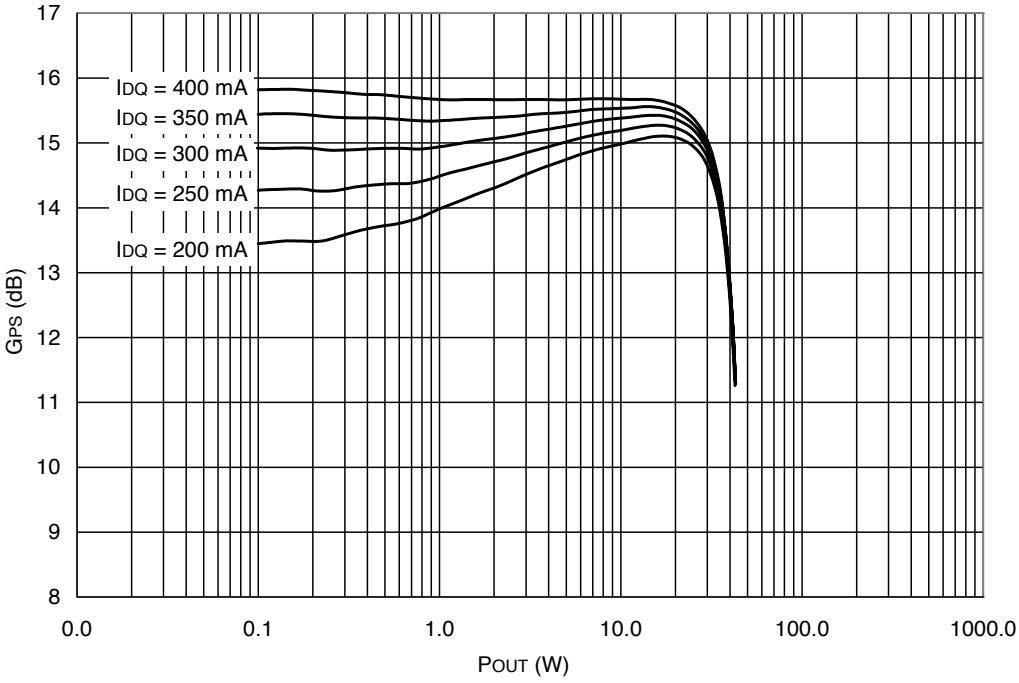
Figure 3. Series Equivalent Input and Output Impedances

Typical Performance Characteristics (continued)



TEST CONDITIONS:
V_{DD} = 26 V, I_{DQ} = 300 mA, f = 1842.5 MHz, CW MEASUREMENT.

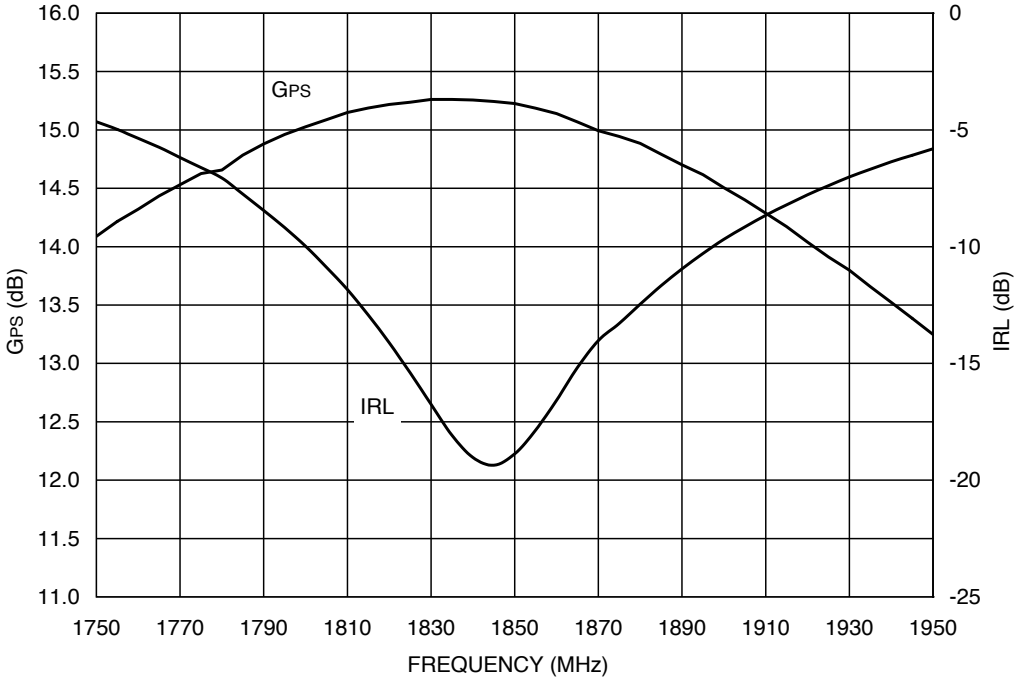
Figure 4. Output Power and Efficiency vs. Input Power



TEST CONDITIONS:
V_{DD} = 26 V, f = 1842.5 MHz, CW MEASUREMENT.

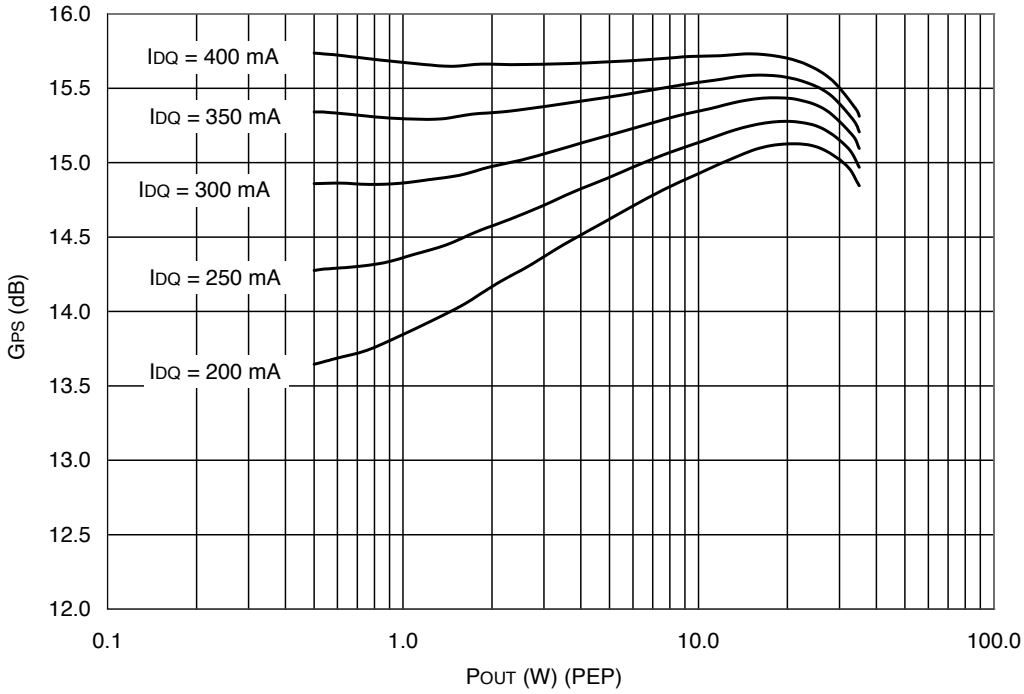
Figure 5. CW Power Gain vs. Output Power

Typical Performance Characteristics (continued)



TEST CONDITIONS:
V_{DD} = 26 V, I_{DQ} = 300 mA, P_{IN} = 25 dBm, CW MEASUREMENT.

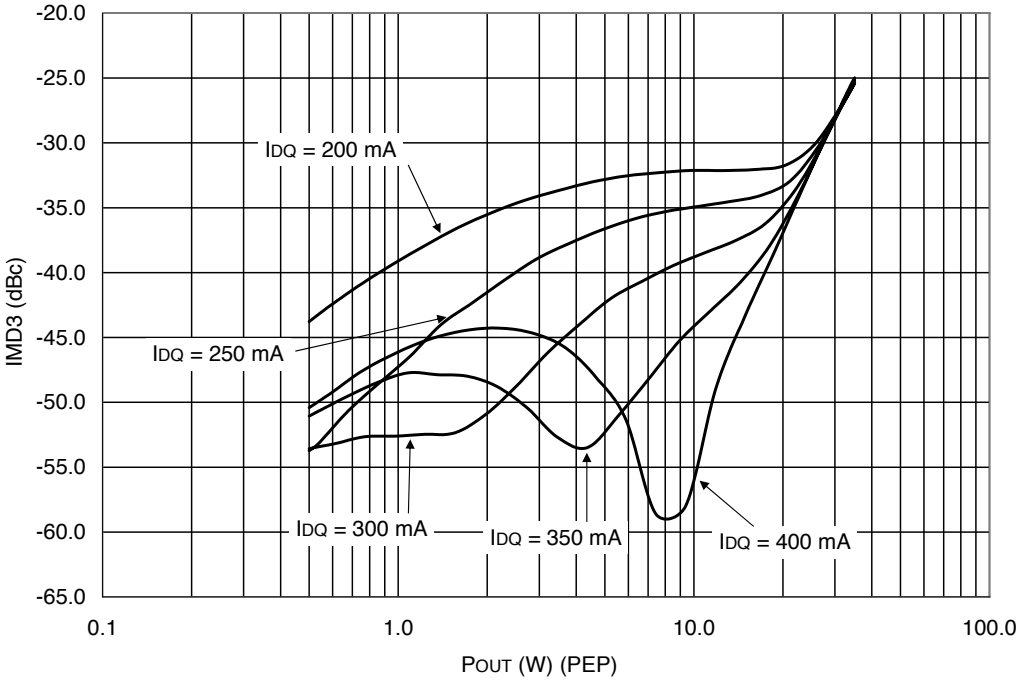
Figure 6. Wideband Gain and Return Loss



TEST CONDITIONS:
V_{DD} = 26 V, fc = 1842.5 MHz, TWO-TONE MEASUREMENT, 100 kHz SPACING.

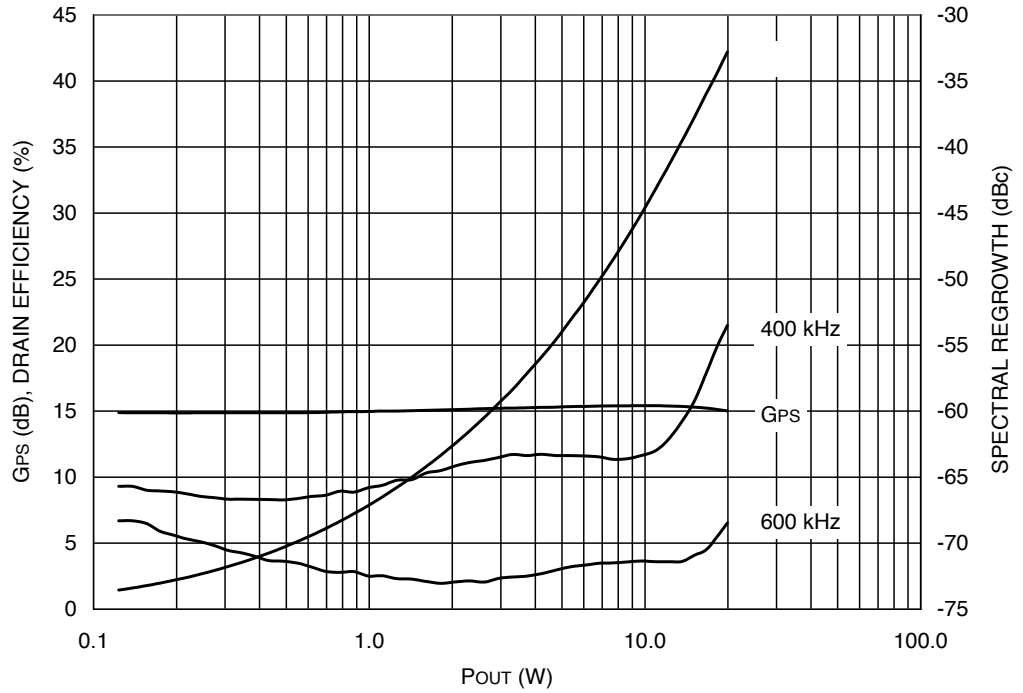
Figure 7. Two Tone Power Gain vs. Output Power

Typical Performance Characteristics (continued)



TEST CONDITIONS:
V_{DD} = 26 V, fc = 1842.5 MHz, TWO-TONE MEASUREMENT, 100 kHz SPACING.

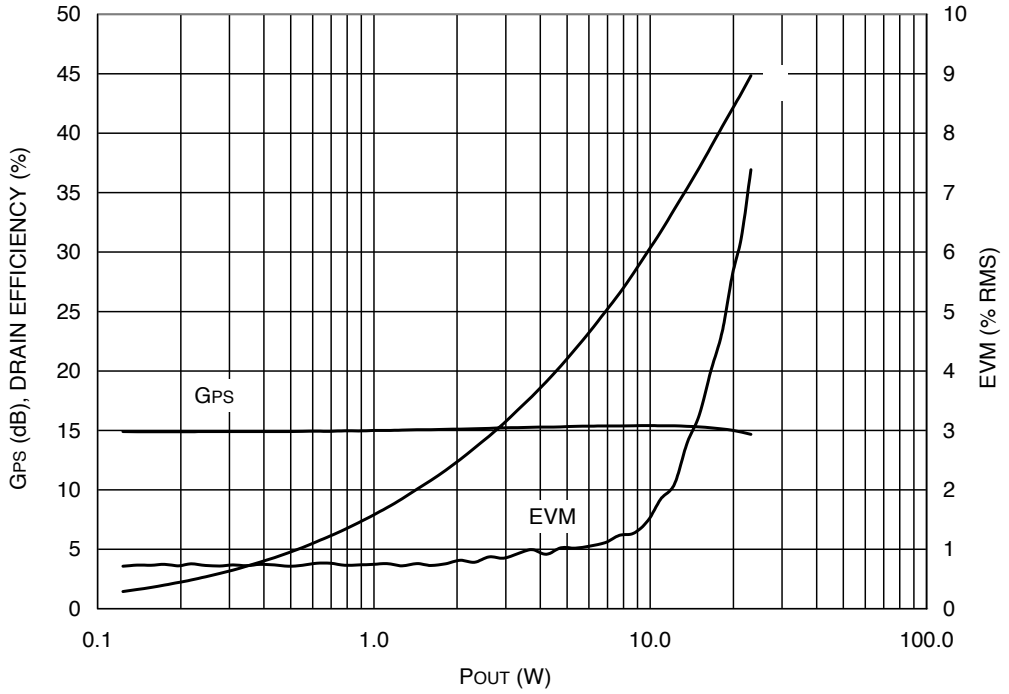
Figure 8. Intermodulation Distortion vs. Output Power



TEST CONDITIONS:
V_{DD} = 26 V, I_{DQ} = 300 mA, fc = 1842.5 MHz, EDGE MODULATION.

Figure 9. Power Gain, Efficiency, and Spectral Regrowth vs. Output Power

Typical Performance Characteristics (continued)



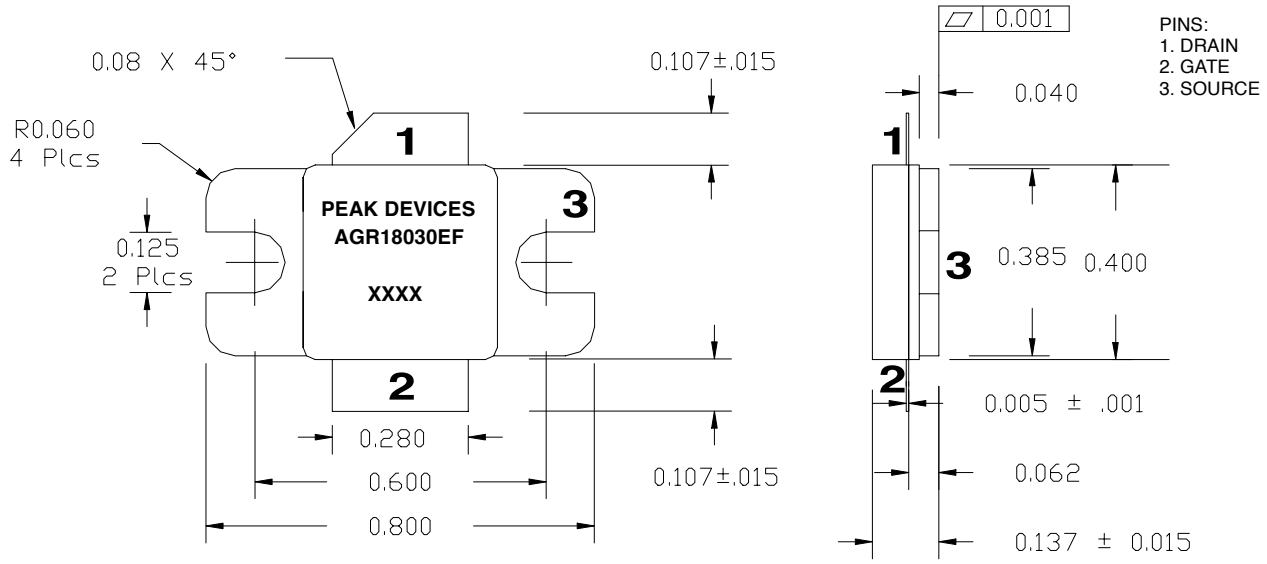
TEST CONDITIONS:
V_{DD} = 26 V, I_{DQ} = 300 mA, fc = 1842.5 MHz, EDGE MODULATION.

Figure 10. Power Gain, Efficiency, and EVM vs. Output Power

Package Dimensions

All dimensions are in inches. Tolerances are ±0.005 in. unless specified.

AGR18030EF



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