PD64004AH - 4-Port Power Sourcing Equipment Manager for Power over Ethernet Systems

Description

Microsemi's™ PD64004AH is a 4-port, mixed-signal, high-voltage Power over Ethernet (PoE) Manager designed to support IEEE 802.3af-2003 and 802.3at-2009 PoE applications.

PD64004AH is used in Ethernet switches (endspans) and midspans to enable next generation network managers to share power and data over the same cable. With full digital control via a serial communication interface and a minimum of external components, the PD64004AH can be placed in multi-port and highly populated Ethernet switches. PD64004AH integrates power, analog and logic functions in a single 48-pin, QFN-PS package allowing compact designs.

The PD64004AH detects IEEE 802.3af-2003 compliant Powered Devices (PDs) and 802.3at-2009 PDs which exceed IEEE802.3af power levels, ensuring safe power feeding and port disconnection.

The PD64004AH executes all real time functions as specified in the IEEE 802.3af-2003 standard and the IEEE802.3at-2009 standard including detection, 1-event classification and port status monitoring. It also executes system level activities such as power management, and MIB support for system management. The PD64004AH is designed to detect and disable disconnected ports, using both DC and AC disconnection methods, as defined in IEEE 802.3af-2003 and IEEE802.3at-2009.

The PD64004AH, in conjunction with the PD63000G or in Automatic mode, can be configured to support 2-pair 802.3at-2009 (up to 600 mA.) and 2-pair standard "af" power (up to 350mA) for full IEEE802.3af compliant functionality. Further, in AF mode the PD64004AH and PD63000G can support 8-ports operation (when working together, the units are in Enhanced mode).

Performance of the PD64004AH can be fully evaluated using the PD-IM-7316AH evaluation board.

IMPORTANT: For the most current data, consult MICROSEMI's website: http://www.microsemi.com

Applicable Documents

- PoE Controller PD63000/G datasheet, Catalogue Number 06-0008-058
- 16 port evaluation board PD-IM-7316AH User Guide, Catalogue Number 06-0025-056
- Twelve-channel PoE manager PD64012GH datasheet, Catalogue Number 06-0003-058
- AN-152, Designing 8-port PoE+ System Using PD64004AH, Catalogue Number 06-0034-080
- AN-140, Layout Design Guidelines for PoE Systems, Catalogue Number 06-0012-080
- AN-161, Layout Guidelines for PoE Systems, Catalogue Number 06-0066-080.
- AN-170, Designing a 16-port Enhanced PoE System, Catalogue Number 06-0042-080

Key Features

- IEEE 802.3af-2003 and 802.3at-2009 compliant
- Up to 600 mA Iport_max
- IETF Power Ethernet MIB (RFC 3621) compliant
- Single DC voltage input (44v-57v)
- Built in 3.3v regulator
- Low thermal dissipation (1 Ω sense resistor)
- Internal power-on reset
- Four ports
- Internal power FET per port
- Thermal monitoring and protection
- Supports any PD64004AH and PD64012GH combination
- Can be cascaded for up to eight PoE managers
- I^2C or UART communication to Host
- User friendly unique PoE communication protocol
- Direct register communication
- Continuous monitoring of individual ports
- Continuous system telemetries
- Parameters setting per port and per system
- Disabling of ports through hardware
- Enhanced power management algorithm
- Advanced power management; up to 32 ports
- Pre-standard PD detection
- Detection of Cisco devices
- Port matrix
- Interrupt out
- Hardware system status pin
- LED support
- Emergency power management with up to eight power supplies
- Rmode for H/W configuration
- RoHS compliant

PACKAGE ORDER INFO	
T_A (°C)	48-Pin QFNPS
-40 to +70*/85** °C	PD64004AH***

* Temperature range for full 802.3at-2009 (up to 600 mA) load.
** Temperature range for full standard “af” (up to 350 mA) load.
*** 'H' Stands for 802.3at-2009

Absolute Maximum Ratings

V_{main} ..... -0.3 to 80 VDC(1)
DGND, AGND, QGND, SENSE_NEG.....-0.3 to 0.3 VDC(2)

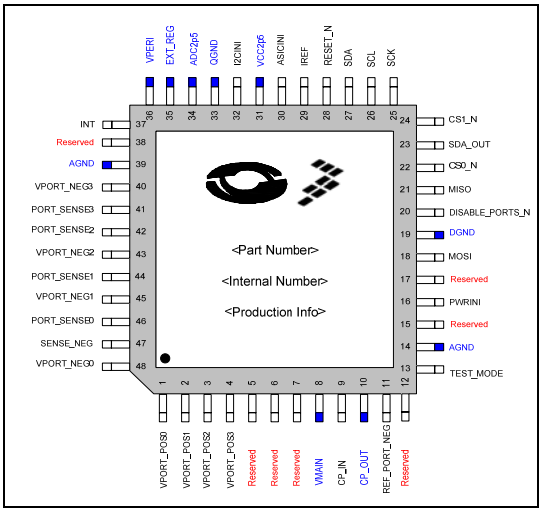
V_{PORT_POSx} ..... -0.3 to 80 VDC(1)
V_{PORT_NEGx}, REF_PORT_NEG
V_{PORT_POSx} - V_{PORT_NEGx}

PORT_SENSEx	0.3 to 15 VDC
VCC_{2p5}, ADC_{2p5}	.-0.3 to 3 VDC
V_{PERI}	4 VDC
EXT_REG	-0.3 to 6 VDC
I2CINI, ASICINI	-0.3 to 3 VDC
MISO, MOSI, SCK, SCL, SDA, CLK, RESETN, CS0_N, CS1_N	-0.3 to (VPERI + 0.3) VDC
ESD (Human Body Model)	-2 to 2 kV(3
Maximum junction temperature (T_{junc})	+150° C
Junction-ambient thermal resistance (θ_{JA})	25 °C/W
Junction-case thermal resistance (θ_{JC})	16° C/W
Lead temperature (soldering, 10 s)	300° C
Storage temperature	-40 to +125° C

Notes: “x” defines port numbers, 0 thru 3, inclusive.
(1) 80 VDC is the transient voltage that can be applied for 1 minute maximum.
(2) Maximum value between grounds.
(3) ESD testing is performed in accordance with the Human Body Model (CZap = 100 pF, RZap = 1500 Ω)

Stresses beyond those listed above may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Pin Out



Operating Conditions				
PARAMETER	MIN.	NOM.	MAX.	UNIT
Operating temperature at full 2-pair 802.3at-2009 load	-40		+70	°C
Operating temperature at full 2-pair standard “af” power (up to 350mA)	-40		+85	°C
Operational limitations (1)	15 to 44	44 to 55	55 to 57	VDC

1. Operating functions depend on the input voltage, as shown in Figure 1.
2. In order to get higher power drive at the PSE output ports, it is recommended to use operating voltage source Vmain > 50v

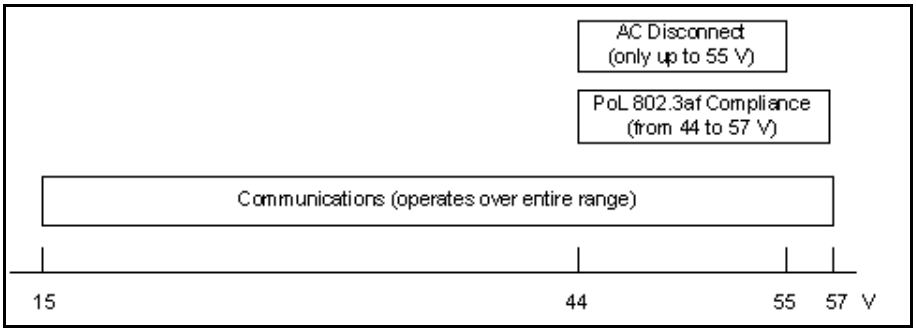


Figure 1: Operational Ranges

Electrical Characteristics

DC Characteristics for Digital Inputs and Outputs					
PARAMETER	**SYMBOL**	**MIN.**	**MAX.**	**UNIT**	**REMARKS**
Pin Name	DISABLE_PORTS, SCL				
Type	Schmitt Trigger CMOS input, TTL level with internal pull-up				
High level input voltage	V_{IH}	2.0		VDC	
Low level input voltage	V_{IL}		0.8	VDC	
Input voltage hysteresis		0.3		VDC	
Input high current	I_{IH}	-1	+1	µA	
Input low current	I_{IL}	-1	+1	µA	
Pin Name	SCL				
Type	Schmitt Trigger CMOS input, TTL level with internal pull-up				
High level input voltage	VIH	2.0		V	
Low level input voltage	VIL		0.8	V	
Pin Name	MOSI, MISO, CS0_N, CS1_N, SCK				
Type	CMOS I/O, TTL level with no internal pull up/pull down resistor				
High level input voltage	VIH	2.0		VDC	
Low level input voltage	VIL		0.8	VDC	
Input voltage hysteresis		0.3		VDC	
Input high current	IIH	-1	+1	µA	
Input low current	IIL	-1	+1	µA	
High level output voltage		VPERI-0.4 VDC		VDC	Iout = 2 mA

DC Characteristics for Digital Inputs and Outputs					
PARAMETER	**SYMBOL**	**MIN.**	**MAX.**	**UNIT**	**REMARKS**
Low level output voltage			0.4	VDC	Iout = 2 mA
Tri state output current		-1	+1	µA	
Pin Name	RESET_N, SDA				
Type	CMOS open drain output with Schmitt Trigger input, TTL level				
High level input voltage	VIH	2.0		VDC	
Low level output voltage	VOL		0.4	VDC	Iout = 6 mA
Low level input voltage	VIL		0.8	VDC	
Input voltage hysteresis		0.3		VDC	
Off state output current		-1	+1	µA	
Pin Name	SDA_OUT, INT				
Low Level output voltage			0.4	VDC	Iout = 6 mA
Off state output current		-1	+1	uA	

Electrical Characteristics for Analog I/O Pads				
PARAMETER	**MIN.**	**MAX.**	**UNIT**	**REMARKS**
Pin Name	VPORT_POSx			
Operating voltage	44	62	VDC	
Pin current consumption	-5	+10	µA	Port driver off, Vport differential measurement off, AC generator off
Pin Name	VPORT_NEGx, REF_PORT_NEG			
Operating voltage	44	62	VDC	Port driver off, Vport differential measurement off, AC generator off
Pin current consumption	-10	+10	µA	
Pin Name	PORT_SENSEx			
Operating voltage	0	1.48	VDC	With external 2 ohms (1%) to ground
Internal current consumption		20	µA	
Pin Name	VMAIN			
Operating voltage	44	57	VDC	
Vmain current consumption		10	mA	Total on Vmain
Pin Name	CP out			
Operating voltage	44	68	VDC	
Pin current consumption		5	mA	
Pin Name	ADC2p5, VCC2p5, VPERI, EXT_REG			
ADC2p5 output voltage	2.45	2.55	VDC	
ADC2p5 internal current consumption		6	mA	Recommended external cap. = 47 to 135 nF
VCC2p5 output voltage	2.37	2.62	V	Recommended external cap. = 47 to 135 nF
VCC2p5 internal current consumption		5	mA	
VPERI output voltage	3.10	3.46	VDC	Recommended external cap. = 1 to 4.7 µF
VPERI external current load		6	mA	Without external NPN
EXT_REG output current		30	mA	When using external NPN for VPERI

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Electrical Characteristics for Analog I/O Pads				
PARAMETER	**MIN.**	**MAX.**	**UNIT**	**REMARKS**
Pin Name	ASICINI, I2CINI			
Operating voltage	0	ADC2p5	VDC	
Current consumption	-1	+1	µA	
Pin Name	I_{REF}			
Output voltage	1.21	1.34	VDC	With external 24.9 kΩ resistor to ground
Pin Name:	PWRINI			
Operating voltage	0	100mV	V	From ADC2p5
Internal current source	+1.5	3	uA	

Dynamic Characteristics

The PD64004AH utilizes three programmable current level thresholds (I_{min}, I_{cut}, I_{lim}) and two timers (T_{min}, T_{cut}). Loads that dissipate more than I_{cut} for longer than T_{cut} (OVL_S to OVL) are classified as 'overloads' and are automatically shutdown. If output power is below I_{min} for more than T_{min} (UDL_S to UDL) the PD is classified as 'no-load' and is shutdown.

Automatic recovery from overload and no-load conditions is attempted every T_{OVLREC} and T_{UDLREC} periods (typically 5 and 1 seconds, respectively). Output power is limited to $I_{lim,}$ which is the maximum peak power allowed at the port.

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
Automatic recovery from overload shutdown	T_{OVLREC} value, measured from port shutdown			5		s
Automatic recovery from no-load shutdown	T_{UDLREC} value, measured from port shutdown			1		s
Cutoff timers accuracy	Typical accuracy of Tcut			3		ms
Inrush current	I_{Inrsh}	AF mode – t = 50 ms, Cload = 180 uF max. IEEE802.3at mode – t = 33 ms		654	450 692	mA
Output current operating range	Iport	Continuous operation after startup period.	10		600	mA
Output power available, operating range	P_{port}	Continuous operation after startup period, at port output.	0.57		30	W
Off mode current	I_{min1}	Must disconnect for t greater than TUVL	0		5	mA
	Imin2	May or may not disconnect for t greater than TUVL	5	7.5	10	mA
PD power maintenance request drop-out time limit	T_{PMDO}	Buffer period to handle transitions for both AF mode and IEEE802.3at mode	300		400	ms
Over load current detection range	Icut	AF mode - Time limited to TOVL IEEE802.3at mode - Time limited to TOVL	350 600		400 615	mA
Over load time limit	TOVL	AF mode IEEE802.3at mode	50	 33	75	ms
Turn on rise time	T_{rise}	From 10% to 90% of V_{port} (Specified for PD load consisting of 100 uF capacitor in parallel to 200 Ω).	15			us
Turn off time	Toff	From Vport to 2.8 VDC			500	ms

Thermal Data (Power Consumption)

The internal power consumption of a single PD64004AH from the DC input is based on:

Input voltage range: 44 to 57 V_{DC}
Input current: 7 mA maximum

$P_{MAIN} = V_{MAIN} \times I_{MAIN}$

Assuming the worst case, maximum power consumption is given by:

$P_{MAIN\_MAX} = 57\ V_{DC} \times 7\ mA = 0.4\ W$

Device Power Dissipation

The PD64004AH integrates four power MOSFETs. Each MOSFET is characterized by:

- Drain-to-Source resistance, R_{DSON} = 0.3 Ω typ; 0.5 Ω maximum
- Drain-Source current, I_{DS} = 600 mA max.

Hence, maximum power dissipation $P_{MOSFET\ MAX}$ of a single PD64004AH device (for 4 MOSFETs) is given by:
$[(I_{DS})^2 \times R_{DSON\_MAX}] \times 4 = [(0.600\ A)^2 \times 0.5\ \Omega] \times 4$
$= 0.\ 73\ W$

Power dissipation of the internal charge pump, P_{CP} is 0.21 W.

Hence total power dissipation P_{TOTAL}, under maximum conditions is given by:
$P_{TOTAL} = P_{MAIN\_MAX} + P_{MOSFET\_MAX.} + P_{CP}$
$= 0.4\ W + 0.73\ W + 0.21\ W$
$= 1.34\ W$

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Protection Mechanism

The PD64004AH includes an internal thermal protection feature, designed to protect the junction from overheating;

Configuration Pins

Three main configuration pins are utilized in the PD64004AH to reduce the need for communication (Figure 2).

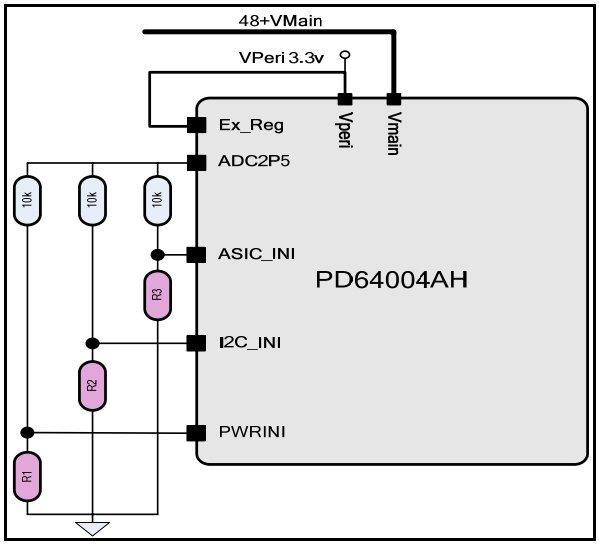

Figure 2: Electric Connection of Configuration Pins

Power_ini
The power limit parameter is set by a resistor divider that actually sets the voltage at pin #16. There are 16 voltage levels that provide various power limit levels and guard-band levels as shown below:

Mode Number	PWRINI Voltage Level**	Power Limit (W)	Guard Band (W)
1*	2.40 VDC to 2.50VDC	800	21
2	2.24VDC to 2.28VDC	22	8
3	2.08VDC to 2.13VDC	30	8
4	1.92VDC to 1.97VDC	35	8
5	1.76VDC to 1.82VDC	40	8
6	1.60VDC to 1.67VDC	45	8
7	1.44VDC to 1.52VDC	50	10
8	1.28VDC to 1.36VDC	55	10
9	1.13VDC to 1.21VDC	60	10
10	0.97VDC to 1.06VDC	65	10
11	0.81VDC to 0.90VDC	70	10
12	0.65VDC to 0.75VDC	80	13
13	0.49VDC to 0.60VDC	90	13
14	0.33VDC to 0.44VDC	100	13
15	0.16VDC to 0.29VDC	110	13
16	0.00VDC to 0.14VDC	800	21

* This mode should be set for applications that have a 2 Ω Rsense only. All other modes are for 1 Ω Rsense applications.

**The above voltage values are calculated assuming that the ADC2p5 voltage is 2.5 VDC with accuracy of ±2%.

ASIC_INI

PoE Manager's configuration is performed via the ASIC_INI pin, as shown below. The ASIC_INI signal is converted into a 10-bit register (A/D). Once a hard reset pulse is detected, the data is latched into an internal mode register.

Mode Name	ASIC_INI Voltage Level
802.3at-2009 mode (including standard AF mode)	0.33v to 0.60v

Pinout Description

Functional Pin Description		
Name	Pin #	Description
VPORT_POS0	1.	Port 0 positive voltage feeding
VPORT_POS1	2.	Port 1 positive voltage feeding
VPORT_POS2	3.	Port 2 positive voltage feeding
VPORT_POS3	4.	Port 3 positive voltage feeding
Reserved	5.	Not connected
Reserved	6.	Not connected
Reserved	7.	Not connected
VMAIN	8.	Main voltage supply
CP_IN	9.	Charge pump input, Vmain
CP_OUT	10.	Charge pump output pulse
REF_PORT_NEG	11.	Port negative reference
Reserved	12.	Not connected
TEST_MODE	13.	Test mode pin – connect to AGND
AGND	14.	Analog ground
Reserved	15.	Not connected
PWRINI	16.	Preset power limit values
Reserved	17.	Not connected
MOSI	18.	SPI bus, master data out/slave in
DGND	19.	Digital ground
DISABLE_PORTS_	20.	Disable all ports power – active low
MISO	21.	SPI bus, master data in/slave out
CS0_N	22.	SPI bus, chip select 0
SDA_OUT	23.	Third pin in I^2C protocol
CS1_N	24.	SPI bus, chip select 1
SCK	25.	SPI bus, serial clock I/O
SCL	26.	I^2C bus, serial clock Input
SDA	27.	I^2C bus, open drain
RESET_N	28.	Active Low Reset I/O
IREF	29.	Current reference
ASICINI	30.	Analog input for ASIC initialization
VCC2p5	31.	Internal 2.5v supply (do not use!)
I2CINI	32.	Analog input for I^2C initialization
QGND	33.	Quiet analog ground
ADC2p5	34.	ADC reference (do not use!)
EXT_REG	35.	External regulation
VPERI	36.	Regulated 3.3v power source
INT	37.	Interrupt, open drain
Reserved	38.	Not connected
AGND	39.	Analog ground
VPORT_NEG3	40.	Port 3 negative voltage feeding
PORT_SENSE3	41.	Channel current monitoring
PORT_SENSE2	42.	Channel current monitoring
VPORT_NEG2	43.	Port 2 negative voltage feeding
PORT_SENSE1	44.	Channel current monitoring
VPORT_NEG1	45.	Port 1 negative voltage feeding
PORT_SENSE0	46.	Channel current monitoring
SENSE_NEG	47.	Port sense reference
VPORT_NEG0	48.	Port 0 negative voltage feeding

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Interrupt State - Machine	

The interrupt state-machine obviates the need for communication between the host CPU and the PD64004AH. When a PoE event occurs, the interrupt pin level drops to 'low', thus the host CPU is notified. Then the host CPU requests information related to the event.
 	
This method differs from the polling method, where the Host controller prompts all PoE Managers cyclically in order to receive information related to a PoE event.
 	
When an event occurs, the type of event is entered into the main interrupt register which is the first register to be read by the Host after receiving an interrupt. There are two main event types.
 	
The first event is a system event and the second is a port event. When a port event occurs, the host CPU should read another register to ascertain which port caused that event.
 	
Port event registers are individually cleared right after reading them (clear on read).
	If desired, one or more registers can be masked so as to avoid receiving non-desired interrupts by the Host. The following are the main events supported by the interrupt:
	
	• Port power switched on
	• Port power switched off due to:
	  ▪ Port disable
	  ▪ Overload, short condition or over temperature
	  ▪ AC disconnect or DC disconnect
	  ▪ Power management algorithm
	• Port was started up
	• AF detection completed successfully
	• AF classification routine was completed. Asserted at the end of classification cycle.
	• Vmain out-of-range
	• Temperature out-of-range

Block Diagram

The PD64004AH PoE Manager complies with all the IEEE standard 802.3af-2003 detection requirements.
PD64004AH is built around two major sections (Figure 3):

- A common digital section that serves all four channels
- Four separate identical channels for driving ports

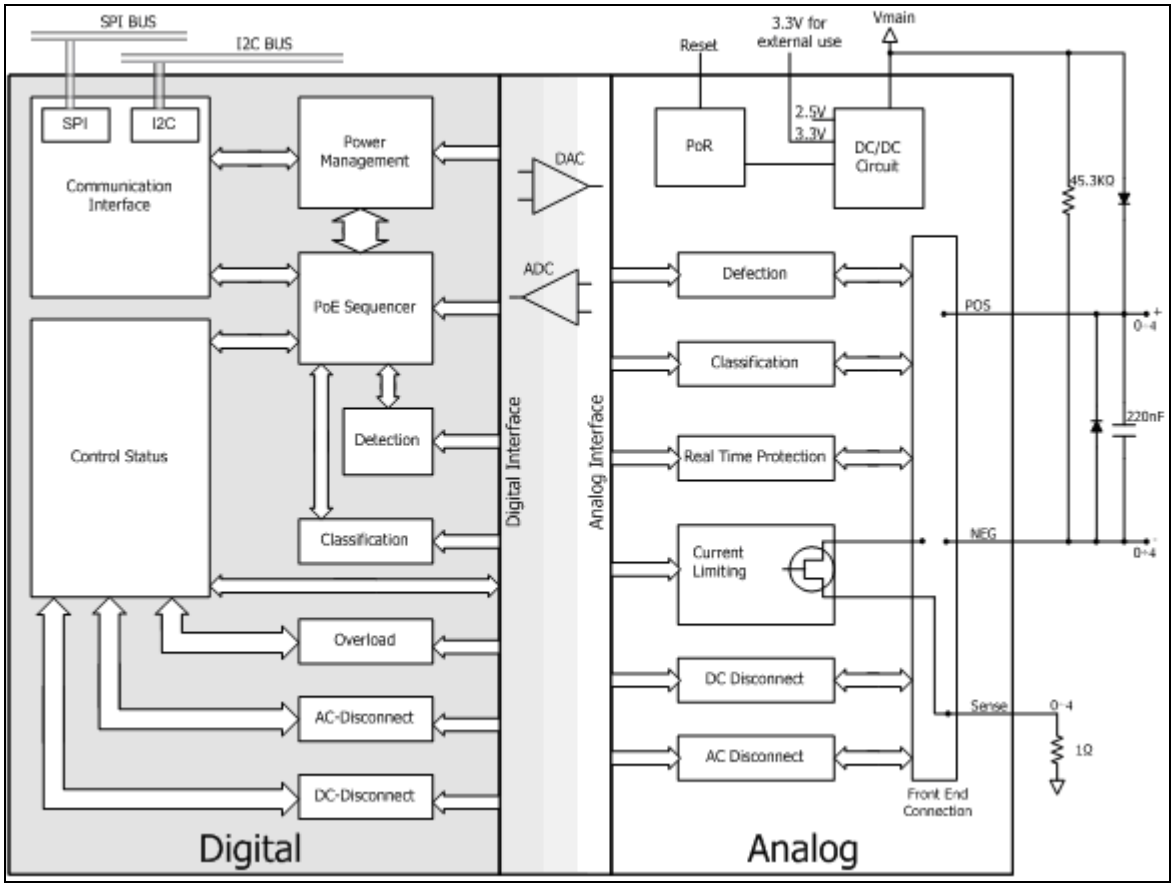

Figure 3: Internal Block Diagram

Communication Interface

The PD64004AH incorporates two communication interfaces. The first interface is an SPI bus which connects the PD63000G PoE Controller to the PD64004AHs. The second interface is an I^2C used to communicate with the Host. Both interfaces transmit the contents of the internal registers between the PD64004AH logic and the PoE Controller.

Power Management

Receives data from the PoE sequencer and determines which port is to be connected and which port is to be disconnected, in accordance with the system's total power. This block is active in the **Master chip only**!

Control Status

Several macros control the port enable function and others control the port disconnect function.

- *Port enable*: Resistor Line Detection, Classification.
- *Port disable*: AC Disconnect, DC Disconnect and Overload Logic.

These macros are connected to the Channel RT Control Status circuitry. Based on the inputs from these macros, the Channel RT controller starts the shutdown process or the recovery process.
This is performed in accordance with the pre-programmed parameters for different time windows.

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PoE Sequencer	AC Disconnect	Current Limit
The PoE Sequencer is the core of the Digital section; it includes an internal state machine that controls the macros (described below) and transfers the data from those macros.	The system applies a sinusoidal signal to the positive port terminal. The voltage developed on the port terminals is proportional to the load value. If the load is high, the AC component riding on the port terminals is low. If the load is low, the AC component is high. A dedicated circuit measures the AC component level and compares it with a pre-defined value stored in a register. Based on the comparison's results, the system determines whether to disable a port or not.	This circuit continuously monitors the current of powered ports and limits the current to a specific value in cases where an over load occurs. If the current exceeds a specific level, the system starts measuring the elapsed time. If this time period is greater than a preset threshold, the port is disconnected.
Detection	**DC Disconnect**	**Power on Reset (POR)**
The PoE Controller or the PoE sequencer generates a request to apply separate voltage levels to the output port. A measurement circuit monitors the difference between the various levels. Voltage differences are compared with values stored in the registers. By comparing these values, the system can determine whether to enable a port or not.	This block senses when the port current drops below 7.5 mA. If this is the case, a flag is 'raised' and timers in the Channel RT Controller start counting. The Channel RT Controller acts in accordance with pre-programmed thresholds limits and time windows, prior to initiating a disconnect status for that port. The circuitry takes into account PDs that modulate their current consumption, disconnecting them only if necessary.	The POR Monitors the internal DC levels; if these voltages drop below specific thresholds, a Reset signal is generated and the PD64004AHs are reset via the RESET_N pin.
Classification	**DC/DC Circuit**	**Real Time Protection**
Upon request from the PoE Controller or from the PoE sequencer, the state machine applies a regulated 18 VDC to the port output. The current is measured by comparing the real current flow with a number of preset thresholds; in this manner the class is verified.	This circuit produces 2.5V and 3.3V, derived from the Vmain main supply.	This circuitry performs all real time measurements and sends the results to the logic circuitry in order to determine whether to disconnect a port or not.
Overload		
This block senses when the port current exceeds the maximum current level as specified in the IEEE-802.3af standard, and disconnects the port if required.		

Application Information

The PD64004AH can be integrated into a number of applications such as Ethernet switches, routers, Midspans, and more. Examples of such applications are described below:

- **Integrated directly into a switch**: Facilitates entire PoE concept, by including the IC(s) on the main switch's PCB.
- **Daughter board add-on:** Which the IC is integrated into a small PoE dedicated PCB, mounted on top of the switch's main PCB.
- **Midspans**: Stand alone devices, installed between the Ethernet switch and PDs (Powered Devices) such as telephone, camera, wireless LAN, etc.).
  These Midspans include the PD64004AH IC as a PoE control element, designed to inject power over the communication lines.

Figure 4 through Figure 6 provide detailed schematic diagrams for various applications of the PD64004AH.

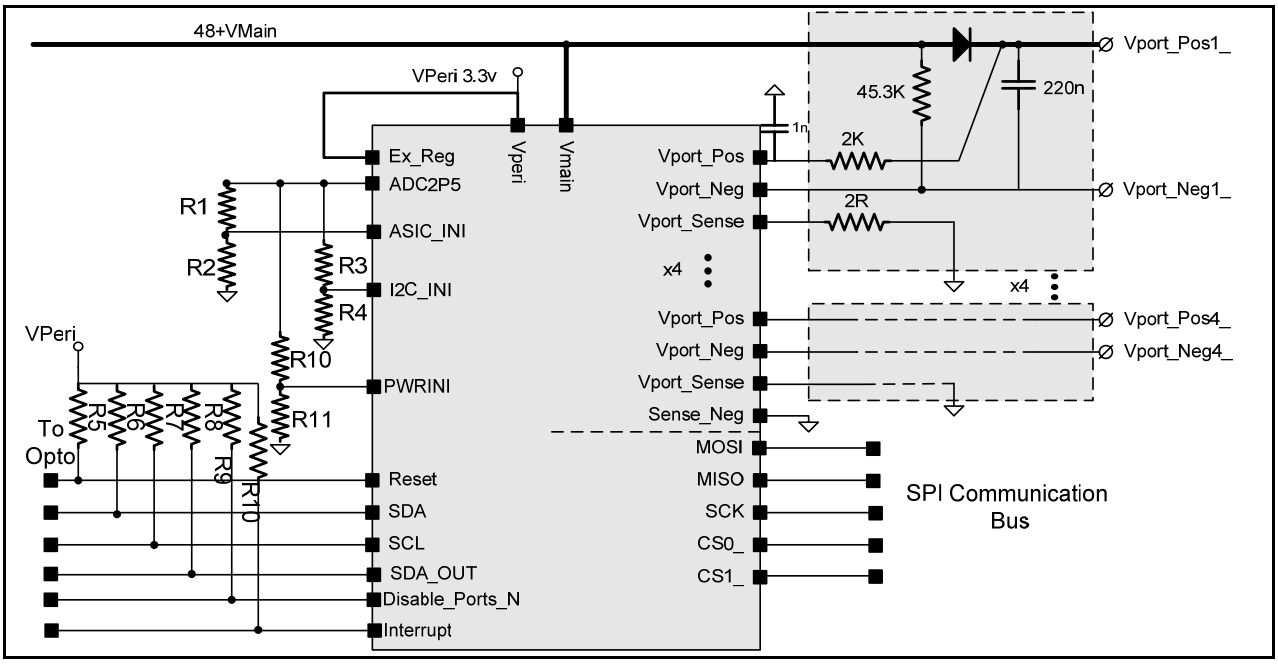


Figure 4: Single-port Application with AC Disconnect Support

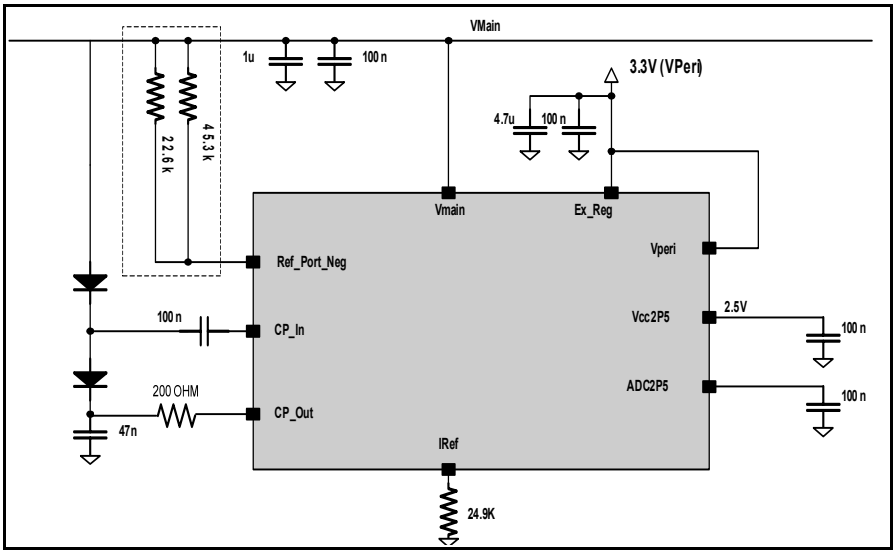


Figure 5: Typical Power Filtering

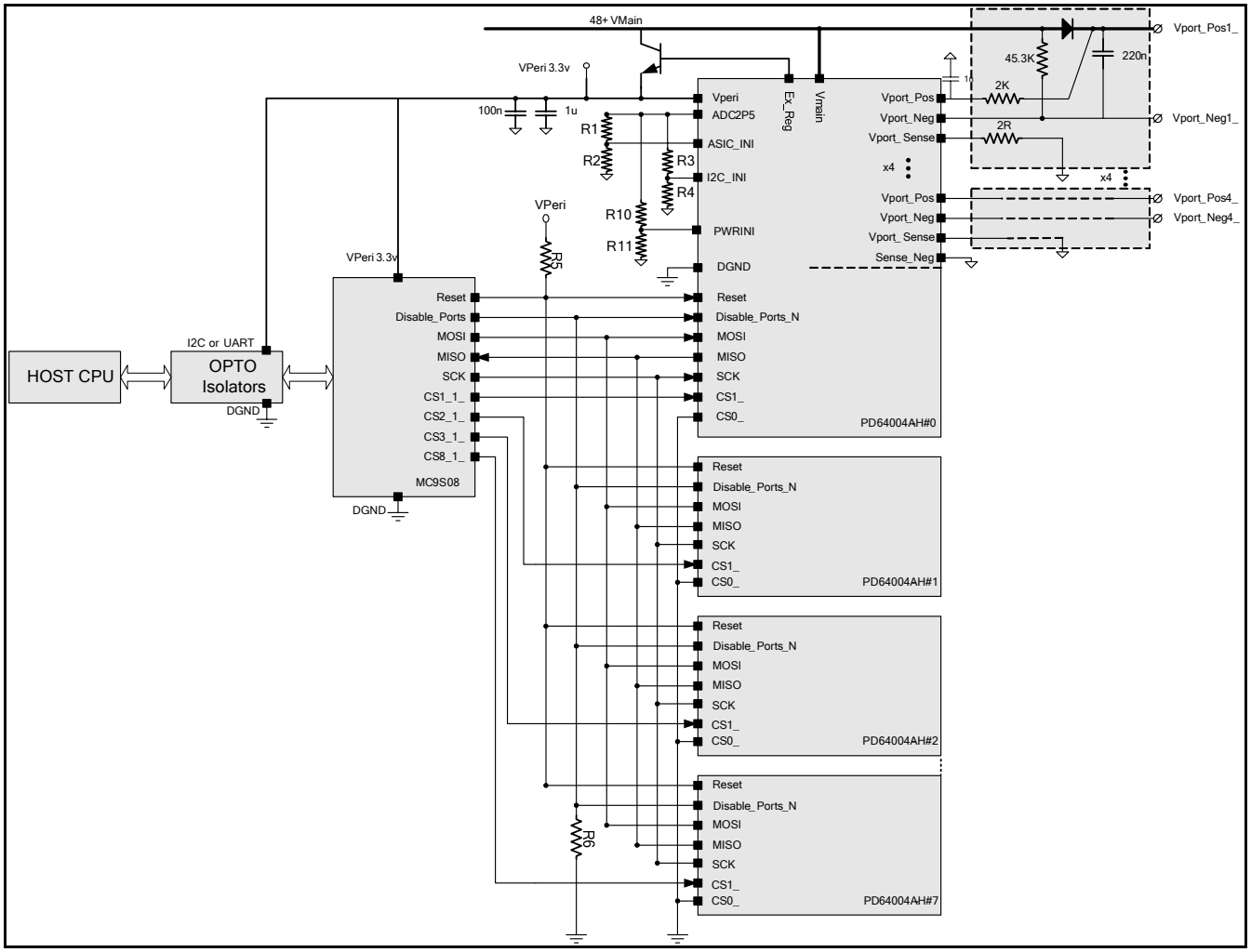
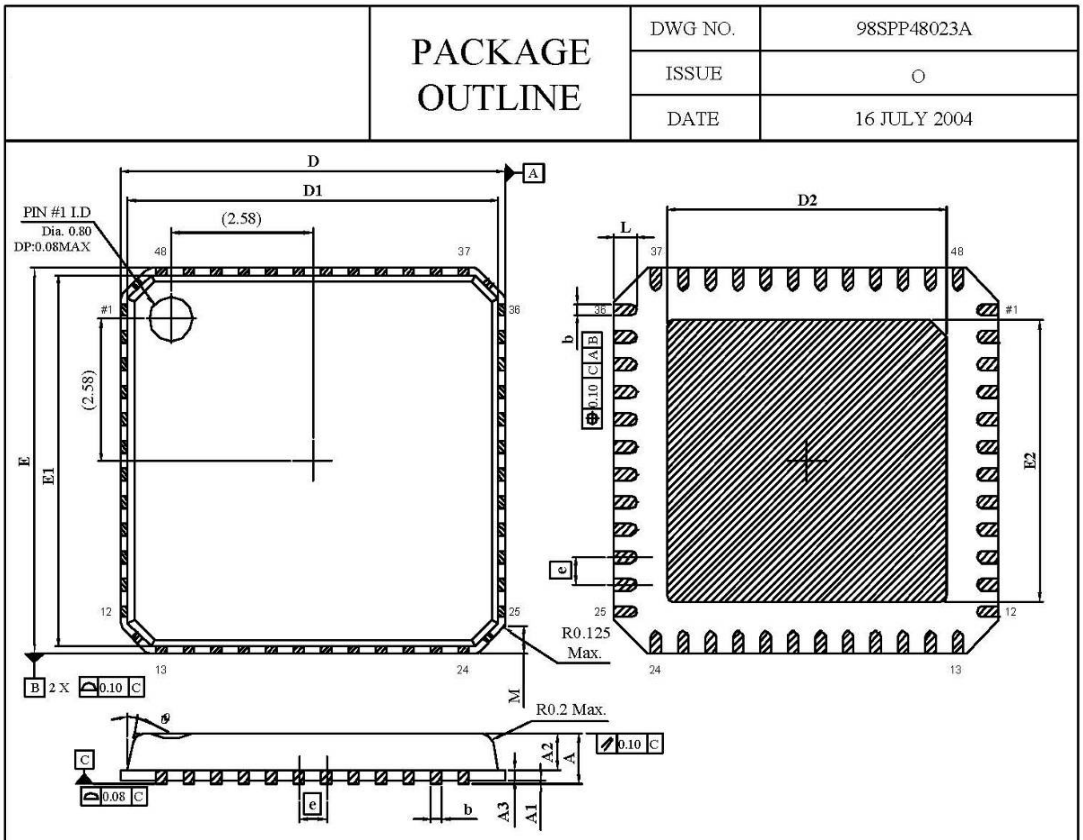


Figure 6: Typical Application

Package Information

The PD64004AH is housed in a 48QFN-PS plastic package, 7 x 7 x 0.9 mm, meeting JEDEC's MS-026 package outline and dimensions. Exposed pad (for heat-sinking purposes) dimensions are 5.00 by 5.00 mm



DIM	MIN.	NOR.	MAX.
A	-	0.85	0.90
A1	0.00	0.01	0.05
A2	-	0.65	0.70
A3		0.20 REF.	
b	0.15	0.20	0.25
D		7.00 BSC.	
D1		6.75 BSC.	
D2	4.95	5.10	5.25
E		7.00 BSC.	
E1		6.75 BSC.	
E2	4.95	5.10	5.25
e		0.50 BSC.	
L	0.30	0.40	0.50
M	0.45	0.50	0.55
θ	-	11°	12°

NOTES

1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.

2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

3.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.

4.0 RADIUS ON TERMINAL IS OPTIONAL.

5.0 MOLD SURFACE ROUGHNESS : 0.8~1.0m(Ra)

QFN 7X7 48LD 5.10 SQ.PAD
(PUNCHED SINGULATION TYPE)

COMPANY

SHEET 1 OF 2

Figure 7: PD64004AH Mechanical Dimensions

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Feature	Description
IEEE 802.3af-2003 Compliant	The PD64004AH meets all IEEE-802.3af-2003 standard requirements including: • Multi-point resistor detection • PD 1-event classification function • AC disconnection and DC disconnection functions • Supports back-off feature for Midspan implementation
802.3at-2009 Compliant	Enables detection and powering of 802.3at-2009 Compliant PDs via the two pair for pre-standard PDs.
IETF Power Ethernet MIB (RFC 3621) Compliant	The PD64004AH meets all IETF power Ethernet MIB (RFC 3621) requirements including port enable/disable, port priority, classification, error counters and system/port power consumption.
Single DC Voltage Input	The PD64004AH requires a single DC voltage input: 44V to 57V. No additional voltage inputs (for example 3.3V/5V) are required to operate the PoE system.
Built-In 3.3 Regulator	The PD64004AH, with few additional components can provide 3.3V source (up to 30mA) for other peripherals such as a PoE Controller and opto-couplers.
Low thermal dissipation (1Ω sense resistor)	The PD64004AH has a very low thermal dissipation. It has an exposed pad that keeps the PoE Manager at a low temperature. The Rsense in PD64004AH applications is only 1 Ω which keeps the peripheral components at a low temperature as well.
Internal Power-on Reset	The power-on reset circuitry monitors the internal voltage regulators (2.5V, Vperi 3.3V and 10V). If one of these voltages drops below a pre-defined level, the PD64004AH is reset until all voltages rise above the proper levels again.
Supports 4 Port PoE implementations	The PD64004AH has high port density (4 ports) integrated into a single device, thus saving PCB space, reducing PoE system cost and simplifying the circuit design.
Internal Power FET Per Port	Four power FETs are integrated into a single PD64004AH to save PCB space and simplify the circuit design. The exposed pad under the 48 QFN package dissipates the heat from the PD64004AH to the PCB.
Thermal Monitoring/Protection	The PD64004AH integrates internal thermal protection features designed to protect the junction from overheating; Three types of temperature sensors are integrated on PD64004AH; two are utilized for protection and one is utilized for monitoring.
Support any PD64004AH and PD64012GH Combination	PD64004AH can also be used with the PD64004AH, 4-Port PSE Manager, to implement more than 12 ports. Multiple PD64012GHs and PD64004AHs can be used simultaneously. This flexibility provides multiple port options, from 12 to 96 ports, with minimizing costs and optimizing PCB space. In this implementation, either the PD64012GH or the PD64004AH can be configured as master or slave.
Cascade up to Eight PoE Managers	Up to eight PD64004AHs can be cascaded to implement multiport PoE system to a maximum of 96 ports.
I2C or UART Communication to Host	Enables I^2C communication or UART Communication between the host CPU and the PoE controller for continuous monitoring and for port parameter setting.
User Friendly Unique PoE Communication Protocol	A unique 'Host CPU' - 'PoE Controller' communication protocol optimizes PoE continuous monitoring and simplifies PoE parameter setting.
Direct Register Communication	The host CPU communicates with the PD64004AH PoE manager by writing and reading to/from its registers directly.
Continuous Monitoring of Individual Ports	The host CPU can receive on-line information per port such as: • Port current and power measurement • Port class • Port status (on, off, overload, and short) • Port matrix, interrupt events, etc.

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Feature	Description
Continuous System Telemetries	On-line system telemetries for the host CPU including: • Voltage measurement • Total system power consumption • System and ICs status
Parameters Setting per Port and Per System	Configurable parameters via the host CPU including: • Port priority • Power management parameters (power limit, Guard band level, PM mode) • Forced power and disable power per port • AC/DC disconnection method • LEDs parameters, port matrix, PoE Controller interrupt-out masks, flags, etc.
Disabling of Ports Through Hardware	The PD64004AH features a dedicated pin (Disable_Ports) enabling an immediate disconnection of all ports. It is controlled by the host CPU. All ports are disconnected when voltage level on this pin is low. This is the quickest way to turn-off all ports.
Enhanced Power Management Algorithm	The system supports the following power management modes: Class mode, Allocation mode, Dynamic mode and Auto-PM mode, which combine all three modes. The power management feature is a continuous real-time algorithm designed to prevent power consumption beyond a predefined limit. Disconnection and connection of ports is performed, as specified, in the power management mode.
Advanced Power Management for up to 96 Ports	Additional flags improve the power management algorithm and provide the host with more flexibility when configuring the system.
Pre-Standard PD Detection	Enables detection and powering of pre-standard PDs.
Detection of Cisco Devices	Enables detection and powering of all Cisco devices including pre-standard terminals.
Port Matrix	Allows the layout designer to connect the physical ports to the logical ports when desired.
Interrupt - Out	Reduces communication overhead of the host CPU. Whenever a PoE event (masked by the host CPU) occurs; the PoE Controller sends an interrupt to signal the PoE event.
Hardware System Status Pin	An optional hardware signal between the PoE Controller and the host CPU, provides the host CPU with a warning that a major failure (for example Vmain out of range) has occurred.
LED Support	Direct SPI interface to an external LED Stream circuitry. It enables the designer to implement a simple LED circuit without any software code.
Emergency Power Management	For systems comprising more than a single power supply, a fast port disconnection mechanism is activated in case one of the power supplies fails, to maintain operation and prevent collapse of other power supplies. Up to eight power supplies are supported.
Rmode – H/W configuration	H/W pin on the PoE Controller allows hardware configuration of the following parameters: • Power management mode • AC or DC disconnect • All ports ON or OFF • IEEE 802.3af detection or IEEE 802.3af & pre-standard detection

System Description

PD64004AHs communicate with the PD63000G, PoE Controller (dedicated controller for PoE tasks), via a Serial Parallel Interface (SPI) bus. In this mode, all PD64004AHs are directly connected to the PD63000G via the SPI bus in slave mode. The switch host CPU communicates with the PD63000G via an isolated I^2C or UART bus.

Figure 8 illustrates a typical application configuration.

The PD63000G controller is configured by the host CPU to initialize and control the PD64004AHs to support 802.3at-2009 PDs and/or IEEE802.3af standard PDs. The PD63000G is designed to perform enhanced sequential start-up mechanism and enhanced power management, maintaining temperature and stress levels within the specification.

802.3at-2009

When configured for 802.3at-2009, each PD64004AH can support up to 600 mA per port (30 watts at PSE output @ 50v) on all the four ports. Under this configuration, if the PD is classified as Class #4, up to 600 mA is supported. If the PD is classified as Class #0, Class #1, Class #2 or Class #3, then standard power up to 350 mA is supported. Hence when configured for IEEE802.3at-2009 both 802.3at-2009 PDs and "af" PDs are supported depending on the class information.

Standard "af" Power

When configured for standard "af" power, each PD64004AH can support up to 350 mA per port (15.4 watt at PSE output @ 44v) on all the four ports.

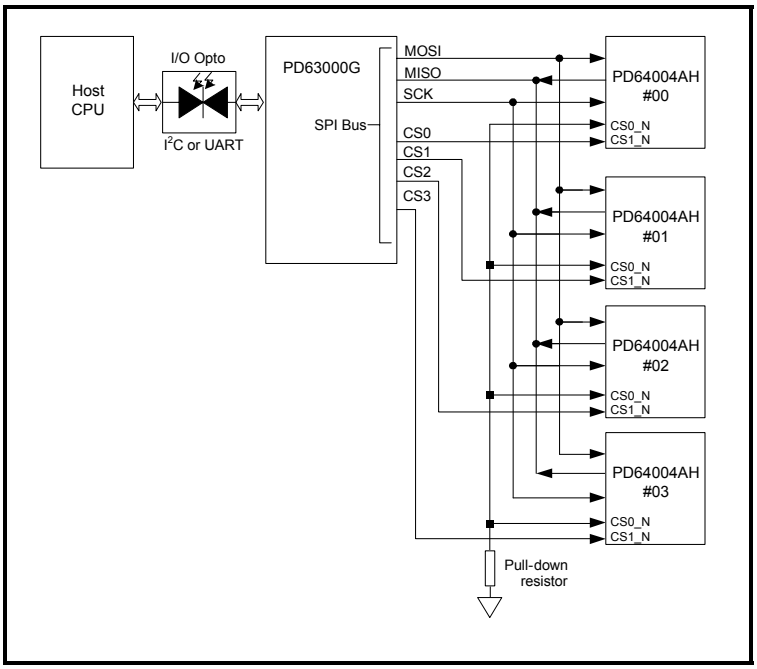

Figure 8: Typical Application Configuration

Revision History

Revision Level / Date	Para. Affected/page	Description
1.0 / 14 January. 10		Initial release

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