

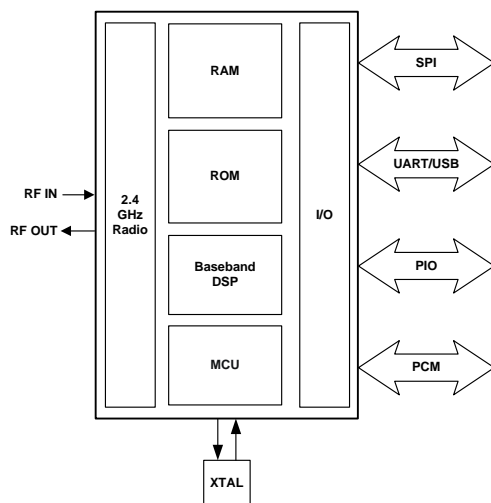
Device Features

- Fully Qualified Bluetooth v2.0 system
- Enhanced Data Rate (EDR) compliant with v2.0.E.2 of specification for both 2Mbps and 3Mbps modulation modes
- Full Speed Bluetooth Operation with Full Piconet Support
- Scatternet Support
- 1.8V core, 1.7 to 3.6V I/O split rails
- Low Power 1.8V Operation
- Small footprint 6 x 6mm 84-ball VFBGA Package
- Minimal External Components Required
- Integrated 1.8V regulator
- USB and Dual UART Ports to 3MBaud
- Support for 802.11 Coexistence
- RoHS Compliant

General Description

BlueCore4-ROM is a single chip radio and baseband IC for Bluetooth 2.4GHz systems including enhanced data rates (EDR) to 3Mbps.

With the on-chip CSR Bluetooth software stack it provides a fully compliant Bluetooth system to v2.0 of the specification for data and voice communications.



BlueCore4-ROM System Architecture

BlueCore™ 4-ROM

Single Chip Bluetooth® v2.0 System with EDR

Production Data Sheet for

BC41B143A

July 2005

Applications

- Cellular Handsets
- Personal Digital Assistants
- Digital cameras and other high volume consumer products

BlueCore4-ROM has been designed to reduce the number of external components required which ensures that production costs are minimised.

The device incorporates auto-calibration and built-in self-test (BIST) routines to simplify development, type approval and production test. All hardware and device firmware is fully compliant with the Bluetooth v2.0 Specification (all mandatory and optional features).

To improve the performance of both Bluetooth and 802.11b/g co-located systems a wide range of co-existence features are available including a variety of hardware signalling: basic activity signalling and Intel WCS activity and channel signalling.

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Status Information

The status of this Data Sheet is **Production Information**.

CSR Product Data Sheets progress according to the following format:

Advance Information

Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

Pre-production Information

Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All electrical specifications may be changed by CSR without notice.

Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

Production Data Sheets supersede all previous document versions.

RoHS Compliance

BlueCore4-ROM devices meet the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS).

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1 Key Features

Radio

- Common TX/RX terminal simplifies external matching; eliminates external antenna switch
- BIST minimises production test time. No external trimming is required in production
- Full RF reference designs available
- Bluetooth v2.0 Specification compliant
- EDR v2.0.E.2 compliant

Transmitter

- +6dBm RF transmit power with level control from on-chip 6-bit DAC over a dynamic range >30dB
- Class 2 and Class 3 support without the need for an external power amplifier or TX/RX switch
- Class1 support using external power amplifier, with RF power controlled by an internal 8-bit DAC
- Supports DQPSK (2Mbps) and 8DPSK (3Mbps) modulation

Receiver

- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real time digitised RSSI available on HCI interface
- Fast AGC for enhanced dynamic range
- Supports DQPSK and 8DPSK modulation
- Channel classification

Synthesiser

- Fully integrated synthesiser requires no external VCO, varactor diode, resonator or loop filter
- Compatible with an external crystal or with an external clock using sinusoidal or logic-level signals
- Accepts frequencies between 8 and 32MHz (in multiples of 250kHz); additionally accepts 7.68, 14.44, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz frequencies typically used in GSM and CDMA devices

Auxiliary Features

- Crystal oscillator with built-in digital trimming
- Power management includes digital shut down, wake up commands with an integrated low power oscillator for ultra-low power Park/Sniff/Hold mode
- 'Clock request' output to control an external clock

Auxiliary Features (continued)

- On-chip linear regulator; 1.8V output from a 2.2 - 4.2V input
- Clock for low power mode can be either supplied from an external 32kHz clock signal or an internal oscillator
- Auto baud rate setting for different TCXO frequencies
- Power-on-reset cell detects low supply voltage
- Arbitrary power supply sequencing permitted
- 8-bit ADC and DAC available to applications

Baseband and Software

- Internal 48Kbyte RAM, allows full speed data transfer, mixed voice and data, and full piconet operation, including all medium rate preset types
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping. Supports all Bluetooth v2.0 features including eSCO and AFH
- Transcoders for A-law, μ -law and linear voice from host and A-law, μ -law and CVSD voice over air

Physical Interfaces

- Synchronous serial interface up to 4Mbaud for system debugging
- UART interface with programmable baud rate up to 3Mbits/s with an optional bypass mode
- Full speed USB v2.0 interface supports OHCI and UHCI host interfaces
- Synchronous bi-directional serial programmable audio interface
- Optional I²C™ compatible interfaces
- Audio PCM interface
- Optional co-existence interfaces

Bluetooth Stack

CSR's Bluetooth Protocol Stack runs on the on-chip MCU in a variety of configurations:

- Standard HCI (UART or USB)
- Fully embedded RFCOMM
- Customised builds with embedded application code

Package Options

- 84-ball VFPGA, 6 x 6mm x 1mm, 0.5mm pitch

2 6 x 6mm VFBGA Package Information

2.1 BlueCore4-ROM Pinout Diagram

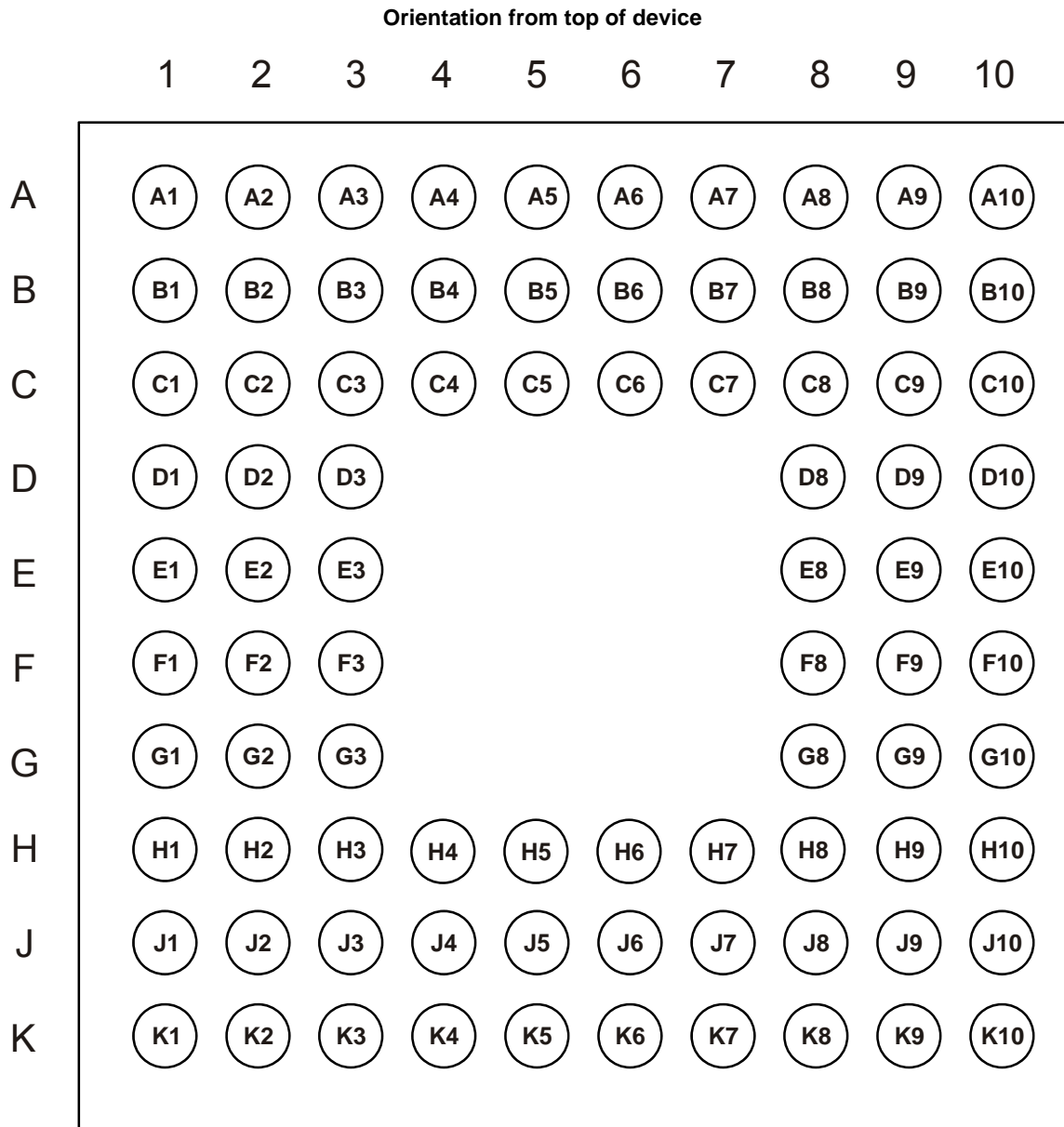


Figure 2.1: BlueCore4-ROM Device Pinout

2.2 Device Terminal Functions

Radio	Ball	Pad Type	Description
RF_IN	D1	Analogue	Single-ended receiver input
PIO[0]/RXEN	B1	Bi-directional with programmable strength internal pull-up/down	Control output for external TX/RX switch (if fitted)
PIO[1]/TXEN	B2	Bi-directional with programmable strength internal pull-up/down	Control output for external PA (if fitted)
TX_A	F1	Analogue	Transmitter output/switched receiver input
TX_B	E1	Analogue	Complement of TX_A
AUX_DAC	D3	Analogue	Voltage DAC output

Synthesiser and Oscillator	Ball	Pad Type	Description
XTAL_IN	K3	Analogue	For crystal or external clock input
XTAL_OUT	J3	Analogue	Drive for crystal

USB and UART	Ball	Pad Type	Description
UART_TX	J10	CMOS output, tri-state with weak internal pull-up	UART data output active high
UART_RX	H9	CMOS input with weak internal pull-down	UART data input active high
UART_RTS	H7	CMOS output, tri-state with weak internal pull-up	UART request to send active low
UART_CTS	H8	CMOS input with weak internal pull-down	UART clear to send active low
USB_DP	J8	Bi-directional	USB data plus with selectable internal 1.5k Ω pull-up resistor
USB_DN	K8	Bi-directional	USB data minus

PCM Interface	Ball	Pad Type	Description
PCM_OUT	G8	CMOS output, tri-state with weak internal pull-down	Synchronous data output
PCM_IN	G9	CMOS input, with weak internal pull-down	Synchronous data input
PCM_SYNC	G10	Bi-directional with weak internal pull-down	Synchronous data sync
PCM_CLK	H10	Bi-directional with weak internal pull-down	Synchronous data clock

Test and Debug	Ball	Pad Type	Description
RESET	C7	CMOS input with weak internal pull-down	Reset if high. Input debounced, so must be high for >5ms to cause a reset
RESETB	D8	CMOS input with weak internal pull-up	Reset if low. Input debounced, so must be low for >5ms to cause a reset
SPI_CSB	C9	CMOS input with weak internal pull-up	Chip select for Serial Peripheral Interface, active low
SPI_CLK	C10	CMOS input with weak internal pull-down	Serial Peripheral Interface clock
SPI_MOSI	C8	CMOS input with weak internal pull-down	Serial Peripheral Interface data input
SPI_MISO	B9	CMOS output, tri-state with weak internal pull-down	Serial Peripheral Interface data output
TEST_EN	C6	CMOS input with strong internal pull-down	For test purposes only (leave unconnected)

PIO Port	Ball	Pad Type	Description
PIO[2]	B3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[3]	B4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[4]	E8	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line or optionally BT_Priority/Ch_Clk output for co-existence signalling
PIO[5]	F8	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line or optionally BT_Active output for co-existence signalling
PIO[6]	F10	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line or optionally WLAN_Active/Ch_Data input for co-existence signalling
PIO[7]	F9	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[8]	C5	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[9]	C3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[10]	C4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[11]	E3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
AIO[0]	H4	Bi-directional	Programmable input/output line
AIO[1]	H5	Bi-directional	Programmable input/output line
AIO[2]	J5	Bi-directional	Programmable input/output line

Power Supplies and Control	Ball	Pad Type	Description
VREG_IN	K6	Linear regulator input	Linear regulator voltage input ⁽¹⁾
VREG_EN	K5	Input	High or not connected to enable active regulator. VSS to disable regulator ⁽¹⁾
VDD_USB	K9	VDD	Positive supply for UART/USB and AIO ports
VDD_PIO	A3	VDD	Positive supply for PIO and AUX DAC ⁽²⁾
VDD_PADS	D10	VDD	Positive supply for all other digital input/output ports ⁽³⁾
VDD_CORE	E10	VDD	Positive supply for internal digital circuitry
VDD_RADIO	C1, C2	VDD	Positive supply for RF circuitry
VDD_VCO	H1	VDD	Positive supply for VCO and synthesiser circuitry
VDD_ANA	K4	VDD/Linear regulator output	Positive supply for analogue circuitry and 1.8V regulated output
VSS_PADS	A1, A2, D9, J9, K10	VSS	Ground connections for input/output
VSS_CORE	E9	VSS	Ground connection for internal digital circuitry
VSS_RADIO	D2, E2, F2	VSS	Ground connections for RF circuitry
VSS_VCO	G1, G2	VSS	Ground connections for VCO and synthesiser
VSS_ANA	J2, J4, K2	VSS	Ground connections for analogue circuitry
VSS	F3	VSS	Ground connection for internal package shield

Unconnected Terminals	Ball	Description
	A4, A5, A6, A7, A8, A9, A10, B5, B6, B7, B8, B10, G3, H2, H3, H6, J1, J6, J7, K1, K7	Leave unconnected

Notes:

- (1) To enable the regulator the VREG_EN pin needs to be either pulled high or left unconnected. This keeps compatibility with BlueCore2-ROM as the corresponding pin on BlueCore2-ROM was designated as a not connect pin. In this situation the BlueCore4-ROM regulator is permanently on replicating the BlueCore2-ROM that has no regulator enable pin.
- (2) Positive supply for PIO[3:0] and PIO[11:8]
- (3) Positive supply for SPI/PCM ports and PIO[7:4]

3 Electrical Characteristics

Absolute Maximum Ratings		
Rating	Min	Max
Storage Temperature	-40°C	+150°C
Supply Voltage: VDD_RADIO, VDD_LO, VDD_ANA and VDD_CORE	-0.4V	2.2V
Supply Voltage: VDD_PADS, VDD_PIO and VDD_USB	-0.4V	3.7V
Supply Voltage: VREG_IN	-0.4V	5.6V
Other Terminal Voltages	VSS-0.4V	VDD+0.4V

Recommended Operating Conditions		
Operating Condition	Min	Max
Operating Temperature Range	-40°C	+105°C
Guaranteed RF performance range ⁽¹⁾	-40°C	+105°C
Supply Voltage: VDD_RADIO, VDD_LO, VDD_ANA and VDD_CORE	1.7V	1.9V
Supply Voltage: VDD_PADS, VDD_PIO and VDD_USB	1.7V	3.6V
Supply Voltage: VREG_IN	2.2V	4.2V ⁽²⁾

Note:

- ⁽¹⁾ Typical figures are given for RF performance between -40°C and +105°C
- ⁽²⁾ The device will operate without damage with VREG_IN as high as 5.6V, however the RF performance is not guaranteed above 4.2V

Input/Output Terminal Characteristics				
Linear Regulator	Min	Typ	Max	Unit
Normal Operation				
Output Voltage (Iload = 70 mA)	1.70	1.78	1.85	V
Temperature Coefficient	-250	-	+250	ppm/C
Output Noise ⁽¹⁾⁽²⁾	-	-	1	mV rms
Load Regulation (Iload < 100 mA)	-	-	50	mV/A
Settling Time ⁽¹⁾⁽³⁾	-	-	50	μs
Maximum Output Current	70	-	-	mA
Minimum Load Current	5	-	-	μA
Input Voltage	-	-	4.2 ⁽⁶⁾	V
Dropout Voltage (Iload = 70 mA)	-	-	350	mV
Quiescent Current (excluding load, Iload < 1mA)	25	35	50	μA
Low Power Mode⁽⁴⁾				
Quiescent Current (excluding load, Iload < 100μA)	4	7	10	μA
Disabled Mode⁽⁵⁾				
Quiescent Current	1.5	2.5	3.5	μA

Notes:

For optimum performance the VDD_ANA ball adjacent to VREG_IN should be used for regulator output.

- (1) Regulator output connected to 47nF pure and 4.7μF 2.2Ω ESR capacitors.
- (2) Frequency range 100Hz to 100kHz
- (3) 1mA to 70mA pulsed load
- (4) Low power mode is entered and exited automatically when the chip enters/leaves Deep Sleep mode.
- (5) Regulator is disabled when VREG_EN is pulled low. It is also disabled when VREG_IN is either open circuit or driven to the same voltage as VDD_ANA.
- (6) Operation up to 5.6V is permissible without damage and without the output voltage rising sufficiently to damage the rest of BlueCore4, but output regulation and other specifications are no longer guaranteed at input voltages in excess of 4.2V.

Input/Output Terminal Characteristics (Continued)					
Digital Terminals		Min	Typ	Max	Unit
Input Voltage Levels					
V _{IL} input logic level low	2.7V ≤ VDD ≤ 3.0V	-0.4	-	+0.8	V
	1.7V ≤ VDD ≤ 1.9V	-0.4	-	+0.4	V
V _{IH} input logic level high		0.7VDD	-	VDD+0.4	V
Output Voltage Levels					
V _{OL} output logic level low, (I _o = 4.0mA), 2.7V ≤ VDD ≤ 3.0V		-	-	0.2	V
V _{OL} output logic level low, (I _o = 4.0mA), 1.7V ≤ VDD ≤ 1.9V		-	-	0.4	V
V _{OH} output logic level high, (I _o = -4.0mA), 2.7V ≤ VDD ≤ 3.0V		VDD-0.2	-	-	V
V _{OH} output logic level high, (I _o = -4.0mA), 1.7V ≤ VDD ≤ 1.9V		VDD-0.4	-	-	V
Input and Tri-state Current with:					
Strong pull-up		-100	-40	-10	μA
Strong pull-down		+10	+40	+100	μA
Weak pull-up		-5.0	-1.0	-0.2	μA
Weak pull-down		+0.2	+1.0	+5.0	μA
I/O pad leakage current		-1	0	+1	μA
C _I Input Capacitance		1.0	-	5.0	pF

Input/Output Terminal Characteristics (Continued)					
USB Terminals		Min	Typ	Max	Unit
VDD_USB for correct USB operation		3.1		3.6	V
Input threshold					
V _{IL} input logic level low		-	-	0.3VDD_USB	V
V _{IH} input logic level high		0.7VDD_USB	-	-	V
Input leakage current					
VSS_PADS < V _{IN} < VDD_USB ⁽¹⁾		-1	1	5	μA
C _I Input capacitance		2.5	-	10.0	pF
Output Voltage levels to correctly terminated USB Cable					
V _{OL} output logic level low		0.0	-	0.2	V
V _{OH} output logic level high		2.8	-	VDD_USB	V

Input/Output Terminal Characteristics (Continued)				
Power-on reset	Min	Typ	Max	Unit
VDD_CORE falling threshold	1.40	1.50	1.60	V
VDD_CORE rising threshold	1.50	1.60	1.70	V
Hysteresis	0.05	0.10	0.15	V

Input/Output Terminal Characteristics (Continued)					
Auxiliary ADC	Min	Typ	Max	Unit	
Resolution	-	-	8	Bits	
Input voltage range (LSB size = VDD_ANA/255)	0	-	VDD_ANA	V	
Accuracy (Guaranteed monotonic)	INL	-1	-	1	LSB
	DNL	0	-	1	LSB
Offset	-1	-	1	LSB	
Gain Error	-0.8	-	0.8	%	
Input Bandwidth	-	100	-	kHz	
Conversion time	-	2.5	-	□s	
Sample rate ⁽²⁾	-	-	700	Samples/s	

Input/Output Terminal Characteristics (Continued)				
Auxiliary DAC	Min	Typ	Max	Unit
Resolution	-	-	8	Bits
Average output step size ⁽³⁾	12.5	14.5	17.0	mV
Output Voltage		monotonic ⁽²⁾		
Voltage range (I _o =0mA)	VSS_PADS	-	VDD_PIO	V
Current range	-10.0	-	+0.1	mA
Minimum output voltage (I _o =100μA)	0.0	-	0.2	V
Maximum output voltage (I _o =10mA)	VDD_PIO-0.3	-	VDD_PIO	V
High Impedance leakage current	-1	-	+1	μA
Offset	-220	-	+120	mV
Integral non-linearity ⁽³⁾	-2	-	+2	LSB
Settling time (50pF load)	-	-	10	μs

Input/Output Terminal Characteristics (Continued)				
Crystal Oscillator	Min	Typ	Max	Unit
Crystal frequency ⁽⁴⁾	8.0	-	32.0	MHz
Digital trim range ⁽⁵⁾	5.0	6.2	8.0	pF
Trim step size ⁽⁵⁾	-	0.1	-	pF
Transconductance	2.0	-	-	mS
Negative resistance ⁽⁶⁾	870	1500	2400	Ω
External Clock				
Input frequency ⁽⁷⁾	7.5	-	40.0	MHz
Clock input level ⁽⁸⁾	0.2	-	VDD_ANA	V pk-pk
Allowable Jitter	-	-	15	ps rms
XTAL_IN input impedance	-	-	-	k Ω
XTAL_IN input capacitance	-	7	-	pF

Notes:

VDD_CORE, VDD_RADIO, VDD_LO and VDD_ANA are at 1.8V unless shown otherwise.

VDD_PADS, VDD_PIO and VDD_USB are at 3.0V unless shown otherwise.

The same setting of the digital trim is applied to both XTAL_IN and XTAL_OUT.

Current drawn into a pin is defined as positive; current supplied out of a pin is defined as negative.

(1) Internal USB pull-up disabled

(2) Access of ADC is through VM function and therefore sample rate given is achieved as part of this function

(3) Specified for an output voltage between 0.2V and VDD_PIO -0.2V

(4) Integer multiple of 250kHz

(5) The difference between the internal capacitance at minimum and maximum settings of the internal digital trim

(6) XTAL frequency = 16MHz; XTAL C0 = 0.75pF; XTAL load capacitance = 8.5pF

(7) Clock input can be any frequency between 8 and 40MHz in steps of 250kHz and also covers the CDMA/3G TCXO frequencies of 7.68, 14.44, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz

(8) Clock input can either be sinusoidal or square wave. If the peaks of the signal are below VSS_ANA or above VDD_ANA a DC blocking capacitor is required between the signal and XTAL_IN

3.1 Power Consumption

Operation Mode	Connection Type	UART Rate (kbps)	Average	Unit
Page scan	-	115.2	0.43	mA
Inquiry & page scan	-	115.2	0.75	mA
ACL data transfer No traffic	Master	115.2	3.71	mA
ACL data transfer With file transfer	Master	115.2	8.44	mA
ACL data transfer No traffic	Slave	115.2	15.1	mA
ACL data transfer With file transfer	Slave	115.2	17.7	mA
ACL data transfer 40ms sniff	Master	115.2	1.58	mA
ACL data transfer 1.28s sniff	Master	115.2	0.14	mA
eSCO EV3 – Setting S1	Master	38.4	24.0	mA
SCO connection HV1	Master	38.4	36.3	mA
SCO connection HV3	Master	38.4	17.8	mA
SCO connection HV3 30ms sniff	Master	38.4	17.5	mA
ACL data transfer 40ms sniff	Slave	38.4	1.39	mA
ACL data transfer 1.28s sniff	Slave	38.4	0.26	mA
eSCO EV3 – Setting S1	Slave	38.4	22.7	mA
SCO connection HV1	Slave	38.4	35.7	mA
SCO connection HV3	Slave	38.4	22.7	mA
SCO connection HV3 30ms sniff	Slave	38.4	16.8	mA
Parked 1.28s beacon	Slave	38.4	0.19	mA
Standby Host connection ⁽¹⁾	-	38.4	36	μA
Reset (RESETB low) ⁽¹⁾	-	-	49	μA

Note:

Conditions: 20°C, 3.15V supply into linear regulator

- ⁽¹⁾ Low power mode on the linear regulator is entered and exited automatically when the chip enters/leaves Deep Sleep mode. For more information about the electrical characteristics of the linear regulator, see section 3 in this document.

4 Radio Characteristics – Basic Data Rate

BlueCore4-ROM meets the Bluetooth specification v2.0 + EDR when used in a suitable application circuit between -40°C and +105°C.

TX output is guaranteed to be unconditionally stable over the guaranteed temperature range.

4.1 Temperature +20°C

4.1.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +20°C					
	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power ⁽¹⁾⁽²⁾	-	4.5	-	-6 to +4 ⁽³⁾	dBm
Variation in RF power over temperature range with compensation enabled (\pm) ⁽⁴⁾	-	1.5	-	-	dB
Variation in RF power over temperature range with compensation disabled (\pm) ⁽⁴⁾	-	2.5	-	-	dB
RF power control range	-	35	-	≥ 16	dB
RF power range control resolution ⁽⁵⁾	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	780	-	≤ 1000	kHz
Adjacent channel transmit power $F=F_0 \pm 2\text{MHz}$ ⁽⁶⁾⁽⁷⁾	-	-35	-	≤ -20	dBm
Adjacent channel transmit power $F=F_0 \pm 3\text{MHz}$ ⁽⁶⁾⁽⁷⁾	-	-45	-	≤ -40	dBm
Adjacent channel transmit power $F=F_0 > \pm 3\text{MHz}$ ⁽⁶⁾⁽⁷⁾	-	<-50	-	≤ -40	dBm
$\Delta f_{1\text{avg}}$ "Maximum Modulation"	-	165	-	$140 < f_{1\text{avg}} < 175$	kHz
$\Delta f_{2\text{max}}$ "Minimum Modulation"	-	152	-	115	kHz
$\Delta f_{1\text{avg}}/\Delta f_{2\text{avg}}$	-	0.98	-	≥ 0.80	-
Initial carrier frequency tolerance	-	8	-	± 75	kHz
Drift Rate	-	7	-	≤ 20	kHz/ 50 μ s
Drift (single slot packet)	-	8	-	≤ 25	kHz
Drift (five slot packet)	-	9	-	≤ 40	kHz
2 nd Harmonic Content	-	-45	-	≤ 30	dBm
3 rd Harmonic Content	-	-50	-	≤ 30	dBm

Notes:

- (1) BlueCore4-ROM firmware maintains the transmit power to be within the Bluetooth specification v2.0 + EDR limits.
- (2) Measurement made using a PSKEY_LC_MAX_TX_POWER setting corresponds to a PSKEY_LC_POWER_TABLE power table entry of 63.
- (3) Class 2 RF transmit power range, Bluetooth specification v2.0 + EDR.
- (4) To some extent these parameters are dependent on the matching circuit used, and its behaviour over temperature. Therefore these parameters may be beyond CSR's direct control.
- (5) Resolution guaranteed over the range -5dB to -25dB relative to maximum power for TX Level >20.
- (6) Measured at $F_0 = 2441\text{MHz}$.
- (7) Up to three exceptions are allowed in v2.0 + EDR of the Bluetooth specification. BlueCore4-ROM is guaranteed to meet the ACP performance as specified by the Bluetooth specification v2.0 + EDR.

Radio Characteristics VDD = 1.8V Temperature = +20°C (Continued)						
	Frequency (GHz)	Min	Typ	Max	Cellular Band	Unit
Emitted power in cellular bands measured at the unbalanced port of the balun. Output power = 4dBm	0.869 – 0.894 ⁽¹⁾	-	-125	-	GSM 850	dBm /Hz
	0.869 – 0.894 ⁽²⁾	-	-129	-	CDMA 850	
	0.925 – 0.960 ⁽¹⁾	-	-129	-	GSM 900	
	1.570 – 1.580 ⁽³⁾	-	-135	-	GPS	
	1.805 – 1.880 ⁽¹⁾	-	-133	-	GSM 1800 / DCS 1800	
	1.930 – 1.990 ⁽⁴⁾	-	-135	-	PCS 1900	
	1.930 – 1.990 ⁽¹⁾	-	-133	-	GSM 1900	
	1.930 – 1.990 ⁽²⁾	-	-135	-	CDMA 1900	
	2.110 – 2.170 ⁽²⁾	-	-131	-	W-CDMA 2000	
	2.110 – 2.170 ⁽⁵⁾	-	-131	-	W-CDMA 2000	

Notes:

- (1) Integrated in 200kHz bandwidth and then normalised to a 1Hz bandwidth.
- (2) Integrated in 1.2MHz bandwidth and then normalised to a 1Hz bandwidth.
- (3) Integrated in 1MHz bandwidth and then normalised to a 1Hz bandwidth.
- (4) Integrated in 30kHz bandwidth and then normalised to a 1Hz bandwidth.
- (5) Integrated in 5MHz bandwidth and then normalised to a 1Hz bandwidth.

4.1.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = +20°C						
	Frequency (GHz)	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.1% BER for all packet types	2.402	-	-85.0	-	≤-70	dBm
	2.441	-	-84.0	-		
	2.480	-	-84.5	-		
Maximum received signal at 0.1% BER		-	>10	-	≥-20	dBm
	Frequency (MHz)	Min	Typ	Max	Bluetooth Specification	Unit
Continuous power required to block Bluetooth reception (for sensitivity of -67dBm with 0.1% BER) measured at the unbalanced port of the balun.	30 – 2000	-	0	-	-10	dBm
	2000 – 2400	-	-10	-	-27	
	2500 – 3000	-	0	-	-27	
C/I co-channel		-	8	-	≤11	dB
Adjacent channel selectivity C/I $F=F_0+1\text{MHz}^{(1)(2)}$		-	-6	-	≤0	dB
Adjacent channel selectivity C/I $F=F_0-1\text{MHz}^{(1)(2)}$		-	-4	-	≤0	dB
Adjacent channel selectivity C/I $F=F_0+2\text{MHz}^{(1)(2)}$		-	-38	-	≤-30	dB
Adjacent channel selectivity C/I $F=F_0-2\text{MHz}^{(1)(2)}$		-	-24	-	≤-20	dB
Adjacent channel selectivity C/I $F\geq F_0+3\text{MHz}^{(1)(2)}$		-	-45	-	≤-40	dB
Adjacent channel selectivity C/I $F\leq F_0-5\text{MHz}^{(1)(2)}$		-	-45	-	≤-40	dB
Adjacent channel selectivity C/I $F=F_{\text{image}}^{(1)(2)}$		-	-21	-	≤-9	dB
Maximum level of intermodulation interferers ⁽³⁾		-	-30	-	≥-39	dBm
Spurious output level ⁽⁴⁾		-	-160	-	-	dBm/Hz

Notes:

- (1) Up to five exceptions are allowed in v2.0 + EDR of the Bluetooth specification. BlueCore4-ROM is guaranteed to meet the C/I performance as specified by the Bluetooth specification v2.0 + EDR.
- (2) Measured at $F_0 = 2441\text{MHz}$
- (3) Measured at $f_1-f_2 = 5\text{MHz}$. Measurement is performed in accordance with Bluetooth RF test RCV/CA/05/c. i.e. wanted signal at -64dBm
- (4) Measured at the unbalanced port of the balun. Integrated in 100kHz bandwidth and then normalized to 1Hz. Actual figure is typically below -160dBm/Hz except for peaks of -65dBm at 1600MHz, -54dBm inband at 2.4GHz and -65dBm at 3.2GHz.

Radio Characteristics VDD = 1.8V Temperature = +20°C (Continued)						
	Frequency (GHz)	Min	Typ	Max	Cellular Band	Unit
Continuous power in cellular bands required to block Bluetooth reception (for sensitivity of -67dBm with 0.1% BER) measured at the unbalanced port of the balun.	0.824 – 0.849	-	0	-	GSM 850	dBm
	0.824 – 0.849	-	-10	-	CDMA	
	0.880 – 0.915	-	0	-	GSM 900	
	1.710 – 1.785	-	>0	-	GSM 1800 / DCS 1800	
	1.850 – 1.910	-	>0	-	GSM 1900 / PCS 1900	
	1.850 – 1.910	-	-12	-	CDMA 1900	
	1.920 – 1.980	-	-12	-	W-CDMA 2000	
Continuous power in cellular bands required to block Bluetooth reception (for sensitivity of -72dBm with 0.1% BER) measured at the unbalanced port of the balun.	0.824 – 0.849	-	-2	-	GSM 850	dBm
	0.824 – 0.849	-	-13	-	CDMA	
	0.880 – 0.915	-	-5	-	GSM 900	
	1.710 – 1.785	-	0	-	GSM 1800 / DCS 1800	
	1.850 – 1.910	-	0	-	GSM 1900 / PCS 1900	
	1.850 – 1.910	-	-16	-	CDMA 1900	
	1.920 – 1.980	-	-18	-	W-CDMA 2000	

4.2 Temperature -40°C

4.2.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = -40°C					
	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power ⁽¹⁾	-	5.5	-	-6 to +4 ⁽²⁾	dBm
RF power control range	-	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	780	-	≤1000	kHz
Adjacent channel transmit power $F=F_0 \pm 2\text{MHz}$ ^{(3) (4)}	-	-35	-	≤-20	dBm
Adjacent channel transmit power $F=F_0 \pm 3\text{MHz}$ ^{(3) (4)}	-	-43	-	≤-40	dBm
$\Delta f_{1\text{avg}}$ "Maximum Modulation"	-	165	-	$140 < \Delta f_{1\text{avg}} < 175$	kHz
$\Delta f_{2\text{max}}$ "Minimum Modulation"	-	154	-	≥115	kHz
$\Delta f_{2\text{avg}} / \Delta f_{1\text{avg}}$	-	0.99	-	≥0.80	-
Initial carrier frequency tolerance	-	9	-	±75	kHz
Drift Rate	-	6	-	≤20	kHz/50μs
Drift (single slot packet)	-	7	-	≤25	kHz
Drift (five slot packet)	-	9	-	≤40	kHz

Notes:

- (1) BlueCore4-ROM firmware maintains the transmit power to be within the Bluetooth specification v2.0 + EDR limits
- (2) Class 2 RF transmit power range, Bluetooth specification v2.0 + EDR.
- (3) Measured at $F_0 = 2441\text{MHz}$
- (4) Up to three exceptions are allowed in v2.0 + EDR of the Bluetooth specification

4.2.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = -40°C						
	Frequency (GHz)	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.1% BER for all packet types	2.402	-	-87.0	-	≤-70	dBm
	2.441	-	-86.5	-		
	2.480	-	-87.0	-		
Maximum received signal at 0.1% BER		-	>10	-	≥-20	dBm

4.3 Temperature -25°C

4.3.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = -25°C					
	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power ⁽¹⁾	-	5.0	-	-6 to +4 ⁽²⁾	dBm
RF power control range	-	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	780	-	≤1000	kHz
Adjacent channel transmit power $F=F_0 \pm 2\text{MHz}$ ^{(3) (4)}	-	-32	-	≤-20	dBm
Adjacent channel transmit power $F=F_0 \pm 3\text{MHz}$ ^{(3) (4)}	-	-43	-	≤-40	dBm
$\Delta f_{1\text{avg}}$ "Maximum Modulation"	-	165	-	$140 < \Delta f_{1\text{avg}} < 175$	kHz
$\Delta f_{2\text{max}}$ "Minimum Modulation"	-	152	-	≥115	kHz
$\Delta f_{2\text{avg}} / \Delta f_{1\text{avg}}$	-	0.98	-	≥0.80	-
Initial carrier frequency tolerance	-	9	-	±75	kHz
Drift Rate	-	7	-	≤20	kHz/50μs
Drift (single slot packet)	-	7	-	≤25	kHz
Drift (five slot packet)	-	9	-	≤40	kHz

Notes:

- (1) BlueCore4-ROM firmware maintains the transmit power to be within the Bluetooth specification v2.0 + EDR limits
- (2) Class 2 RF transmit power range, Bluetooth specification v2.0 + EDR.
- (3) Measured at $F_0 = 2441\text{MHz}$
- (4) Up to three exceptions are allowed in v2.0 + EDR of the Bluetooth specification

4.3.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = -25°C						
	Frequency (GHz)	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.1% BER for all packet types	2.402	-	-86.5	-	≤-70	dBm
	2.441	-	-86.0	-		
	2.480	-	-86.5	-		
Maximum received signal at 0.1% BER		-	10	-	≥-20	dBm

4.4 Temperature +85°C

4.4.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +85°C					
	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power ⁽¹⁾	-	2.0	-	-6 to +4 ⁽²⁾	dBm
RF power control range	-	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	800	-	≤1000	kHz
Adjacent channel transmit power $F=F_0 \pm 2\text{MHz}$ ^{(3) (4)}	-	-38	-	≤-20	dBm
Adjacent channel transmit power $F=F_0 \pm 3\text{MHz}$ ^{(3) (4)}	-	-45	-	≤-40	dBm
$\Delta f_{1\text{avg}}$ "Maximum Modulation"	-	165	-	$140 < \Delta f_{1\text{avg}} < 175$	kHz
$\Delta f_{2\text{max}}$ "Minimum Modulation"	-	150	-	≥115	kHz
$\Delta f_{2\text{avg}} / \Delta f_{1\text{avg}}$	-	0.96	-	≥0.80	-
Initial carrier frequency tolerance	-	8	-	±75	kHz
Drift Rate	-	8	-	≤20	kHz/50μs
Drift (single slot packet)	-	8	-	≤25	kHz
Drift (five slot packet)	-	9	-	≤40	kHz

Notes:

- (1) BlueCore4-ROM firmware maintains the transmit power to be within the Bluetooth specification v2.0 + EDR limits
- (2) Class 2 RF transmit power range, Bluetooth specification v2.0 + EDR.
- (3) Measured at $F_0 = 2441\text{MHz}$
- (4) Up to three exceptions are allowed in v2.0 + EDR of the Bluetooth specification

4.4.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = +85°C						
	Frequency (GHz)	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.1% BER for all packet types	2.402	-	-81.5	-	≤-70	dBm
	2.441	-	-81.0	-		
	2.480	-	-81.5	-		
Maximum received signal at 0.1% BER		-	10	-	≥-20	dBm

4.5 Temperature +105°C

4.5.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +105°C					
	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power ⁽¹⁾	-	0.0	-	-6 to +4 ⁽²⁾	dBm
RF power control range	-	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	840	-	≤1000	kHz
Adjacent channel transmit power $F=F_0 \pm 2\text{MHz}$ ^{(3) (4)}	-	-40	-	≤-20	dBm
Adjacent channel transmit power $F=F_0 \pm 3\text{MHz}$ ^{(3) (4)}	-	-43	-	≤-40	dBm
$\Delta f_{1\text{avg}}$ "Maximum Modulation"	-	165	-	$140 < \Delta f_{1\text{avg}} < 175$	kHz
$\Delta f_{2\text{max}}$ "Minimum Modulation"	-	145	-	≥115	kHz
$\Delta f_{2\text{avg}} / \Delta f_{1\text{avg}}$	-	0.95	-	≥0.80	-
Initial carrier frequency tolerance	-	8	-	±75	kHz
Drift Rate	-	7	-	≤20	kHz/50µs
Drift (single slot packet)	-	8	-	≤25	kHz
Drift (five slot packet)	-	9	-	≤40	kHz

Notes:

- (1) BlueCore4-ROM firmware maintains the transmit power to be within the Bluetooth specification v2.0 + EDR limits.
- (2) Class 2 RF transmit power range, Bluetooth specification v2.0 + EDR.
- (3) Measured at $F_0 = 2441\text{MHz}$.
- (4) Up to three exceptions are allowed in v2.0 + EDR of the Bluetooth specification.

4.5.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = +105°C						
	Frequency (GHz)	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.1% BER for all packet types	2.402	-	-80.5	-	≤-70	dBm
	2.441	-	-80.0	-		
	2.480	-	-80.5	-		
Maximum received signal at 0.1% BER		-	10	-	≥20	dBm

5 Radio Characteristics – Enhanced Data Rate

5.1 Temperature +20°C

5.1.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +20°C						
		Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power ⁽¹⁾		-	1.5	-	-6 to +4 ⁽²⁾	dBm
Relative transmit power ⁽³⁾		-	-1.2	-	-4 to +1	dB
$\pi/4$ DQPSK Max carrier frequency stability ⁽³⁾ w_0		-	2	-	$\leq \pm 10$ for all blocks	kHz
$\pi/4$ DQPSK Max carrier frequency stability ⁽³⁾ w_i		-	6	-	$\leq \pm 75$ for all packets	kHz
$\pi/4$ DQPSK Max carrier frequency stability ⁽³⁾ $ w_0 + w_i $		-	8	-	$\leq \pm 75$ for all blocks	kHz
8DPSK Max carrier frequency stability ⁽³⁾ w_0		-	2	-	$\leq \pm 10$ for all blocks	kHz
8DPSK Max carrier frequency stability ⁽³⁾ w_i		-	6	-	$\leq \pm 75$ for all packets	kHz
8DPSK Max carrier frequency stability ⁽³⁾ $ w_0 + w_i $		-	8	-	$\leq \pm 75$ for all blocks	kHz
$\pi/4$ DQPSK Modulation Accuracy ⁽³⁾⁽⁴⁾	RMS DEVM	-	7	-	≤ 20	%
	99% DEVM	-	13	-	≤ 30	%
	Peak DEVM	-	19	-	≤ 35	%
8DPSK Modulation Accuracy ⁽³⁾⁽⁴⁾	RMS DEVM	-	7	-	≤ 13	%
	99% DEVM	-	13	-	≤ 20	%
	Peak DEVM	-	17	-	≤ 25	%
In-band spurious emissions ⁽⁵⁾	$F > F_0 + 3\text{MHz}$	-	<-50	-	≤ -40	dBm
	$F < F_0 - 3\text{MHz}$	-	<-50	-	≤ -40	dBm
	$F = F_0 - 3\text{MHz}$	-	-46	-	≤ -40	dBm
	$F = F_0 - 2\text{MHz}$	-	-34	-	≤ -20	dBm
	$F = F_0 - 1\text{MHz}$	-	-35	-	≤ -26	dB
	$F = F_0 + 1\text{MHz}$	-	-35	-	≤ -26	dB
	$F = F_0 + 2\text{MHz}$	-	-31	-	≤ -20	dBm
$F = F_0 + 3\text{MHz}$ ⁽⁵⁾	-	-33	-	≤ -40	dBm	
EDR Differential Phase Encoding		-	No errors	-	≥ 99	%

Notes:

- (1) BlueCore4-ROM firmware maintains the transmit power to be within the Bluetooth v2.0 + EDR specification limits.

- (2) Class 2 RF transmit power range, Bluetooth v2.0 + EDR specification.
- (3) Measurements methods are in accordance with the EDR RF Test Specification v2.0.E.2.
- (4) Modulation accuracy utilises differential error vector magnitude (DEVm) with tracking of the carrier frequency drift.
- (5) The Bluetooth specification values are for 8DPSK modulation. Up to three exceptions are allowed in the Bluetooth v2.0 + EDR specification. BlueCore4 is guaranteed to meet the ACP performance as specified by the Bluetooth v2.0 + EDR specification.

5.1.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = +20°C						
	Modulation	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.01% BER ⁽¹⁾	$\pi/4$ DQPSK	-	-87	-	≤ -70	dBm
	8DPSK	-	-78	-	≤ -70	dBm
Maximum received signal at 0.1% BER ⁽¹⁾	$\pi/4$ DQPSK	-	-8	-	≥ -20	dBm
	8DPSK	-	-10	-	≥ -20	dBm
C/I co-channel at 0.1% BER ⁽¹⁾	$\pi/4$ DQPSK	-	10	-	$\leq +13$	dB
	8DPSK	-	19	-	$\leq +21$	dB
Adjacent channel selectivity C/I $F=F_0 + 1\text{MHz}$ ⁽¹⁾⁽²⁾⁽³⁾	$\pi/4$ DQPSK	-	-10	-	≤ 0	dB
	8DPSK	-	-5	-	$\leq +5$	dB
Adjacent channel selectivity C/I $F=F_0 - 1\text{MHz}$ ⁽¹⁾⁽²⁾⁽³⁾	$\pi/4$ DQPSK	-	-11	-	≤ 0	dB
	8DPSK	-	-5	-	$\leq +5$	dB
Adjacent channel selectivity C/I $F=F_0 + 2\text{MHz}$ ⁽¹⁾⁽²⁾⁽³⁾	$\pi/4$ DQPSK	-	-40	-	≤ -30	dB
	8DPSK	-	-40	-	≤ -25	dB
Adjacent channel selectivity C/I $F=F_0 - 2\text{MHz}$ ⁽¹⁾⁽²⁾⁽³⁾	$\pi/4$ DQPSK	-	-23	-	≤ -20	dB
	8DPSK	-	-20	-	≤ -13	dB
Adjacent channel selectivity C/I $F \geq F_0 + 3\text{MHz}$ ⁽¹⁾⁽²⁾⁽³⁾	$\pi/4$ DQPSK	-	-45	-	≤ -40	dB
	8DPSK	-	-45	-	≤ -33	dB
Adjacent channel selectivity C/I $F \leq F_0 - 5\text{MHz}$ ⁽¹⁾⁽²⁾⁽³⁾	$\pi/4$ DQPSK	-	-45	-	≤ -40	dB
	8DPSK	-	-45	-	≤ -33	dB
Adjacent channel selectivity C/I $F=F_{\text{image}}$ ⁽¹⁾⁽²⁾⁽³⁾	$\pi/4$ DQPSK	-	-20	-	≤ -7	dB
	8DPSK	-	-15	-	≤ 0	dB

Notes:

- (1) Measurements methods are in accordance with the EDR RF Test Specification v2.0.E.2
- (2) Up to five exceptions are allowed in EDR RF Test Specification v2.0.E.2. BlueCore4-ROM is guaranteed to meet the C/I performance as specified by the EDR RF Test Specification v2.0.E.2.
- (3) Measured at $F_0 = 2405\text{MHz}, 2441\text{MHz}, 2477\text{MHz}$

5.2 Temperature -40°C

5.2.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = -40°C						
	Min	Typ	Max	Bluetooth Specification	Unit	
Maximum RF transmit power ⁽¹⁾	-	4	-	-6 to +4 ⁽²⁾		dBm
Relative transmit power ⁽³⁾	-	-1.2	-	-4 to +1		dB
$\pi/4$ DQPSK Max carrier frequency stability ⁽³⁾ w_0	-	2	-	$\leq \pm 10$ for all blocks		kHz
$\pi/4$ DQPSK Max carrier frequency stability ⁽³⁾ w_i	-	7	-	$\leq \pm 75$ for all packets		kHz
$\pi/4$ DQPSK Max carrier frequency stability ⁽³⁾ $ w_0 + w_i $	-	8	-	$\leq \pm 75$ for all blocks		kHz
8DPSK Max carrier frequency stability ⁽³⁾ w_0	-	3	-	$\leq \pm 10$ for all blocks		kHz
8DPSK Max carrier frequency stability ⁽³⁾ w_i	-	7	-	$\leq \pm 75$ for all packets		kHz
8DPSK Max carrier frequency stability ⁽³⁾ $ w_0 + w_i $	-	9	-	$\leq \pm 75$ for all blocks		kHz
$\pi/4$ DQPSK Modulation Accuracy ⁽³⁾⁽⁴⁾	RMS DEVM	-	7	-	≤ 20	%
	99% DEVM	-	14	-	≤ 30	%
	Peak DEVM	-	19	-	≤ 35	%
8DPSK Modulation Accuracy ⁽³⁾⁽⁴⁾	RMS DEVM	-	6	-	≤ 13	%
	99% DEVM	-	12	-	≤ 20	%
	Peak DEVM	-	18	-	≤ 25	%
In-band spurious emissions ⁽⁵⁾	$F > F_0 + 3\text{MHz}$	-	< -50	-	≤ -40	dBm
	$F < F_0 - 3\text{MHz}$	-	< -50	-	≤ -40	dBm
	$F = F_0 - 3\text{MHz}$	-	-42	-	≤ -40	dBm
	$F = F_0 - 2\text{MHz}$	-	-25	-	≤ -20	dBm
	$F = F_0 - 1\text{MHz}$	-	-32	-	≤ -26	dB
	$F = F_0 + 1\text{MHz}$	-	-33	-	≤ -26	dB
	$F = F_0 + 2\text{MHz}$	-	-25	-	≤ -20	dBm
$F = F_0 + 3\text{MHz}$ ⁽⁵⁾	-	-30	-	≤ -40	dBm	
EDR Differential Phase Encoding	-	No errors	-	≥ 99		%

Notes:

- (1) BlueCore4-ROM firmware maintains the transmit power to be within the Bluetooth v2.0 + EDR specification limits.
- (2) Class 2 RF transmit power range, Bluetooth v2.0 + EDR specification.
- (3) Measurements methods are in accordance with the EDR RF Test Specification v2.0.E.2.

- (4) Modulation accuracy utilises differential error vector magnitude (DEVM) with tracking of the carrier frequency drift.
- (5) The Bluetooth specification values are for 8DPSK modulation. Up to three exceptions are allowed in the Bluetooth v2.0 + EDR specification. BlueCore4 is guaranteed to meet the ACP performance as specified by the Bluetooth v2.0 + EDR specification.

5.2.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = -40°C						
	Modulation	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.01% BER ⁽¹⁾	$\pi/4$ DQPSK	-	-89	-	≤ -70	dBm
	8DPSK	-	-79	-	≤ -70	dBm
Maximum received signal at 0.1% BER ⁽¹⁾	$\pi/4$ DQPSK	-	-12	-	≥ -20	dBm
	8DPSK	-	-15	-	≥ -20	dBm

Notes:

- (1) Measurements methods are in accordance with the EDR RF Test Specification v2.0.E.2

5.3 Temperature -25°C

5.3.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = -25°C						
	Min	Typ	Max	Bluetooth Specification	Unit	
Maximum RF transmit power ⁽¹⁾	-	3	-	-6 to +4 ⁽²⁾	dBm	
Relative transmit power ⁽³⁾	-	-1.2	-	-4 to +1	dB	
$\pi/4$ DQPSK Max carrier frequency stability ⁽³⁾ w_0	-	2	-	$\leq \pm 10$ for all blocks	kHz	
$\pi/4$ DQPSK Max carrier frequency stability ⁽³⁾ w_i	-	6	-	$\leq \pm 75$ for all packets	kHz	
$\pi/4$ DQPSK Max carrier frequency stability ⁽³⁾ $ w_0 + w_i $	-	8	-	$\leq \pm 75$ for all blocks	kHz	
8DPSK Max carrier frequency stability ⁽³⁾ w_0	-	2	-	$\leq \pm 10$ for all blocks	kHz	
8DPSK Max carrier frequency stability ⁽³⁾ w_i	-	6	-	$\leq \pm 75$ for all packets	kHz	
8DPSK Max carrier frequency stability ⁽³⁾ $ w_0 + w_i $	-	8	-	$\leq \pm 75$ for all blocks	kHz	
$\pi/4$ DQPSK Modulation Accuracy ⁽³⁾⁽⁴⁾	RMS DEVM	-	6	-	≤ 20	%
	99% DEVM	-	13	-	≤ 30	%
	Peak DEVM	-	16	-	≤ 35	%
8DPSK Modulation Accuracy ⁽³⁾⁽⁴⁾	RMS DEVM	-	6	-	≤ 13	%
	99% DEVM	-	11	-	≤ 20	%
	Peak DEVM	-	16	-	≤ 25	%
In-band spurious emissions ⁽⁵⁾	$F > F_0 + 3\text{MHz}$	-	< -50	-	≤ -40	dBm
	$F < F_0 - 3\text{MHz}$	-	< -50	-	≤ -40	dBm
	$F = F_0 - 3\text{MHz}$	-	-43	-	≤ -40	dBm
	$F = F_0 - 2\text{MHz}$	-	-29	-	≤ -20	dBm
	$F = F_0 - 1\text{MHz}$	-	-32	-	≤ -26	dB
	$F = F_0 + 1\text{MHz}$	-	-33	-	≤ -26	dB
	$F = F_0 + 2\text{MHz}$	-	-27	-	≤ -20	dBm
$F = F_0 + 3\text{MHz}$ ⁽⁵⁾	-	-31	-	≤ -40	dBm	
EDR Differential Phase Encoding	-	No errors	-	≥ 99	%	

Notes:

- (1) BlueCore4-ROM firmware maintains the transmit power to be within the Bluetooth v2.0 + EDR specification limits.
- (2) Class 2 RF transmit power range, Bluetooth v2.0 + EDR specification.
- (3) Measurements methods are in accordance with the EDR RF Test Specification v2.0.E.2.

- (4) Modulation accuracy utilises differential error vector magnitude (DEVM) with tracking of the carrier frequency drift.
- (5) The Bluetooth specification values are for 8DPSK modulation. Up to three exceptions are allowed in the Bluetooth v2.0 + EDR specification. BlueCore4 is guaranteed to meet the ACP performance as specified by the Bluetooth v2.0 + EDR specification.

5.3.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = -25°C						
	Modulation	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.01% BER ⁽¹⁾	$\pi/4$ DQPSK	-	-85	-	≤ -70	dBm
	8DPSK	-	-79	-	≤ -70	dBm
Maximum received signal at 0.1% BER ⁽¹⁾	$\pi/4$ DQPSK	-	-12	-	≥ -20	dBm
	8DPSK	-	-15	-	≥ -20	dBm

Notes:

- (1) Measurements methods are in accordance with the EDR RF Test Specification v2.0.E.2

5.4 Temperature +85°C

5.4.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +85°C						
	Min	Typ	Max	Bluetooth Specification	Unit	
Maximum RF transmit power ⁽¹⁾	-	-3	-	-6 to +4 ⁽²⁾	dBm	
Relative transmit power ⁽³⁾	-	-1.2	-	-4 to +1	dB	
$\pi/4$ DQPSK Max carrier frequency stability ⁽³⁾ w_0	-	2	-	$\leq \pm 10$ for all blocks	kHz	
$\pi/4$ DQPSK Max carrier frequency stability ⁽³⁾ w_i	-	7	-	$\leq \pm 75$ for all packets	kHz	
$\pi/4$ DQPSK Max carrier frequency stability ⁽³⁾ $ w_0 + w_i $	-	9	-	$\leq \pm 75$ for all blocks	kHz	
8DPSK Max carrier frequency stability ⁽³⁾ w_0	-	2	-	$\leq \pm 10$ for all blocks	kHz	
8DPSK Max carrier frequency stability ⁽³⁾ w_i	-	7	-	$\leq \pm 75$ for all packets	kHz	
8DPSK Max carrier frequency stability ⁽³⁾ $ w_0 + w_i $	-	9	-	$\leq \pm 75$ for all blocks	kHz	
$\pi/4$ DQPSK Modulation Accuracy ⁽³⁾⁽⁴⁾	RMS DEVM	-	6	-	≤ 20	%
	99% DEVM	-	13	-	≤ 30	%
	Peak DEVM	-	16	-	≤ 35	%
8DPSK Modulation Accuracy ⁽³⁾⁽⁴⁾	RMS DEVM	-	6	-	≤ 13	%
	99% DEVM	-	11	-	≤ 20	%
	Peak DEVM	-	16	-	≤ 25	%
In-band spurious emissions ⁽⁵⁾	$F > F_0 + 3\text{MHz}$	-	< -50	-	≤ -40	dBm
	$F < F_0 - 3\text{MHz}$	-	< -50	-	≤ -40	dBm
	$F = F_0 - 3\text{MHz}$	-	-43	-	≤ -40	dBm
	$F = F_0 - 2\text{MHz}$	-	-29	-	≤ -20	dBm
	$F = F_0 - 1\text{MHz}$	-	-32	-	≤ -26	dB
	$F = F_0 + 1\text{MHz}$	-	-33	-	≤ -26	dB
	$F = F_0 + 2\text{MHz}$	-	-27	-	≤ -20	dBm
$F = F_0 + 3\text{MHz}$ ⁽⁵⁾	-	-31	-	≤ -40	dBm	
EDR Differential Phase Encoding	-	No errors	-	≥ 99	%	

Notes:

- (1) BlueCore4-ROM firmware maintains the transmit power to be within the Bluetooth v2.0 + EDR specification limits.
- (2) Class 2 RF transmit power range, Bluetooth v2.0 + EDR specification.
- (3) Measurements methods are in accordance with the EDR RF Test Specification v2.0.E.2.
- (4) Modulation accuracy utilises differential error vector magnitude (DEVM) with tracking of the carrier frequency drift.

- ⁽⁵⁾ The Bluetooth specification values are for 8DPSK modulation. Up to three exceptions are allowed in the Bluetooth v2.0 + EDR specification. BlueCore4 is guaranteed to meet the ACP performance as specified by the Bluetooth v2.0 + EDR specification.

5.4.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = +85°C						
	Modulation	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.01% BER ⁽¹⁾	$\pi/4$ DQPSK	-	-85	-	≤ -70	dBm
	8DPSK	-	-74	-	≤ -70	dBm
Maximum received signal at 0.1% BER ⁽¹⁾	$\pi/4$ DQPSK	-	-5	-	≥ -20	dBm
	8DPSK	-	-5	-	≥ -20	dBm

Notes:

- ⁽¹⁾ Measurements methods are in accordance with the EDR RF Test Specification v2.0.E.2

5.5 Temperature +105°C

5.5.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +105°C						
	Min	Typ	Max	Bluetooth Specification	Unit	
Maximum RF transmit power ⁽¹⁾	-	-4	-	-6 to +4 ⁽²⁾	dBm	
Relative transmit power ⁽³⁾	-	-1.3	-	-4 to +1	dB	
$\pi/4$ DQPSK Max carrier frequency stability ⁽³⁾ w_0	-	1	-	$\leq \pm 10$ for all blocks	kHz	
$\pi/4$ DQPSK Max carrier frequency stability ⁽³⁾ w_i	-	7	-	$\leq \pm 75$ for all packets	kHz	
$\pi/4$ DQPSK Max carrier frequency stability ⁽³⁾ $ w_0 + w_i $	-	8	-	$\leq \pm 75$ for all blocks	kHz	
8DPSK Max carrier frequency stability ⁽³⁾ w_0	-	1	-	$\leq \pm 10$ for all blocks	kHz	
8DPSK Max carrier frequency stability ⁽³⁾ w_i	-	7	-	$\leq \pm 75$ for all packets	kHz	
8DPSK Max carrier frequency stability ⁽³⁾ $ w_0 + w_i $	-	8	-	$\leq \pm 75$ for all blocks	kHz	
$\pi/4$ DQPSK Modulation Accuracy ⁽³⁾⁽⁴⁾	RMS DEVM	-	7	-	≤ 20	%
	99% DEVM	-	12	-	≤ 30	%
	Peak DEVM	-	16	-	≤ 35	%
8DPSK Modulation Accuracy ⁽³⁾⁽⁴⁾	RMS DEVM	-	7	-	≤ 13	%
	99% DEVM	-	12	-	≤ 20	%
	Peak DEVM	-	15	-	≤ 25	%
In-band spurious emissions ⁽⁵⁾	$F > F_0 + 3\text{MHz}$	-	< -50	-	≤ -40	dBm
	$F < F_0 - 3\text{MHz}$	-	< -50	-	≤ -40	dBm
	$F = F_0 - 3\text{MHz}$	-	-51	-	≤ -40	dBm
	$F = F_0 - 2\text{MHz}$	-	-45	-	≤ -20	dBm
	$F = F_0 - 1\text{MHz}$	-	-37	-	≤ -26	dB
	$F = F_0 + 1\text{MHz}$	-	-32	-	≤ -26	dB
	$F = F_0 + 2\text{MHz}$	-	-37	-	≤ -20	dBm
$F = F_0 + 3\text{MHz}$ ⁽⁵⁾	-	-38	-	≤ -40	dBm	
EDR Differential Phase Encoding	-	No errors	-	≥ 99	%	

Notes:

- (1) BlueCore4-ROM firmware maintains the transmit power to be within the Bluetooth v2.0 + EDR specification limits.
- (2) Class 2 RF transmit power range, Bluetooth v2.0 + EDR specification.
- (3) Measurements methods are in accordance with the EDR RF Test Specification v2.0.E.2.

- (4) Modulation accuracy utilises differential error vector magnitude (DEVM) with tracking of the carrier frequency drift.
- (5) The Bluetooth specification values are for 8DPSK modulation. Up to three exceptions are allowed in the Bluetooth v2.0 + EDR specification. BlueCore4 is guaranteed to meet the ACP performance as specified by the Bluetooth v2.0 + EDR specification.

5.5.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = +105°C						
	Modulation	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.01% BER ⁽¹⁾	$\pi/4$ DQPSK	-	-85	-	≤ -70	dBm
	8DPSK	-	-73	-	≤ -70	dBm
Maximum received signal at 0.1% BER ⁽¹⁾	$\pi/4$ DQPSK	-	-5	-	≥ -20	dBm
	8DPSK	-	-5	-	≥ -20	dBm

Notes:

- (1) Measurements methods are in accordance with the EDR RF Test Specification v2.0.E.2

6 Device Diagram

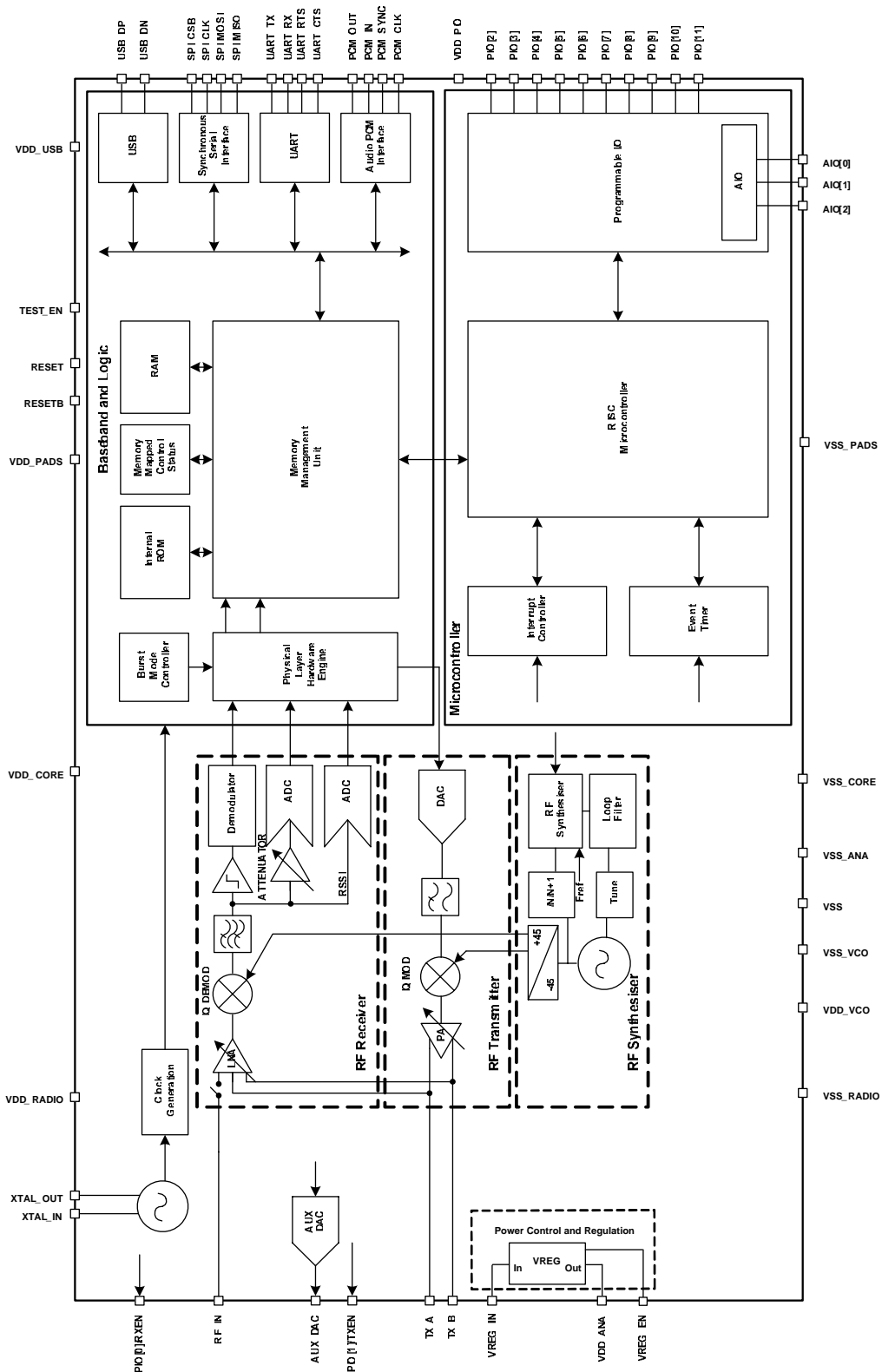


Figure 6.1: BlueCore4-ROM Device Diagram

7 Description of Functional Blocks

7.1 RF Receiver

The receiver features a near-zero Intermediate Frequency (IF) architecture that allows the channel filters to be integrated on to the die. Sufficient out-of-band blocking specification at the Low Noise Amplifier (LNA) input allows the radio to be used in close proximity to Global System for Mobile Communications (GSM) and Wideband Code Division Multiple Access (W-CDMA) cellular phone transmitters without being desensitised. The use of a digital Frequency Shift Keying (FSK) discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore4-ROM to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

For EDR, an ADC is used to digitise the IF received signal.

7.1.1 Low Noise Amplifier

The LNA can be configured to operate in single-ended or differential mode. Single-ended mode is used for Class 1 Bluetooth operation; differential mode is used for Class 2 operation.

7.1.2 Analogue to Digital Converter

The Analogue to Digital Converter (ADC) is used to implement fast Automatic Gain Control (AGC). The ADC samples the Received Signal Strength Indicator (RSSI) voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

7.2 RF Transmitter

7.2.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise the frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

7.2.2 Power Amplifier

The internal Power Amplifier (PA) has a maximum output power of +6dBm allowing BlueCore4-ROM to be used in Class 2 and Class 3 radios without an external RF PA. Support for transmit power control allows a simple implementation for Class 1 with an external RF PA.

7.2.3 Auxiliary DAC

An 8-bit voltage Auxiliary DAC is provided for power control of an external PA for Class 1 operation.

7.3 RF Synthesiser

The radio synthesiser is fully integrated onto the die with no requirement for an external Voltage Controlled Oscillator (VCO) screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth specification v2.0 + EDR.

7.4 Power Control and Regulation

BlueCore4-ROM contains a 1.8V linear regulator which can be used to power the complete chip.

7.5 Clock Input and Generation

The reference clock for the system is generated from a TCXO or crystal input between 8 and 40MHz. All internal reference clocks are generated using a phase locked loop, which is locked to the external reference frequency.

7.6 Baseband and Logic

7.6.1 Memory Management Unit

The Memory Management Unit (MMU) provides a number of dynamically allocated ring buffers that hold the data which is in transit between the host and the air. The dynamic allocation of memory ensures efficient use of the available Random Access Memory (RAM) and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

7.6.2 Burst Mode Controller

During radio transmission the Burst Mode Controller (BMC) constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During radio reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

7.6.3 Physical Layer Hardware Engine DSP

Dedicated logic is used to perform the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

The following voice data translations and operations are performed by firmware:

- A-law/ μ -law/linear voice data (from host)
- A-law/ μ -law/Continuously Variable Slope Delta (CVSD) (over the air)
- Voice interpolation for lost packets
- Rate mismatches

The hardware supports all optional and mandatory features of Bluetest v1.2 including AFH and eSCO.

7.6.4 RAM

48Kbytes of on-chip RAM is provided to support the RISC MCU and is shared between the ring buffers used to hold voice/data for each active connection and the general purpose memory required by the Bluetooth stack.

7.6.5 ROM

4Mbits of metal programmable ROM is provided for system firmware implementation.

7.6.6 USB

This is a full speed Universal Serial Bus (USB) interface for communicating with other compatible digital devices. BlueCore4-ROM acts as a USB peripheral, responding to requests from a Master host controller such as a PC.

7.6.7 Synchronous Serial Interface

This is a synchronous serial port interface (SPI) for interfacing with other digital devices. The SPI port can be used for system debugging. It can also be used for programming the Flash memory.

7.6.8 UART

This is a standard Universal Asynchronous Receiver Transmitter (UART) interface for communicating with other serial devices.

7.6.9 Audio PCM Interface

The Audio Pulse Code Modulation (PCM) Interface supports continuous transmission and reception of PCM encoded audio data over Bluetooth.

7.7 Microcontroller

The microcontroller (MCU), interrupt controller and event timer run the Bluetooth software stack and control the radio and host interfaces. A 16-bit reduced instruction set computer (RISC) microcontroller is used for low power consumption and efficient use of memory.

7.7.1 Programmable I/O

BlueCore4-ROM has a total of 15 (12 digital and 3 analogue) programmable I/O terminals. These are controlled by firmware running on the device.

7.7.2 802.11 Coexistence Interface

Dedicated hardware is provided to implement a variety of coexistence schemes. Channel skipping AFH, priority signalling, channel signalling and host passing of channel instructions are all supported. The features are configured in firmware. Since the details of some methods are proprietary (e.g. Intel WCS) please contact CSR for details.

8 CSR Bluetooth Software Stacks

BlueCore4-ROM is supplied with Bluetooth v2.0 compliant stack firmware, which runs on the internal RISC microcontroller.

The BlueCore4-ROM software architecture allows Bluetooth processing and the application program to be shared in different ways between the internal RISC microcontroller and an external host processor (if any). The upper layers of the Bluetooth stack (above HCI) can be run either on-chip or on the host processor.

8.1 BlueCore HCI Stack

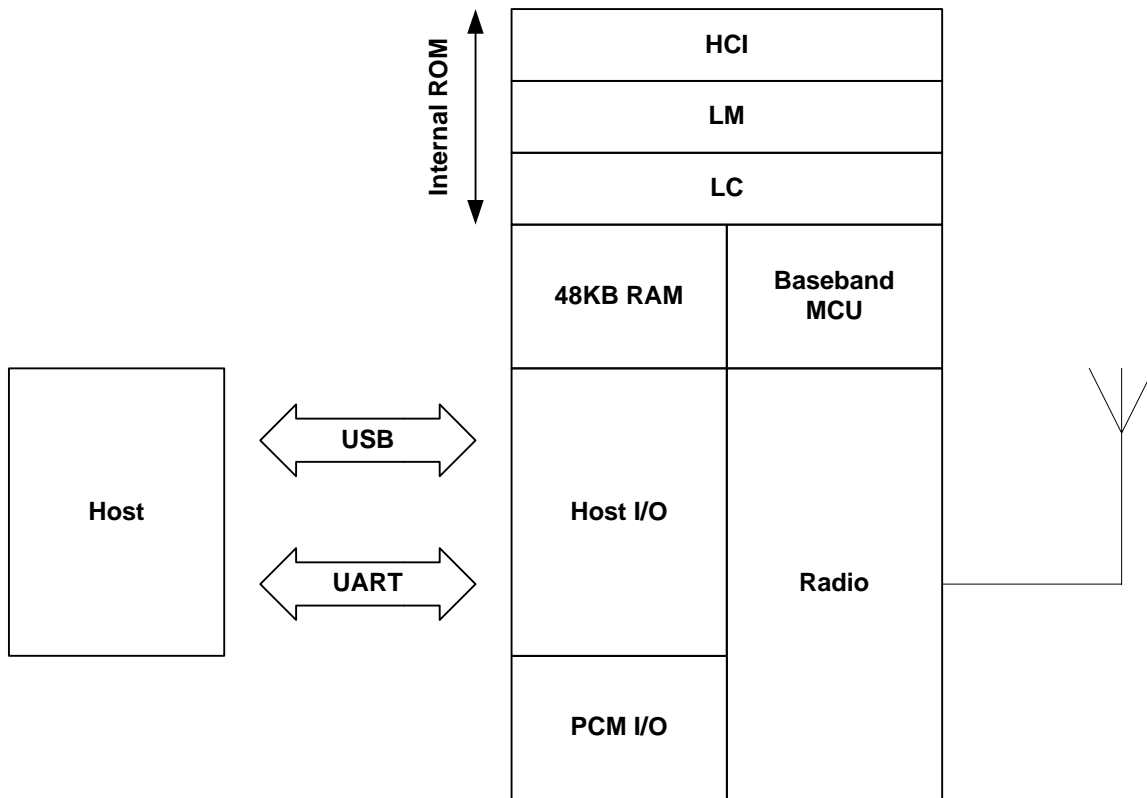


Figure 8.1: BlueCore HCI Stack

In the implementation shown in Figure 8.1 the internal processor runs the Bluetooth stack up to the Host Controller Interface (HCI). The Host processor must provide all upper layers including the application.

8.1.1 Key Features of the HCI Stack – Standard Bluetooth Functionality

Bluetooth v2.0 Mandatory Functionality:

- Adaptive frequency hopping (AFH), including Packet Loss Rate (PLR) and RSSI classification.
- Faster connections
- Flow and flush timeout
- LMP improvements
- Parameter ranges

Optional v2.0 functionality supported:

- Extended SCO (eSCO), eV3, eV4 and eV5
- Quality of Service and SCO handle
- L2CAP flow and error control
- Synchronisation

The firmware has been written against the Bluetooth v2.0 + EDR Specification.

- Bluetooth components:
 - Baseband (including LC)
 - LM
 - HCI
- Standard USB v1.1 and UART HCI Transport Layers
- All standard radio packet types
- Full Bluetooth data rate, enhanced data rates of 2 and 3Mbps(1)
- Operation with up to 7 active slaves(1)
- Operation as slave to one master while master of several slaves (Scatternet “2.0”)
- Page and Inquiry scanning while slave and master (Scatternet “2.5”)
- Maximum number of simultaneous active ACL connections: 7(2)
- Maximum number of simultaneous active SCO connections: 3(2)
- Operation with up to 3 SCO links, routed to one or more slaves
- All standard SCO voice coding
- Standard operating modes: page, inquiry, page-scan and inquiry-scan
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanisms: Hold, Sniff and Park modes, including “Forced Hold”
- Dynamic control of peers’ transmit power via LMP
- Master/Slave switch
- Broadcast
- Channel quality driven data rate
- All standard Bluetooth Test Modes
- Standard firmware upgrade via USB (DFU)

The firmware's supported Bluetooth features are detailed in the standard Protocol Implementation Conformance Statement (PICS) documents, available from <http://www.csr.com>

Note:

- (1) Supports basic data rate up to 723.2kbps asymmetric, maximum allowed by Bluetooth v2.0 + EDR specification
- (2) BlueCore4-Audio ROM supports all combinations of active ACL and SCO channels for both Master and Slave operation, as specified by the Bluetooth v2.0 + EDR specification

8.1.2 Key Features of the HCI Stack – Extra Functionality

The firmware extends the standard Bluetooth functionality with the following features:

- Supports BlueCore Serial Protocol (BCSP) – a proprietary, reliable alternative to the standard Bluetooth UART Host Transport
- Provides a set of approximately 50 manufacturer-specific HCI extension commands. This command set (called BCCMD – “BlueCore Command”), provides:
 - Access to the chip's general-purpose PIO port
 - The negotiated effective encryption key length on established Bluetooth links
 - Access to the firmware's random number generator
- Controls to set the default and maximum transmit powers – these can help minimise interference between overlapping, fixed-location piconets
- Dynamic UART configuration
- Radio transmitter enable/disable – a simple command connects to a dedicated hardware switch that determines whether the radio can transmit
- The firmware can read the voltage on a pair of the chip's external pins. This is normally used to build a battery monitor, using either VM or host code
- A block of BCCMD commands provides access to the chip's “persistent store” configuration database (PS). The database sets the device's Bluetooth address, Class of Device, radio (transmit class) configuration, SCO routing, LM, USB and DFU constants, etc.
- A UART “break” condition can be used in three ways:
 1. Presenting a UART break condition to the chip can force the chip to perform a hardware reboot
 2. Presenting a break condition at boot time can hold the chip in a low power state, preventing normal initialisation while the condition exists
 3. With BCSP, the firmware can be configured to send a break to the host before sending data- normally used to wake the host from a deep sleep state
- The DFU standard has been extended with public/private key authentication, allowing manufacturers to control the firmware that can be loaded onto their Bluetooth modules
- A modified version of the DFU protocol allows firmware upgrade via the chip's UART
- A block of “radio test” or BIST commands allows direct control of the chip's radio. This aids the development of modules' radio designs, and can be used to support Bluetooth qualification.
- Virtual Machine (VM). The firmware provides the VM environment in which to run application-specific code. Although the VM is mainly used with BlueLab and “RFCOMM builds” (alternative firmware builds providing L2CAP, SDP and RFCOMM), the VM can be used with this build to perform simple tasks such as flashing LED's via the chip's PIO port.
- Hardware low power modes: shallow sleep and deep sleep. The chip drops into modes that significantly reduce power consumption when the software goes idle.
- SCO channels are normally routed via HCI (over BCSP). However, up to three SCO channels can be routed over the chip's single PCM port (at the same time as routing any remaining SCO channels over HCI).

- Co-operative existence with 802.11b/g chipsets. The device can be optionally configured to support a number of different co-existence schemes including:
 - TDMA – Bluetooth and WLAN avoid transmitting at the same time.
 - FDMA – Bluetooth avoids transmitting within the WLAN channel
 - Combination TDMA and FDMA – Bluetooth avoids transmitting in the WLAN channel only when WLAN is active.
- Please refer to separate documentation for full details of the co-existence schemes that CSR supports.

Note:

Always refer to the Firmware Release Note for the specific functionality of a particular build.

8.2 BlueCore RFCOMM Stack

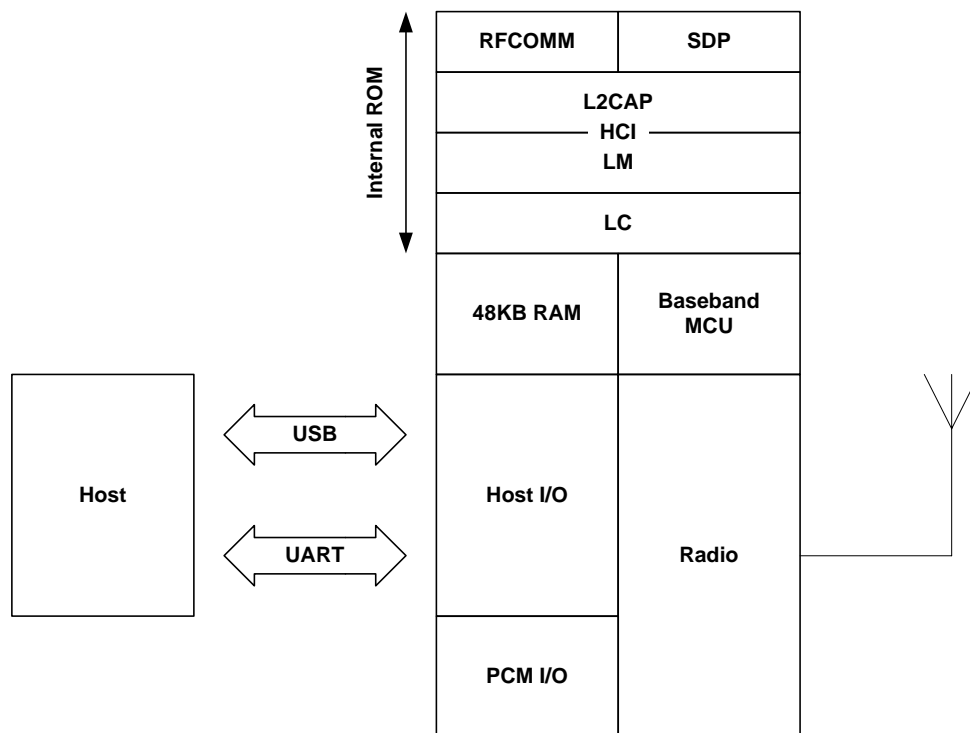


Figure 8.2: BlueCore RFCOMM Stack

In the version of the firmware, shown in Figure 8.2 the upper layers of the Bluetooth stack up to RFCOMM are run on-chip. This reduces host-side software and hardware requirements at the expense of some of the power and flexibility of the HCI only stack.

8.2.1 Key Features of the BlueCore4-ROM RFCOMM Stack

Interfaces to Host:

- RFCOMM, an RS-232 serial cable emulation protocol
- SDP, a service database look-up protocol

Connectivity:

- Maximum number of active slaves: 3
- Maximum number of simultaneous active ACL connections: 3
- Maximum number of simultaneous active SCO connections: 3
- Data Rate: up to 350 Kbps

Security:

- Full support for all Bluetooth security features up to and including strong (128-bit) encryption.

Power Saving:

- Full support for all Bluetooth power saving modes (Park, Sniff and Hold).

Data Integrity:

- CQDDR increases the effective data rate in noisy environments.
- RSSI used to minimise interference to other radio devices using the ISM band.

8.3 BlueCore Virtual Machine Stack

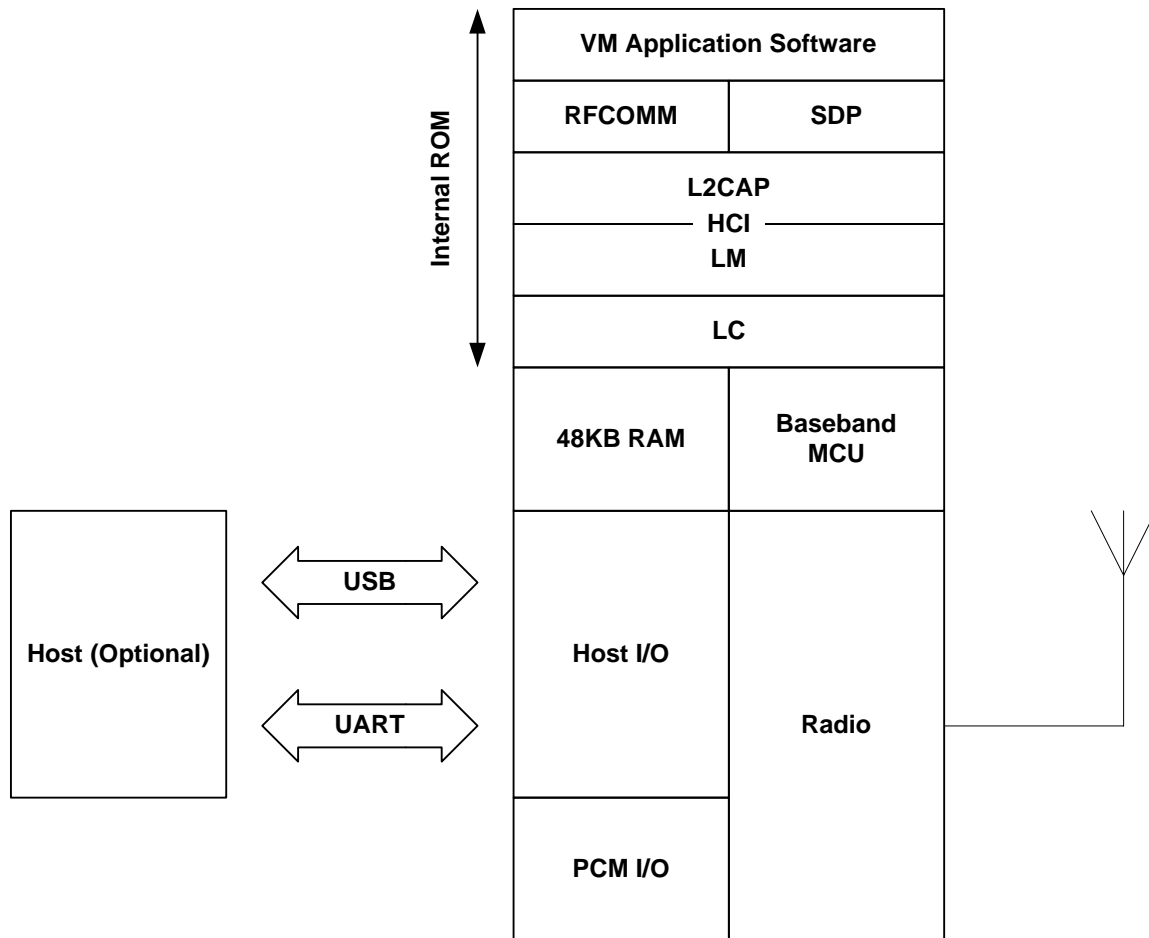


Figure 8.3: Virtual Machine

In Figure 8.3, this version of the stack firmware shown requires no host processor (but can use a host processor for debugging etc.). All software layers, including application software, run on the internal RISC processor in a protected user software execution environment known as a Virtual Machine (VM).

The user may write custom application code to run on the BlueCore VM using BlueLab™ software development kit (SDK) supplied with the BlueLab Multimedia and Casira development kits, available separately from CSR. This code will then execute alongside the main BlueCore firmware. The user is able to make calls to the BlueCore firmware for various operations.

The execution environment is structured so the user application does not adversely affect the main software routines, thus ensuring that the Bluetooth stack software component does not need re-qualification when the application is changed.

Using the VM and the BlueLab SDK the user is able to develop applications such as a cordless headset or other profiles without the requirement of a host controller. BlueLab is supplied with example code including a full implementation of the headset profile.

Note:

Sample applications to control PIO lines can also be written with BlueLab SDK and the VM for the HCI stack.

8.4 BCCHS Software

BlueCore Embedded Host Software is designed to enable CSR customers to implement Bluetooth functionality into embedded products quickly, cheaply and with low risk.

BCCHS is developed to work with CSR's family of BlueCore IC's. BCCHS is intended for embedded products that have a host processor for running BCCHS and the Bluetooth application e.g. a mobile phone or a PDA. BCCHS together with the BlueCore IC with embedded Bluetooth core stack (L2CAP, RFCOMM and SDP) is a complete Bluetooth system solution from RF to profiles.

BCCHS includes most of the Bluetooth intelligence and gives the user a simple API. This makes it possible to develop a Bluetooth product without in-depth Bluetooth knowledge.

The BlueCore Embedded Host Software contains 3 elements:

- Example Drivers (BCSP and proxies)
- Bluetooth Profile Managers
- Example Applications

The profiles are qualified which makes the qualification of the final product very easy. BCCHS is delivered with source code (ANSI C). With BCCHS also come example applications in ANSI C, which makes the process of writing the application easier.

8.5 Additional Software for Other Embedded Applications

When the upper layers of the Bluetooth protocol stack are run as firmware on BlueCore4-ROM, a UART software driver is supplied that presents the L2CAP, RFCOMM and Service Discovery (SDP) APIs to higher Bluetooth stack layers running on the host. The code is provided as 'C' source or object code.

8.6 CSR Development Systems

CSR's BlueLab and Casira development kits are available to allow the evaluation of the BlueCore4-ROM hardware and software, and as toolkits for developing on-chip and host software.

9 Enhanced Data Rate

Enhanced Data Rate (EDR) has been introduced to provide 2x and 3x⁽¹⁾ data rates with minimal disruption to higher layers of the Bluetooth stack. BlueCore4-ROM supports both of the new data rates and is compliant with the Bluetooth v2.0 + EDR specification.

Note:

⁽¹⁾ The inclusion of 3x data rates is optional.

9.1 Enhanced Data Rate Baseband

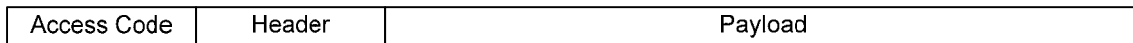
At the baseband level EDR utilises the same 1.6kHz slot rate and 1MHz symbol rate as the basic data rate. Where EDR differs is that each symbol in the payload portion of a packet represents 2 or 3-bits. This is achieved using two new distinct modulation schemes. These are summarised in Table 9.1 and in Figure 9.1.

Link establishment and management are unchanged and still use GFSK for both the header and payload portions of these packets.

Data Rate Scheme	Bits Per Symbol	Modulation
Basic Data Rate	1	GFSK
EDR	2	$\pi/4$ DQPSK
EDR	3	8DPSK (optional)

Table 9.1: Data Rate Schemes

Basic Rate



Enhanced Data Rate

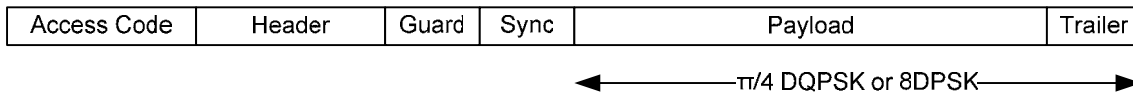


Figure 9.1: Basic Data Rate and Enhanced Data Rate Packet Structure

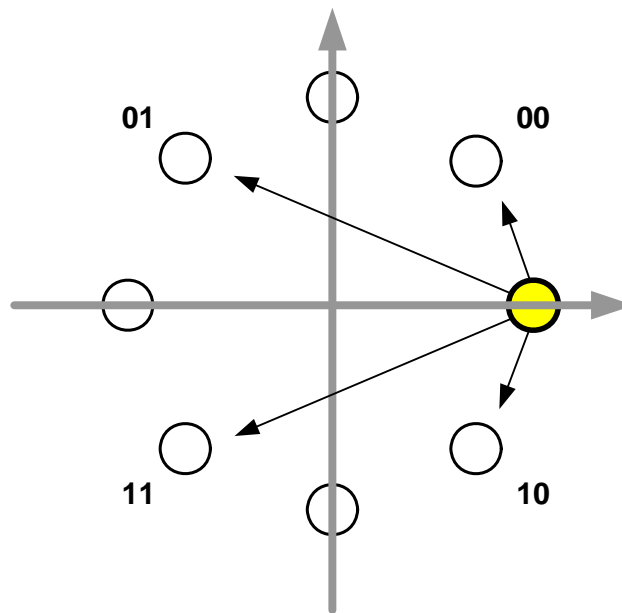
9.2 Enhanced Data Rate $\pi/4$ DQPSK

The 2x rate for EDR uses a $\pi/4$ DQPSK. Each symbol represents two bits of information. The constellation is shown in Figure 9.2 . It is described as having two planes, each with four points. Although there appear to be eight possible phase states, the encoding ensures that the trajectory of the modulation between symbols is restricted to the four states in the other plane.

For a given starting point, each phase change between symbols is restricted to $+3\pi/4$, $+\pi/4$, $-\pi/4$ or $-3\pi/4$ radians ($+135^\circ$, $+45^\circ$, -135° or -45°). For example, the arrows shown in Figure 9.2 represents trajectory to the four possible states in the other plane. The phase shift encoding of symbols is shown in Table 9.2.

There are two primary advantages in using $\pi/4$ -DQPSK modulation:

- The scheme avoids crossing the origin (a $+\pi$ or $-\pi$ phase shift) and therefore minimises amplitude variations in the envelope of the transmitted signal. This in turn allows the RF power amplifiers of the transmitter to be operated closer to their compression point without introducing spectral distortions. Consequently, the DC to RF efficiency is maximised.
- The differential encoding also allows for demodulation without the knowledge of an absolute value for the phase of the RF carrier.


 Figure 9.2: $\pi/4$ DQPSK Constellation Pattern

Bit Pattern	Phase Shift
00	$\pi/4$
01	$3\pi/4$
11	$-3\pi/4$
10	$-\pi/4$

Table 9.2: 2-Bits Determine Phase Shift Between Consecutive Symbols

9.3 Enhanced Data Rate 8DPSK

The 3x data rate modulation uses eight phase differential phase shift keying (8DPSK). Each symbol in the payload portion of the packet represents three baseband bits. Although 8DPSK appears to be similar to $\pi/4$ DQPSK, the differential phase shifts between symbols are now permissible between any of the eight possible phase states. This reduces the separation between adjacent symbols on the constellation to $\pi/4$ (45°) and thereby reduces the noise and interference immunity of the modulation scheme. Nevertheless, since each symbol now represents 3 baseband bits, the actual throughput of the data is 3x when compared with the basic data rate packet.

Figure 9.3 illustrates the 8DPSK constellation and Table 9.3 defines the phase encoding.

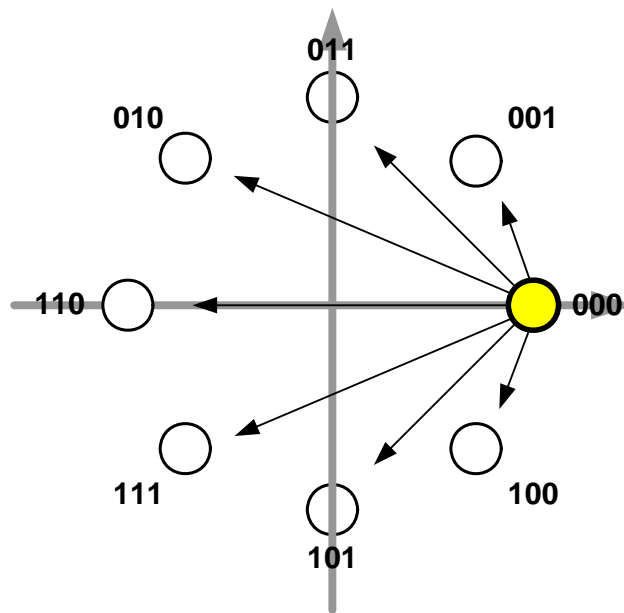


Figure 9.3: 8DPSK Constellation Pattern

Bit Pattern	Phase Shift
000	0
001	$\pi/4$
011	$\pi/2$
010	$3\pi/4$
110	π
111	$-3\pi/4$
101	$-\pi/2$
100	$-\pi/4$

Table 9.3: 3-Bits Determine Phase Shift Between Consecutive Symbols

10 Device Terminal Descriptions

10.1 RF Ports

The BlueCore4-ROM RF_IN terminal can be configured as either a single ended or differential input. The operational mode is determined by the setting the PS Key PSKEY_TXRX_PIO_CONTROL (0x20).

10.1.1 TX_A and TX_B

TX_A and TX_B form a complementary balanced pair. On transmit; their outputs are combined using a balun into the single-ended output required for the antenna. Similarly, on receive their input signals are combined internally. Both terminals present similar complex impedances that require matching networks between them and the balun. Starting from the substrate (chip side), the outputs can each be modelled as an ideal current source in parallel with a lossy resistance and a capacitor. The bond wire can be represented as series inductance.

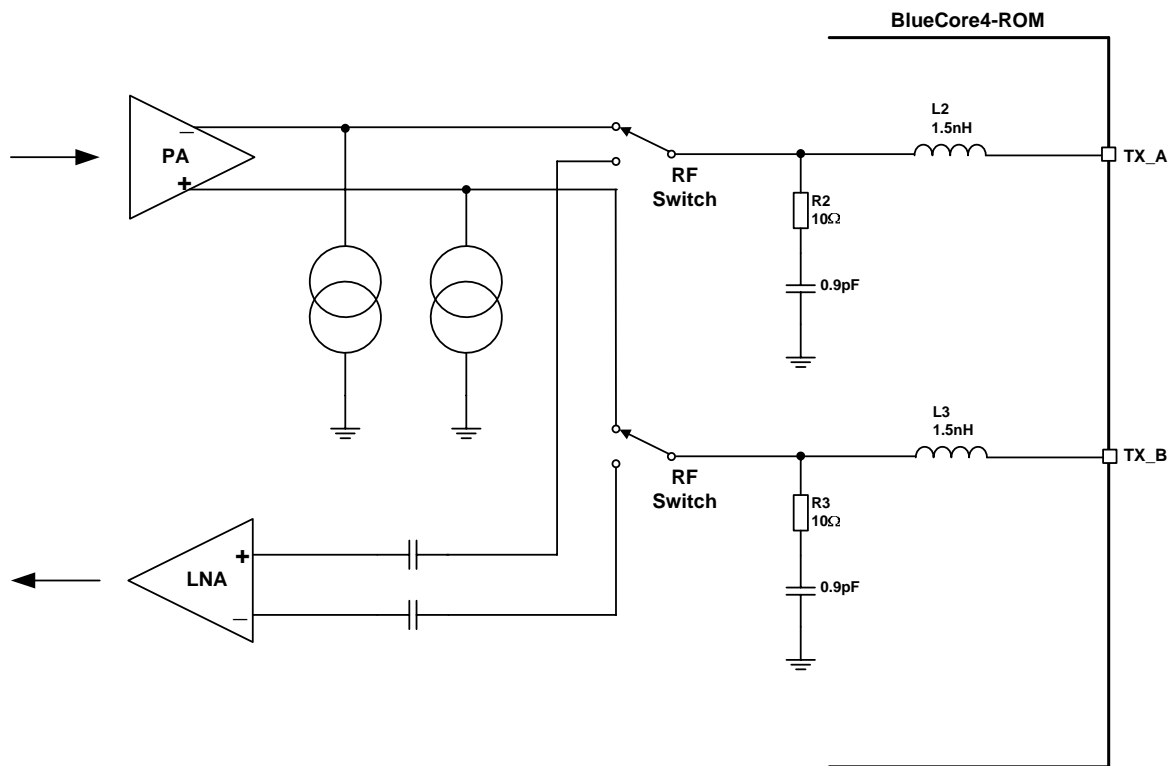


Figure 10.1: Circuit TX/RX_A and TX/RX_B

10.1.2 Single-Ended Input (RF_IN)

This is the single ended RF input from the antenna. The input presents a complex impedance that requires a matching network between the terminal and the antenna. Starting from the substrate (chip) side, the input can be modelled as a lossy capacitor with the bond wire to the ball grid represented as a series inductance.

The terminal is DC blocked. The DC level must not exceed (VSS_RADIO -0.3V to VDD_RADIO + 0.3V).

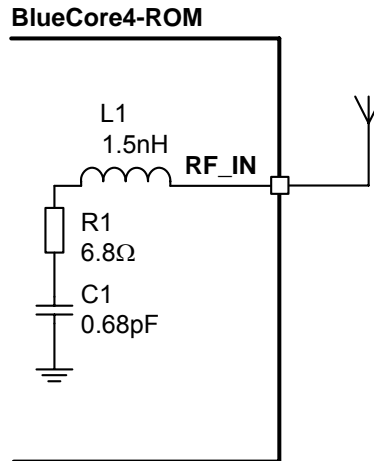


Figure 10.2: Circuit RF_IN

Note:

Both terminals must be externally DC biased to VDD_RADIO.

10.1.3 Transmit RF Power Control for Class 1 Applications (TX_PWR)

An 8-bit voltage DAC (AUX_DAC) is used to control the amplification level of the external PA for Class 1 operation. The DAC output is derived from the on chip band gap and is virtually independent of temperature and supply voltage. The output voltage is given by:

$$V_{DAC} = \text{MIN} \left(\left(3.3\text{v} \times \frac{\text{CNTRL_WORD}}{255} \right), (VDD_PIO - 0.3\text{v}) \right)$$

Equation 10.1: Output Voltage with Load Current $\leq 10\text{mA}$

for a load current $\leq 10\text{mA}$ (sourced from the device).

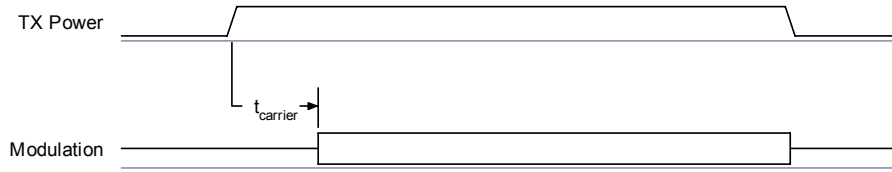
or

$$V_{DAC} = \text{MIN} \left(\left(3.3\text{v} \times \frac{\text{CNTRL_WORD}}{255} \right), VDD_PIO \right)$$

Equation 10.2: Output Voltage with No Load Current

for no load current.

BlueCore4-ROM enables the external PA only when transmitting. Before transmitting, the chip normally ramps up the power to the internal PA, then it ramps it down again afterwards. However, if a suitable external PA is used, it may be possible to ramp the power externally by driving the TX_PWR pin on the PA from AUX_DAC.


Figure 10.3: Internal Power Ramping

The persistent store key (PS Key) PSKEY_TX_GAINRAMP (0x1d), is used to control the delay (in units of μs) between the end of the transmit power ramp and the start of modulation. In this period the carrier is transmitted, which gives the transmit circuitry time to fully settle to the correct frequency.

Bits[15:8] define a delay, t_{carrier} , (in units of μs) between the end of the transmit power ramp and the start of modulation. In this period the carrier is transmitted, which aids interoperability with some other vendor equipment which is not strictly Bluetooth compliant.

10.1.4 Control of External RF Components

A PS Key TXRX_PIO_CONTROL (0x209) is used to control external RF components such as a switch, an external PA or an external LNA. PIO[0], PIO[1] and the AUX_DAC can be used for this purpose, as indicated in Table 10.1.

TXRX_PIO_CONTROL Value	AUX_DAC Use
0	PIO[0], PIO[1], AUX_DAC not used to control RF. Power ramping is internal.
1	PIO[0] is high during RX, PIO[1] is high during TX. AUX_DAC not used. Power ramping is internal.
2	PIO[0] is high during RX, PIO[1] is high during TX. AUX_DAC used to set gain of external PA. Power ramping is external.
3	PIO[0] is low during RX, PIO[1] is low during TX. AUX_DAC used to set gain of external PA. Power ramping is external.
4	PIO[0] is high during RX, PIO[1] is high during TX. AUX_DAC used to set gain of external PA. Power ramping is internal.

Table 10.1: TXRX_PIO_CONTROL Values

10.2 External Reference Clock Input (XTAL_IN)

The BlueCore4-ROM RF local oscillator and internal digital clocks are derived from the reference clock at the BlueCore4-ROM XTAL_IN input. This reference may be either an external clock or from a crystal connected between XTAL_IN and XTAL_OUT. The crystal mode is described in Section 10.2.5.

10.2.1 External Mode

BlueCore4-ROM can be configured to accept an external reference clock (from another device, such as TCXO) at XTAL_IN by connecting XTAL_OUT to ground. The external clock can either be a digital level square wave or sinusoidal and this may be directly coupled to XTAL_IN without the need for additional components. If the peaks of the reference clock are below VSS_ANA or above VDD_ANA, it must be driven through a DC blocking capacitor (~33pF) connected to XTAL_IN. A digital level reference clock gives superior noise immunity as the high slew rate clock edges have lower voltage to phase conversion.

The external clock signal should meet the specifications in Table 10.2:

	Min	Typ	Max
Frequency ⁽¹⁾	7.5MHz	16MHz	40MHz
Duty cycle	20:80	50:50	80:20
Edge Jitter (At Zero Crossing)	-	-	15ps rms
Signal Level	400mV pk-pk	-	VDD_ANA ⁽²⁾⁽³⁾

Table 10.2: External Clock Specifications

Notes:

- (1) The frequency should be an integer multiple of 250kHz except for the CDMA/3G frequencies
- (2) VDD_ANA is 1.8V nominal
- (3) If the external clock is driven through a DC blocking capacitor then maximum allowable amplitude is reduced from VDD_ANA to 800mV pk-pk

10.2.2 XTAL_IN Impedance in External Mode

The impedance of the XTAL_IN will not change significantly between operating modes, typically 10fF. When transitioning from deep sleep to an active state a spike of up to 1pC may be measured. For this reason it is recommended that a buffered clock input be used.

10.2.3 Clock Timing Accuracy

As Figure 10.4 indicates, the 250ppm timing accuracy on the external clock is required 7ms after the assertion of the system clock request line. This is to guarantee that the firmware can maintain timing accuracy in accordance with the Bluetooth v2.0 specification. Radio activity may occur after 11ms, therefore at this point, the timing accuracy of the external clock source must be within 20ppm.

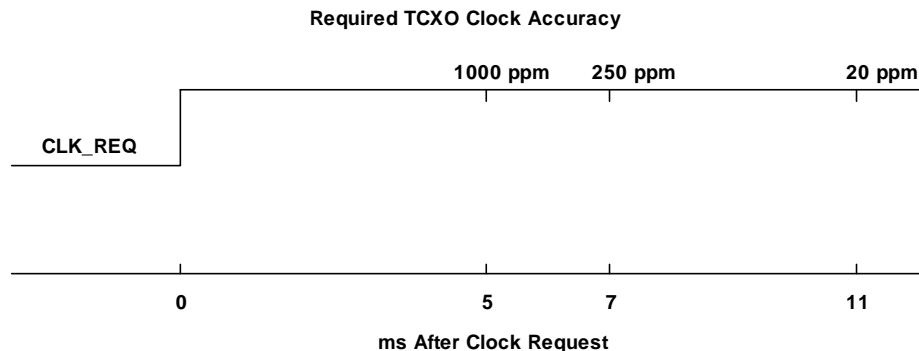


Figure 10.4: TCXO Clock Accuracy

10.2.4 Clock Start-Up Delay

BlueCore4-ROM hardware incorporates an automatic 5ms delay after the assertion of the system clock request signal before running firmware. This is suitable for most applications using an external clock source. However, there may be scenarios where the clock cannot be guaranteed to either exist or be stable after this period. Under these conditions, BlueCore4-ROM firmware provides a software function which will extend the system clock request signal by a period stored in PSKEY_CLOCK_STARTUP_DELAY. This value is set in milliseconds from 5-31ms.

This PS Key allows the designer to optimise a system where clock latencies may be longer than 5ms while still keeping the current consumption of BlueCore4-ROM as low as possible. BlueCore4-ROM will consume about 2mA of current for the duration of PSKEY_CLOCK_STARTUP_DELAY before activating the firmware.

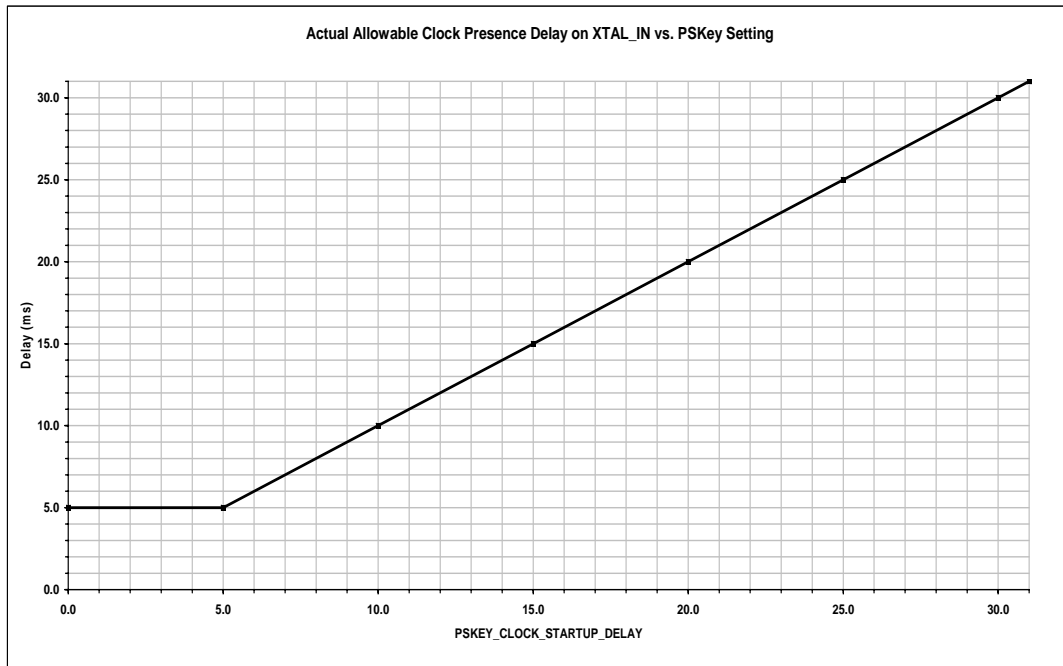


Figure 10.5: Actual Allowable Clock Presence Delay on XTAL_IN vs. PS Key Setting

10.2.5 Input Frequencies and PS Key Settings

BlueCore4-ROM should be configured to operate with the chosen reference frequency. This is accomplished by setting the PS Key PSKEY_ANA_FREQ (0x1fe) for all frequencies with an integer multiple of 250kHz. The input frequency default setting in BlueCore4-ROM is 26MHz.

The following CDMA/3G TCXO frequencies are also catered for: 7.68, 14.4, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz.

Reference Crystal Frequency (MHz)	PSKEY_ANA_FREQ (0x1fe) (Units of 1kHz)
7.68	7680
14.40	14400
15.36	15360
16.20	16200
16.80	16800
19.20	19200
19.44	19440
19.68	19680
19.80	19800
38.40	38400
n x 250kHz	-
+26.00 Default	26000

Table 10.3: PS Key Values for CDMA/3G Phone TCXO Frequencies

10.3 Crystal Oscillator (XTAL_IN, XTAL_OUT)

The BlueCore4-ROM RF local oscillator and internal digital clocks are derived from the reference clock at the BlueCore4-ROM XTAL_IN input. This reference may be either an external clock or from a crystal connected between XTAL_IN and XTAL_OUT. The external reference clock mode is described in Section 10.2.

10.3.1 XTAL Mode

BlueCore4-ROM contains a crystal driver circuit. This operates with an external crystal and capacitors to form a Pierce oscillator.

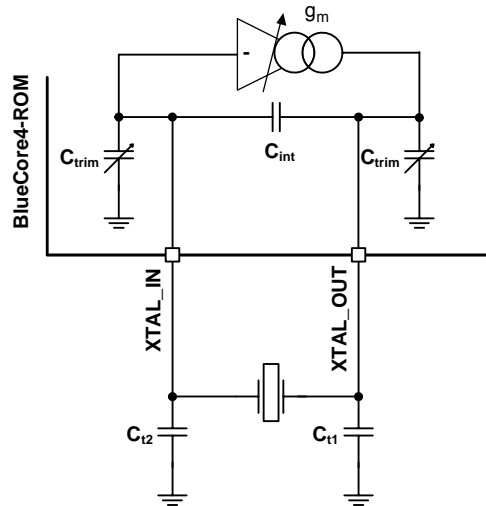


Figure 10.6: Crystal Driver Circuit

Figure 10.7 shows an electrical equivalent circuit for a crystal. The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors.

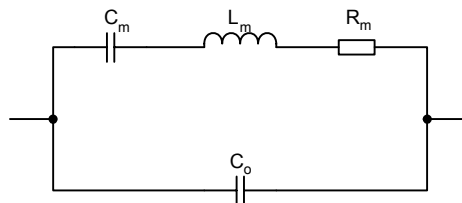


Figure 10.7: Crystal Equivalent Circuit

The resonant frequency may be trimmed with the crystal load capacitance. BlueCore4-ROM contains variable internal capacitors to provide a fine trim.

The BlueCore4-ROM driver circuit is a transconductance amplifier. A voltage at XTAL_IN generates a current at XTAL_OUT. The value of transconductance is variable and may be set for optimum performance.

10.3.2 Load Capacitance

For resonance at the correct frequency the crystal should be loaded with its specified load capacitance, which is defined for the crystal. This is the total capacitance across the crystal viewed from its terminals. BlueCore4-ROM provides some of this load with the capacitors C_{trim} and C_{int} . The remainder should be from the external capacitors labelled C_{t1} and C_{t2} . C_{t1} should be three times the value of C_{t2} for best noise performance. This maximises the signal swing, hence slew rate at XTAL_IN, to which all on chip clocks are referred. Crystal load capacitance, C_l is calculated with the following equation:

$$C_l = C_{int} + \frac{C_{trim}}{2} + \frac{C_{t1} \cdot C_{t2}}{C_{t1} + C_{t2}}$$

Equation 10.3: Load Capacitance

Where:

$C_{trim} = 3.4\text{pF}$ nominal (Mid range setting)

$C_{int} = 1.5\text{pF}$

Note:

C_{int} does not include the crystal internal self capacitance, it is the driver self capacitance

10.3.3 Frequency Trim

BlueCore4-ROM enables frequency adjustments to be made. This feature is typically used to remove initial tolerance frequency errors associated with the crystal. Frequency trim is achieved by adjusting the crystal load capacitance with on chip trim capacitors, C_{trim} . The value of C_{trim} is set by a 6-bit word in the Persistent Store Key PSKEY_ANA_FTRIM (0x1f6). Its value is calculated thus:

$$C_{trim} = 110 \text{ fF} \times \text{PSKEY_ANA_FTRIM}$$

Equation 10.4: Trim Capacitance

There are two C_{trim} capacitors, which are both connected to ground. When viewed from the crystal terminals, they appear in series so each least significant bit (LSB) increment of frequency trim presents a load across the crystal of 55fF.

The frequency trim is described by Equation 10.5:

$$\frac{\Delta(F_x)}{F_x} = \text{pullability} \times 55 \times 10^{-3} (\text{ppm/LSB})$$

Equation 10.5: Frequency Trim

Where F_x is the crystal frequency and pullability is a crystal parameter with units of ppm/pF. Total trim range is 63 times the value above.

If not specified, the pullability of a crystal may be calculated from its motional capacitance with Equation 10.6:

$$\frac{\partial(F_x)}{\partial(C)} = F_x \cdot \frac{C_m}{4(C_l + C_0)^2}$$

Equation 10.6: Pullability

Where:

C_0 = Crystal self capacitance (shunt capacitance)

C_m = Crystal motional capacitance (series branch capacitance in crystal model). See Figure 10.7.

Note:

It is a Bluetooth requirement that the frequency is always within $\pm 20\text{ppm}$. The trim range should be sufficient to pull the crystal within $\pm 5\text{ppm}$ of the exact frequency. This leaves a margin of $\pm 15\text{ppm}$ for frequency drift with ageing and temperature. A crystal with an ageing and temperature drift specification of better than $\pm 15\text{ppm}$ is required.

10.3.4 Transconductance Driver Model

The crystal and its load capacitors should be viewed as a transimpedance element, whereby a current applied to one terminal generates a voltage at the other. The transconductance amplifier in BlueCore4-ROM uses the voltage at its input, XTAL_IN, to generate a current at its output, XTAL_OUT. Therefore, the circuit will oscillate if the transconductance, transimpedance product is greater than unity. For sufficient oscillation amplitude, the product should be greater than 3. The transconductance required for oscillation is defined by the following relationship:

$$g_m > \frac{3(C_{t1} + C_{trim})(C_{t2} + C_{trim})}{(2\pi F_x)^2 R_m ((C_0 + C_{int})(C_{t1} + C_{t2} + 2C_{trim}) + (C_{t1} + C_{trim})(C_{t2} + C_{trim}))^2}$$

Equation 10.7: Transconductance Required for Oscillation

BlueCore4-ROM guarantees a transconductance value of at least 2mA/V at maximum drive level.

Notes:

More drive strength is required for higher frequency crystals, higher loss crystals (larger R_m) or higher capacitance loading.

Optimum drive level is attained when the level at XTAL_IN is approximately 1V pk-pk. The drive level is determined by the crystal driver transconductance, by setting the Persistent Store KEY_XTAL_LVL (0x241).

10.3.5 Negative Resistance Model

An alternative representation of the crystal and its load capacitors is a frequency dependent resistive element. The driver amplifier may be considered as a circuit that provides negative resistance. For oscillation, the value of the negative resistance must be greater than that of the crystal circuit equivalent resistance. Although the BlueCore4-ROM crystal driver circuit is based on a transimpedance amplifier, an equivalent negative resistance may be calculated for it with the following formula in Equation 10.8:

$$R_{neg} > \frac{3(C_{t1} + C_{trim})(C_{t2} + C_{trim})}{g_m (2\pi F_x)^2 (C_0 + C_{int})(C_{t1} + C_{t2} + 2C_{trim}) + (C_{t1} + C_{trim})(C_{t2} + C_{trim})^2}$$

Equation 10.8: Equivalent Negative Resistance

This formula shows the negative resistance of the BlueCore4-ROM driver as a function of its drive strength.

The value of the driver negative resistance may be easily measured by placing an additional resistance in series with the crystal. The maximum value of this resistor (oscillation occurs) is the equivalent negative resistance of the oscillator.

	Min	Typ	Max
Frequency	8MHz	16MHz	32MHz
Initial Tolerance	-	±25ppm	-
Pullability	-	±20ppm/pF	-

Table 10.4: Oscillator Negative Resistance

10.3.6 Crystal PS Key Settings

See tables in Section 10.2.5.

10.3.7 Crystal Oscillator Characteristics

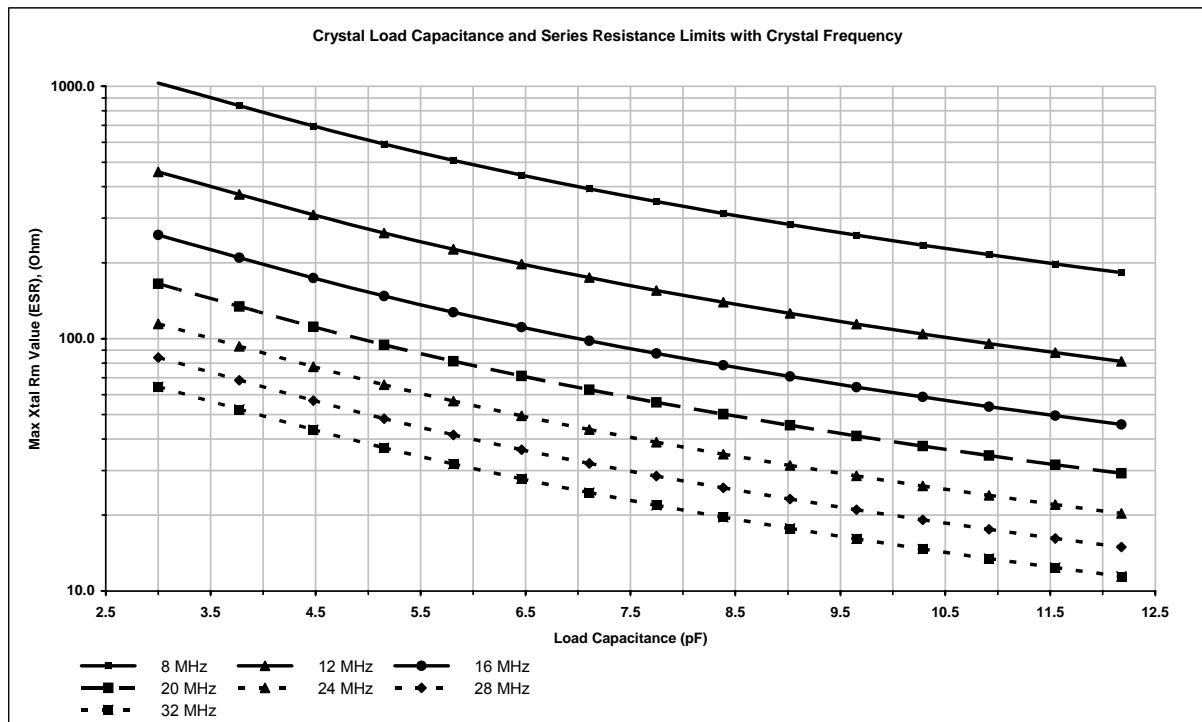


Figure 10.8: Crystal Load Capacitance and Series Resistance Limits with Crystal Frequency

Note:

Graph shows results for BlueCore4-ROM crystal driver at maximum drive level.

Conditions:

$C_{trim} = 3.4\text{pF}$ centre value

Crystal $C_o = 2\text{pF}$

Transconductance setting = 2mA/V

Loop gain = 3

$C_{t1}/C_{t2} = 3$

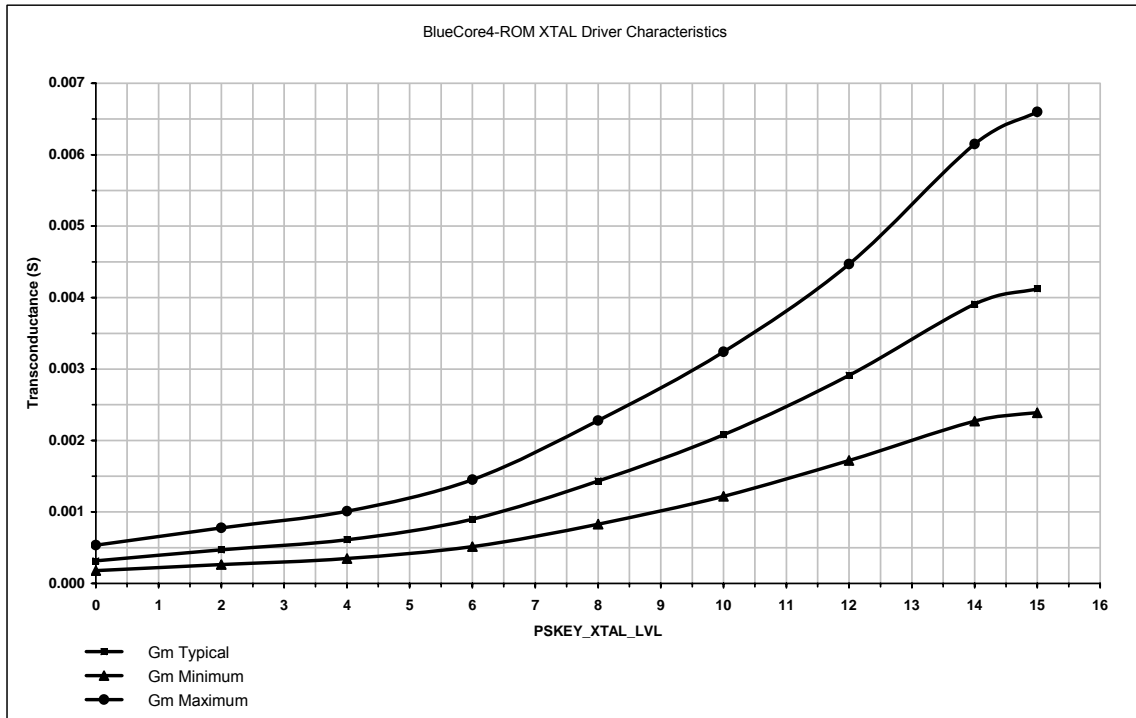


Figure 10.9: Crystal Driver Transconductance vs. Driver Level Register Setting

Note:

Drive level is set by Persistent Store Key PSKEY_XTAL_LVL (0x241).

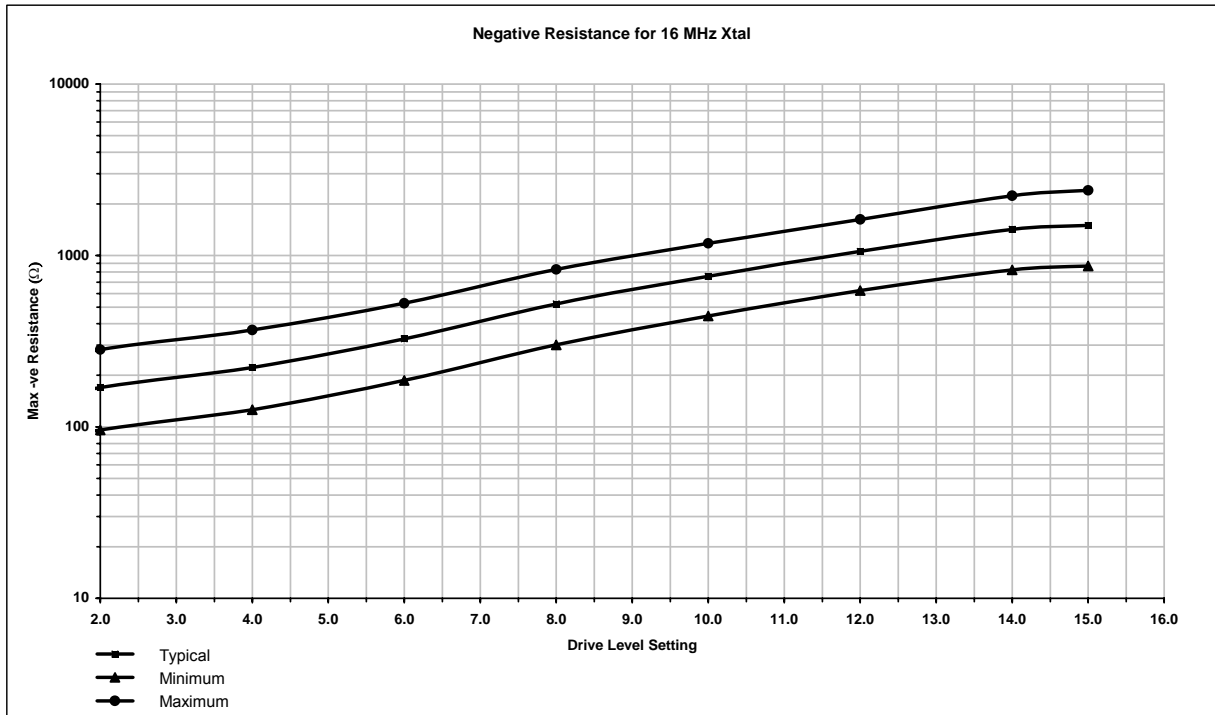


Figure 10.10: Crystal Driver Negative Resistance as a Function of Drive Level Setting

Crystal parameters:

Crystal frequency 16MHz (Please refer to your software build release note for frequencies supported);

Crystal $C_0 = 0.75\text{pF}$

Circuit parameters:

$C_{\text{trim}} = 8\text{pF}$, maximum value

$C_{t1}, C_{t2} = 5\text{pF}$ (3.9pF plus 1.1 pF stray)

(Crystal total load capacitance 8.5pF)

Note:

This is for a specific crystal and load capacitance.

10.4 UART Interface

BlueCore4-ROM Universal Asynchronous Receiver Transmitter (UART) interface provides a simple mechanism for communicating with other serial devices using the RS232 standard⁽¹⁾.

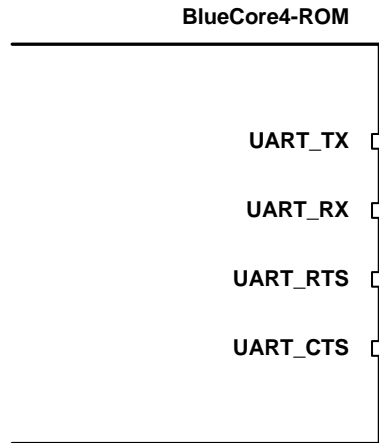


Figure 10.11: Universal Asynchronous Receiver

Four signals are used to implement the UART function, as shown in Figure 10.11. When BlueCore4-ROM is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators. All UART connections are implemented using CMOS technology and have signalling levels of 0V and VDD_USB.

UART configuration parameters, such as Baud rate and packet format, are set using BlueCore4-ROM software.

Notes:

In order to communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

⁽¹⁾ Uses RS232 protocol but voltage levels are 0V to VDD_USB, (requires external RS232 transceiver chip)

Parameter		Possible Values
Baud Rate	Minimum	1200 Baud ($\leq 2\%$ Error)
		9600 Baud ($\leq 1\%$ Error)
	Maximum	1.5Mbaud ($\leq 1\%$ Error)
Flow Control		RTS/CTS or None
Parity		None, Odd or Even
Number of Stop Bits		1 or 2
Bits per channel		8

Table 10.5: Possible UART Settings

The UART interface is capable of resetting BlueCore4-ROM upon reception of a break signal. A Break is identified by a continuous logic low (0V) on the UART_RX terminal, as shown in Figure 10.12. If t_{BRK} is longer than the value, defined by the PS Key PSKEY_HOST_IO_UART_RESET_TIMEOUT, (0x1a4), a reset will occur. This feature allows a host to initialise the system to a known state. Also, BlueCore4-ROM can emit a Break character that may be used to wake the Host.

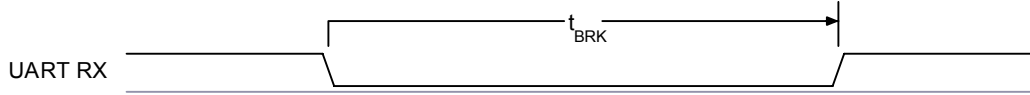


Figure 10.12: Break Signal

Note:

The DFU boot loader must be loaded into the Flash device before the UART or USB interfaces can be used. This initial flash programming can be done via the SPI.

Table 10.4 shows a list of commonly used Baud rates and their associated values for the Persistent Store Key PSKEY_UART_BAUD_RATE (0x204). There is no requirement to use these standard values. Any Baud rate within the supported range can be set in the Persistent Store Key according to the formula in Equation 10.9.

$$\text{Baud Rate} = \frac{\text{PSKEY_UART_BAUD_RATE}}{0.004096}$$

Equation 10.9: Baud Rate

Baud Rate	Persistent Store Value		Error
	Hex	Dec	
1200	0x0005	5	1.73%
2400	0x000a	10	1.73%
4800	0x0014	20	1.73%
9600	0x0027	39	-0.82%
19200	0x004f	79	0.45%
38400	0x009d	157	-0.18%
57600	0x00ec	236	0.03%
76800	0x013b	315	0.14%
115200	0x01d8	472	0.03%
230400	0x03b0	944	0.03%
460800	0x075f	1887	-0.02%
921600	0x0ebf	3775	0.00%
1382400	0x161e	5662	-0.01%

Table 10.6: Standard Baud Rates ⁽¹⁾

Note:

⁽¹⁾ Table will be extended to cover EDR

10.4.1 UART Bypass

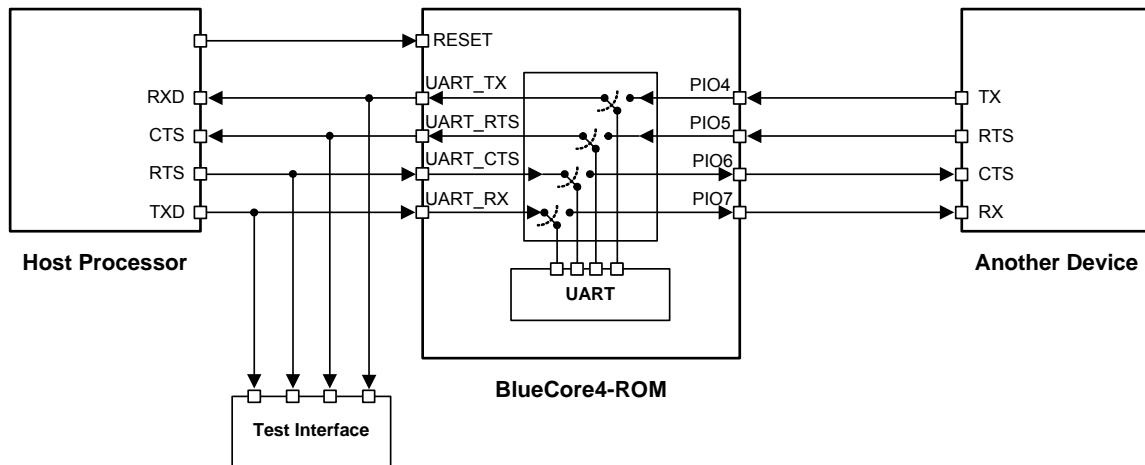


Figure 10.13: UART Bypass Architecture

10.4.2 UART Configuration While RESET is Active

The UART interface for BlueCore4-ROM while the chip is being held in reset is tri-state. This will allow the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tri-state when BlueCore4-ROM reset is de-asserted and the firmware begins to run.

10.4.3 UART Bypass Mode

Alternatively, for devices that do not tri-state the UART bus, the UART bypass mode on BlueCore4-ROM can be used. The default state of BlueCore4-ROM after reset is de-asserted, this is for the host UART bus to be connected to the BlueCore4-ROM UART, thereby allowing communication to BlueCore4-ROM via the UART. All UART bypass mode connections are implemented using CMOS technology and have signalling levels of 0V and VDD_PADS⁽¹⁾.

In order to apply the UART bypass mode, a BCCMD command will be issued to BlueCore4-ROM upon this, it will switch the bypass to PIO[7:4] as shown in Figure 10.13. Once the bypass mode has been invoked, BlueCore4-ROM will enter the deep sleep state indefinitely.

In order to re-establish communication with BlueCore4-ROM, the chip must be reset so that the default configuration takes affect.

It is important for the host to ensure a clean Bluetooth disconnection of any active links before the bypass mode is invoked. Therefore it is not possible to have active Bluetooth links while operating the bypass mode.

10.4.4 Current Consumption in UART Bypass Mode

The current consumption for a device in UART Bypass Mode is equal to the values quoted for a device in standby mode.

Note:

- ⁽¹⁾ The range of the signalling level for the standard UART described in section 10.4 and the UART bypass may differ between CSR BlueCore devices, as the power supply configurations are chip dependent.

For BlueCore3-Multimedia the standard UART is supplied by VDD_USB so has signalling levels of 0V and VDD_USB. Whereas in the UART bypass mode the signals appear on the PIO[4:7] which are supplied by VDD_PADS, therefore the signalling levels are 0V and VDD_PADS.

10.5 USB Interface

BlueCore4-ROM USB devices contain a full speed (12Mbits/s) USB interface that is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth specification v2.0 or alternatively can appear as a set of endpoint appropriate to USB audio devices such as speakers.

As USB is a Master/Slave oriented system (in common with other USB peripherals), BlueCore4-ROM only supports USB Slave operation.

10.5.1 USB Data Connections

The USB data lines emerge as pins USB_DP and USB_DN. These terminals are connected to the internal USB I/O buffers of the BlueCore4-ROM and therefore have a low output impedance. To match the connection to the characteristic impedance of the USB cable, resistors must be placed in series with USB_DP / USB_DN and the cable.

10.5.2 USB Pull-Up Resistor

BlueCore4-ROM features an internal USB pull-up resistor. This pulls the USB_DP pin weakly high when BlueCore4-ROM is ready to enumerate. It signals to the PC that it is a full speed (12Mbit/s) USB device.

The USB internal pull-up is implemented as a current source, and is compliant with Section 7.1.5 of the USB specification v1.1. The internal pull-up pulls USB_DP high to at least 2.8V when loaded with a $15k\Omega \pm 5\%$ pull-down resistor (in the hub/host) when $VDD_PADS=3.1V$. This presents a Thevenin resistance to the host of at least 900Ω . Alternatively, an external $1.5k\Omega$ pull-up resistor can be placed between a PIO line and D+ on the USB cable. The firmware must be alerted to which mode is used by setting PS Key PSKEY_USB_PIO_PULLUP appropriately. The default setting uses the internal pull-up resistor.

10.5.3 Power Supply

The USB specification dictates that the minimum output high voltage for USB data lines is 2.8V. To safely meet the USB specification, the voltage on the VDD_USB supply terminals must be an absolute minimum of 3.1V. CSR recommends 3.3V for optimal USB signal quality.

10.5.4 Self Powered Mode

In self powered mode, the circuit is powered from its own power supply and not from the VBUS (5V) line of the USB cable. It draws only a small leakage current (below 0.5mA) from VBUS on the USB cable. This is the easier mode for which to design for, as the design is not limited by the power that can be drawn from the USB hub or root port. However, it requires that VBUS be connected to BlueCore4-ROM via a resistor network (R_{vb1} and R_{vb2}), so BlueCore4-ROM can detect when VBUS is powered up. BlueCore4-ROM will not pull USB_DP high when VBUS is off.

Self powered USB designs (powered from a battery or PSU) must ensure that a PIO line is allocated for USB pull-up purposes. A 1.5K 5% pull-up resistor between USB_DP and the selected PIO line should be fitted to the design. Failure to fit this resistor may result in the design failing to be USB compliant in self powered mode. The internal pull-up in BlueCore is only suitable for bus powered USB devices i.e. dongles.

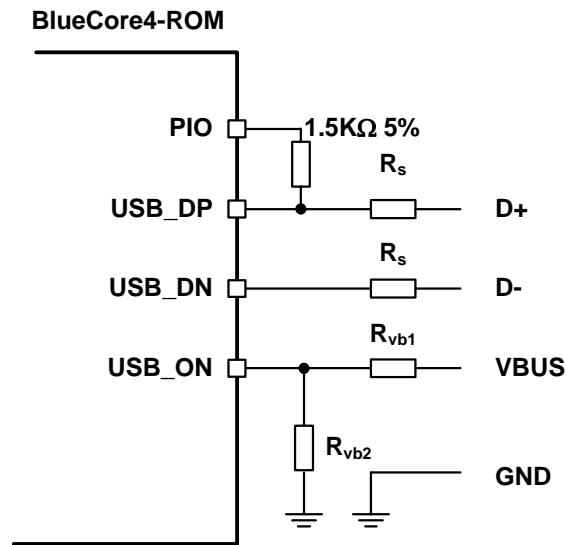


Figure 10.14: USB Connections for Self Powered Mode

The terminal marked USB_ON can be any free PIO pin. The PIO pin selected must be registered by setting PSKEY_USB_PIO_VBUS to the corresponding pin number.

Note:

USB_ON is shared with BlueCore4-ROM PIO terminals

Identifier	Value	Function
R_s	27 Ω nominal	Impedance matching to USB cable
R_{vb1}	22k Ω 5%	VBUS ON sense divider
R_{vb2}	47k Ω 5%	VBUS ON sense divider

Table 10.7: USB Interface Component Values

10.5.5 Bus Powered Mode

In bus powered mode the application circuit draws its current from the 5V VBUS supply on the USB cable. BlueCore4-ROM negotiates with the PC during the USB enumeration stage about how much current it is allowed to consume.

For Class 2 Bluetooth applications, CSR recommends that the regulator used to derive 3.3V from VBUS is rated at 100mA average current and should be able to handle peaks of 120mA without foldback or limiting. In bus powered mode, BlueCore4-ROM requests 100mA during enumeration.

For Class 1 Bluetooth applications, the USB power descriptor should be altered to reflect the amount of power required. This is accomplished by setting the PS Key PSKEY_USB_MAX_POWER (0x2c6). This is higher than for a Class 2 application due to the extra current drawn by the Transmit RF PA.

When selecting a regulator, be aware that VBUS may go as low as 4.4V. The inrush current (when charging reservoir and supply decoupling capacitors) is limited by the USB specification (see USB specification v1.1, Section 7.2.4.1). Some applications may require soft start circuitry to limit inrush current if more than 10 μ F is present between VBUS and GND.

The 5V VBUS line emerging from a PC is often electrically noisy. As well as regulation down to 3.3V and 1.8V, applications should include careful filtering of the 5V line to attenuate noise that is above the voltage regulator bandwidth. Excessive noise on the 1.8V supply to the analogue supply pins of BlueCore4-ROM will result in reduced receive sensitivity and a distorted RF transmit signal.

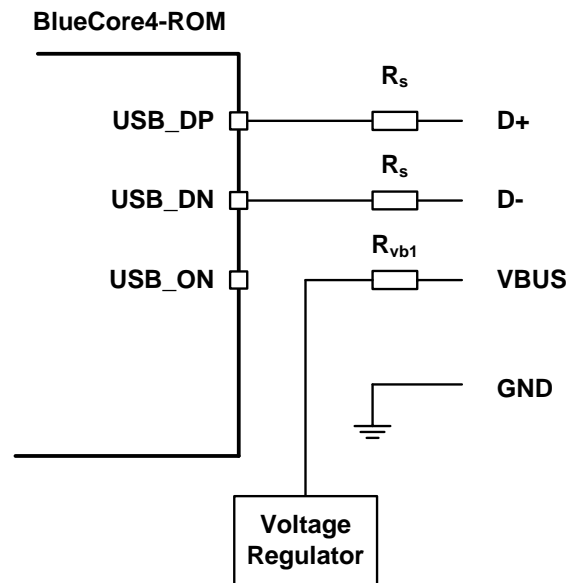


Figure 10.15: USB Connections for Bus Powered Mode

10.5.6 Suspend Current

All USB devices must permit the USB controller to place them in a USB Suspend mode. While in USB Suspend, bus powered devices must not draw more than 0.5mA from USB VBUS (self powered devices may draw more than 0.5mA from their own supply). This current draw requirement prevents operation of the radio by bus powered devices during USB Suspend.

The voltage regulator circuit itself should draw only a small quiescent current (typically less than 100 μ A) to ensure adherence to the suspend current requirement of the USB specification. This is not normally a problem with modern regulators. Ensure that external LEDs and/or amplifiers can be turned off by BlueCore4-ROM. The entire circuit must be able to enter the suspend mode. (For more details on USB Suspend, see separate CSR documentation).

10.5.7 Detach and Wake-Up Signalling

BlueCore4-ROM can provide out-of-band signalling to a host controller by using the control lines called 'USB_DETACH' and 'USB_WAKE_UP'. These are outside the USB specification (no wires exist for them inside the USB cable), but can be useful when embedding BlueCore4-ROM into a circuit where no external USB is visible to the user. Both control lines are shared with PIO pins and can be assigned to any PIO pin by setting the PS Keys PSKEY_USB_PIO_DETACH and PSKEY_USB_PIO_WAKEUP to the selected PIO number.

USB_DETACH is an input which, when asserted high, causes BlueCore4-ROM to put USB_DN and USB_DP in a high impedance state and turned off the pull-up resistor on D+. This detaches the device from the bus and is logically equivalent to unplugging the device. When USB_DETACH is taken low, BlueCore4-ROM will connect back to USB and await enumeration by the USB host.

USB_WAKE_UP is an active high output (used only when USB_DETACH is active) to wake up the host and allow USB communication to recommence. It replaces the function of the software USB WAKE_UP message (which runs over the USB cable), and cannot be sent while BlueCore4-ROM is effectively disconnected from the bus.

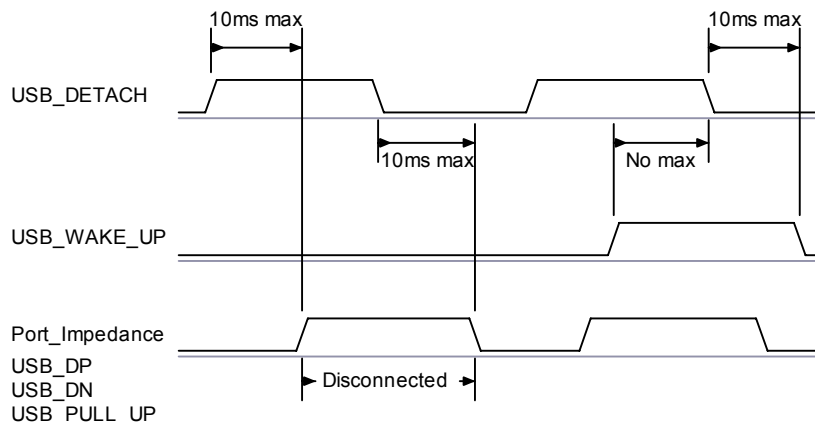


Figure 10.16: USB_DETACH and USB_WAKE_UP Signal

10.5.8 USB Driver

A USB Bluetooth device driver is required to provide a software interface between BlueCore4-ROM and Bluetooth software running on the host computer. Suitable drivers are available from www.csrsupport.com.

10.5.9 USB 1.1 Compliance

BlueCore4-ROM is qualified to the USB specification v1.1, details of which are available from <http://www.usb.org>

The specification contains valuable information on aspects such as PCB track impedance, supply inrush current and product labelling.

Although BlueCore4-ROM meets the USB specification, CSR cannot guarantee that an application circuit designed around the chip is USB compliant. The choice of application circuit, component choice and PCB layout all affect USB signal quality and electrical characteristics. The information in this document is intended as a guide and should be read in association with the USB specification, with particular attention being given to Chapter 7. Independent USB qualification must be sought before an application is deemed USB compliant and can bear the USB logo. Such qualification can be obtained from a USB plugfest or from an independent USB test house.

Terminals USB_DP and USB_DN adhere to the USB specification 2.0 (Chapter 7) electrical requirements.

10.5.10 USB 2.0 Compatibility

BlueCore4-ROM is compatible with USB v2.0 host controllers; under these circumstances the two ends agree the mutually acceptable rate of 12Mbits/s according to the USB v2.0 specification.

10.6 Serial Peripheral Interface

BlueCore4-ROM uses 16-bit data and 16-bit address serial peripheral interface, where transactions may occur when the internal processor is running or is stopped. This section details the considerations required when interfacing to BlueCore4-ROM via the four dedicated serial peripheral interface terminals. Data may be written or read one word at a time or the auto increment feature may be used to access blocks.

10.6.1 Instruction Cycle

The BlueCore4-ROM is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO. The instruction cycle for a SPI transaction is shown in Table 10.8.

1	Reset the SPI interface	Hold SPI_CSB high for two SPI_CLK cycles
2	Write the command word	Take SPI_CSB low and clock in the 8-bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word(s)
5	Termination	Take SPI_CSB high

Table 10.8: Instruction Cycle for an SPI Transaction

With the exception of reset, SPI_CSB must be held low during the transaction. Data on SPI_MOSI is clocked into the BlueCore4-ROM on the rising edge of the clock line SPI_CLK. When reading, BlueCore4-ROM will reply to the master on SPI_MISO with the data changing on the falling edge of the SPI_CLK. The master provides the clock on SPI_CLK. The transaction is terminated by taking SPI_CSB high.

Sending a command word and the address of a register for every time it is to be read or written is a significant overhead, especially when large amounts of data are to be transferred. To overcome this BlueCore4-ROM offers increased data transfer efficiency via an auto increment operation. To invoke auto increment, SPI_CSB is kept low, which auto increments the address, while providing an extra 16 clock cycles for each extra word to be written or read.

10.6.2 Writing to BlueCore4-ROM

To write to BlueCore4-ROM, the 8-bit write command (00000010) is sent first (C[7:0]) followed by a 16-bit address (A[15:0]). The next 16-bits (D[15:0]) clocked in on SPI_MOSI are written to the location set by the address (A). Thereafter for each subsequent 16-bits clocked in, the address (A) is incremented and the data written to consecutive locations until the transaction terminates when SPI_CSB is taken high.

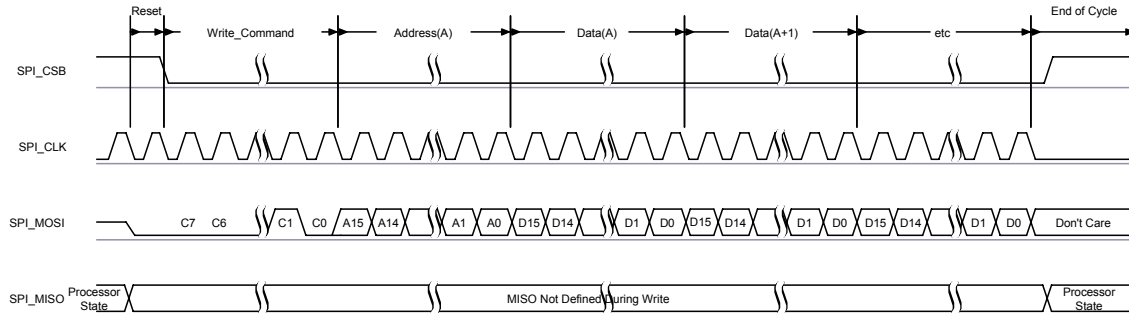


Figure 10.17: Write Operation

10.6.3 Reading from BlueCore4-ROM

Reading from BlueCore4-ROM is similar to writing to it. An 8-bit read command (00000011) is sent first (C[7:0]), followed by the address of the location to be read (A[15:0]). BlueCore4-ROM then outputs on SPI_MISO a check word during T[15:0] followed by the 16-bit contents of the addressed location during bits D[15:0].

The check word is composed of {command, address [15:8]}. The check word may be used to confirm a read operation to a memory location. This overcomes the problems encountered with typical serial peripheral interface slaves, whereby it is impossible to determine whether the data returned by a read operation is valid data or the result of the slave device not responding.

If SPI_CSB is kept low, data from consecutive locations is read out on SPI_MISO for each subsequent 16 clocks, until the transaction terminates when SPI_CSB is taken high.

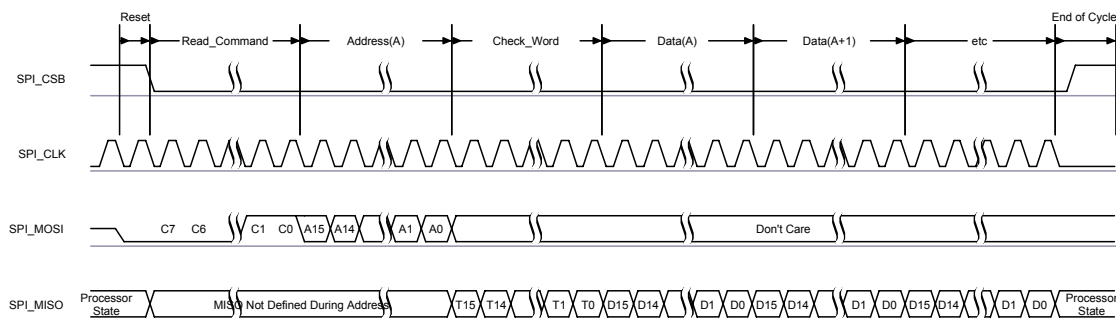


Figure 10.18: Read Operation

10.6.4 Multi Slave Operation

BlueCore4-ROM should not be connected in a multi slave arrangement by simple parallel connection of slave MISO lines. When BlueCore4-ROM is deselected (SPI_CSB = 1), the SPI_MISO line does not float, instead, BlueCore4-ROM outputs 0 if the processor is running or 1 if it is stopped.

10.7 Audio PCM Interface

Pulse Code Modulation (PCM) is a standard method used to digitise audio (particularly voice) patterns for transmission over digital communication channels. Through its PCM interface, BlueCore4-ROM has hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for wireless headset applications. BlueCore4-ROM offers a bi directional digital audio interface that routes directly into the baseband layer of the on chip firmware. It does not pass through the HCI protocol layer.

Hardware on BlueCore4-ROM allows the data to be sent to and received from a SCO connection.

Up to three SCO connections can be supported by the PCM interface at any one time⁽¹⁾.

BlueCore4-ROM can operate as the PCM interface Master generating an output clock of 128, 256 or 512kHz. When configured as PCM interface slave it can operate with an input clock up to 2048kHz. BlueCore4-ROM is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13 or 16-bit linear, 8-bit μ -law or A-law companded sample formats at 8ksamples/s and can receive and transmit on any selection of three of the first four slots following PCM_SYNC. The PCM configuration options are enabled by setting the PS Key PS_KEY_PCM_CONFIG32 (0x1b3).

BlueCore4-ROM interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 four channel A-law and μ -law CODEC
- Motorola MC145481 8-bit A-law and μ -law CODEC
- Motorola MC145483 13-bit linear CODEC
- STW 5093 and 5094 14-bit linear CODECs
- BlueCore4-ROM is also compatible with the Motorola SSI™ interface

Note:

- ⁽¹⁾ Subject to firmware support, contact CSR for current status.

10.7.1 PCM Interface Master/Slave

When configured as the Master of the PCM interface, BlueCore4-ROM generates PCM_CLK and PCM_SYNC.

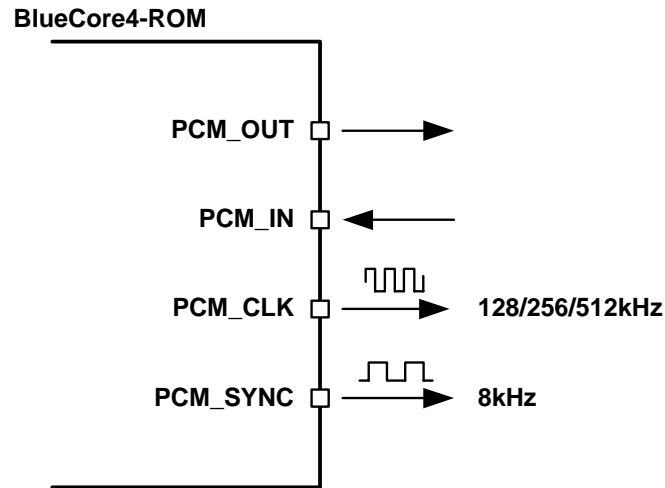


Figure 10.19: BlueCore4-ROM as PCM Interface Master

When configured as the Slave of the PCM interface, BlueCore4-ROM accepts PCM_CLK rates up to 2048kHz.

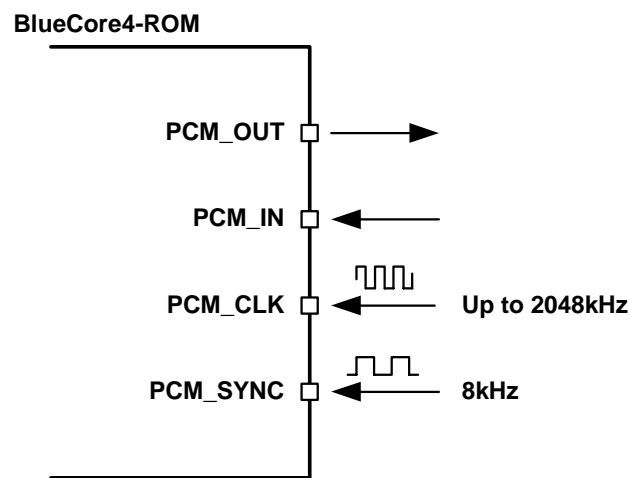


Figure 10.20: BlueCore4-ROM as PCM Interface Slave

10.7.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When BlueCore4-ROM is configured as PCM Master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When BlueCore4-ROM is configured as PCM Slave, PCM_SYNC may be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate, i.e. 62.5µs long.

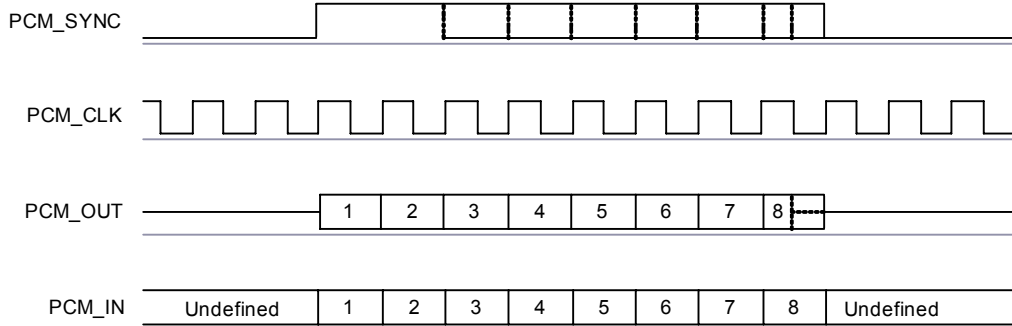


Figure 10.21: Long Frame Sync (Shown with 8-bit Companded Sample)

BlueCore4-ROM samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

10.7.3 Short Frame Sync

In Short Frame Sync the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

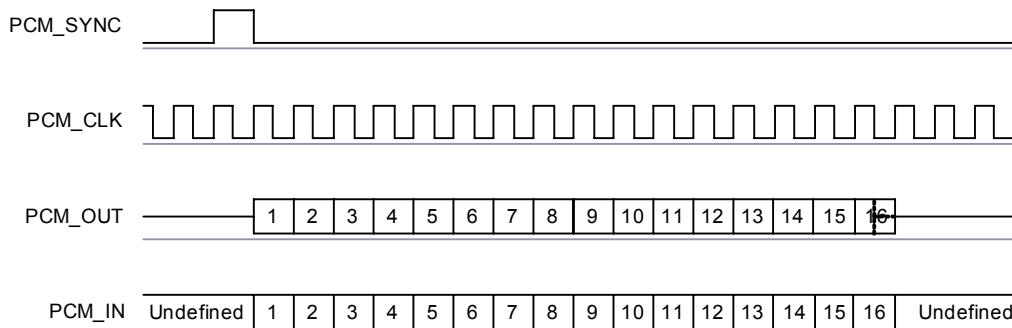


Figure 10.22: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, BlueCore4-ROM samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

10.7.4 Multi Slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.

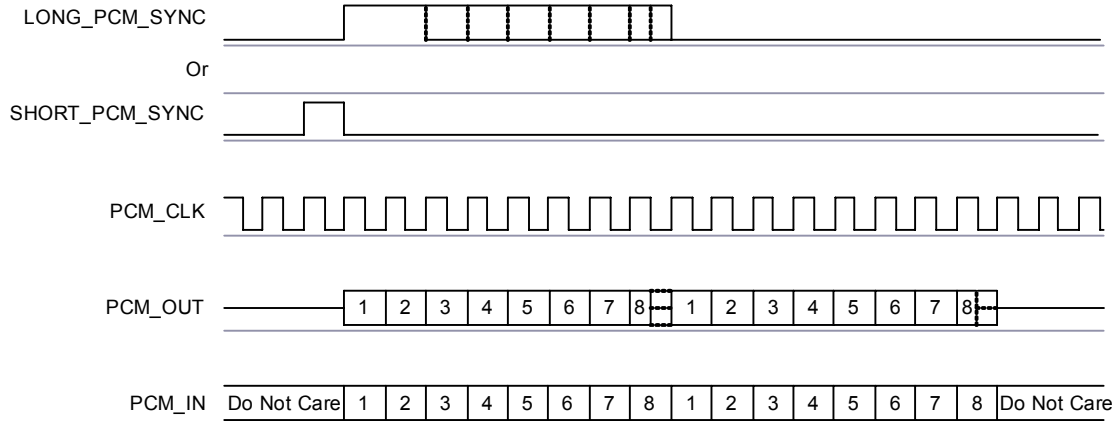


Figure 10.23: Multi Slot Operation with Two Slots and 8-bit Companded Samples

10.7.5 GCI Interface

BlueCore4-ROM is compatible with the General Circuit Interface, a standard synchronous 2B+D ISDN timing interface. The two 64Kbps B channels can be accessed when this mode is configured.

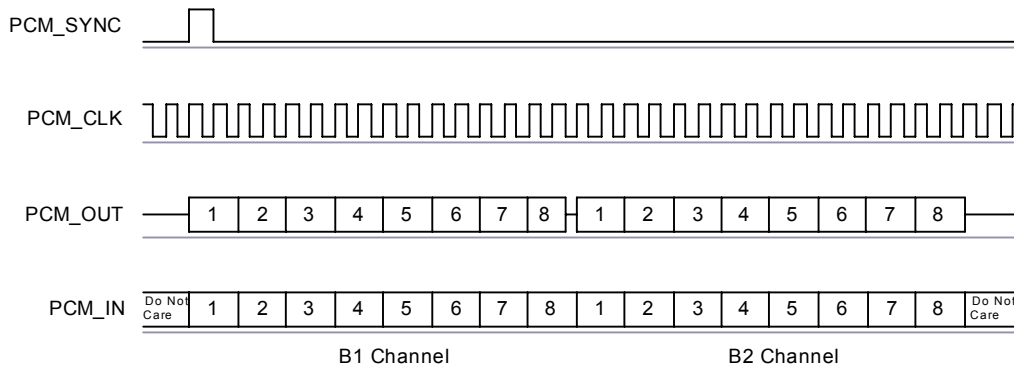


Figure 10.24: GCI Interface

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz. With BlueCore4-ROM in Slave mode, the frequency of PCM_CLK can be up to 4.096MHz.

10.7.6 Slots and Sample Formats

BlueCore4-ROM can receive and transmit on any selection of the first four slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Durations of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8, 13 or 16-bit sample formats.

BlueCore4-ROM supports 13-bit linear, 16-bit linear and 8-bit μ -law or A-law sample formats. The sample rate is 8ksamples/s. The bit order may be little or big Endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola CODECs.

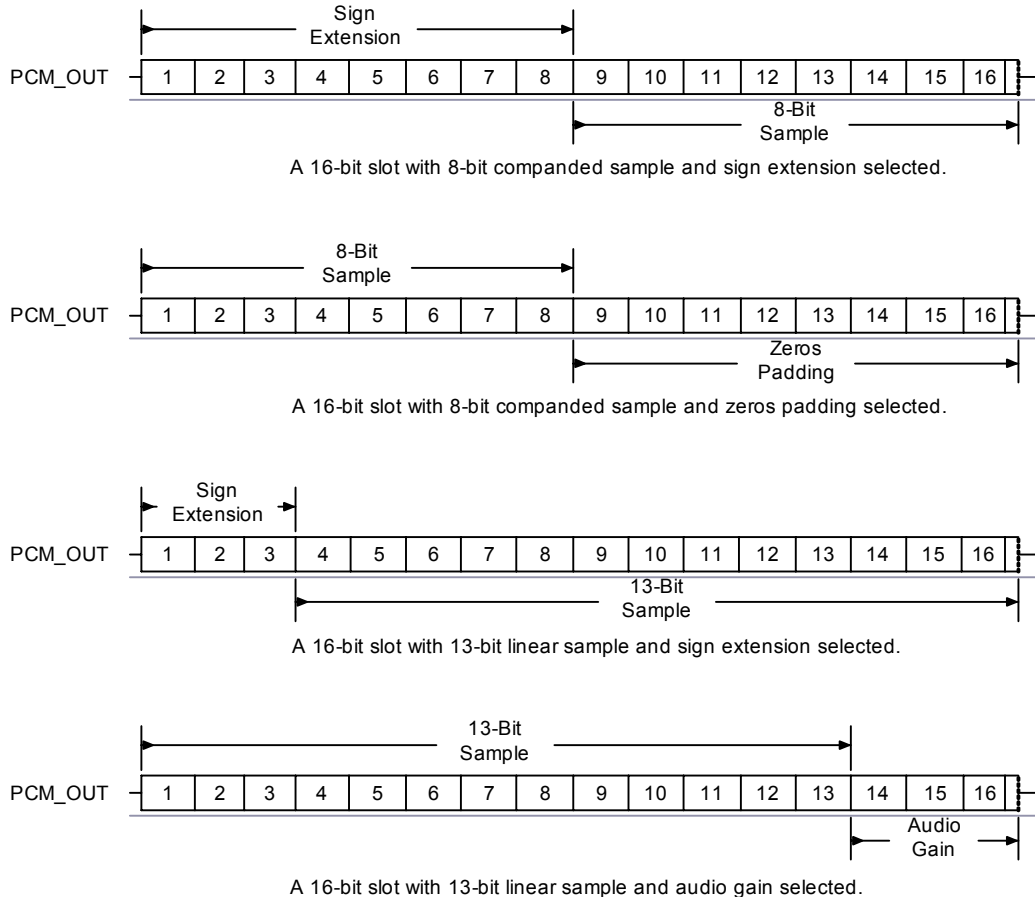


Figure 10.25: 16-Bit Slot Length and Sample Formats

10.7.7 Additional Features

BlueCore4-ROM has a mute facility that forces PCM_OUT to be 0. In Master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some CODECS use to control power down.

10.7.8 PCM Timing Information

Symbol	Parameter		Min	Typ	Max	Unit
f_{mclk}	PCM_CLK frequency	4MHz DDS generation. Selection of frequency is programmable, see Table 10.11	-	128 256 512	-	kHz
		48MHz DDS generation. Selection of frequency is programmable, see Table 10.12 and Section 10.7.10	2.9	-	-	kHz
-	PCM_SYNC frequency		-	8	-	kHz
$t_{mclkh}^{(1)}$	PCM_CLK high	4MHz DDS generation	980	-	-	ns
$t_{mckl}^{(1)}$	PCM_CLK low	4MHz DDS generation	730	-	-	ns
-	PCM_CLK jitter	48MHz DDS generation	-	-	21	ns pk-pk
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high		-	-	20	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
$t_{dmcklsyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)		-	-	20	ns
$t_{dmcklksyncl}$	Delay time from PCM_CLK high to PCM_SYNC low		-	-	20	ns
$t_{dmcklpoutz}$	Delay time from PCM_CLK low to PCM_OUT high impedance		-	-	20	ns
$t_{dmcklhpoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance		-	-	20	ns
$t_{supinckl}$	Set-up time for PCM_IN valid to PCM_CLK low		30	-	-	ns
$t_{hpinckl}$	Hold time for PCM_CLK low to PCM_IN invalid		10	-	-	ns

Table 10.9: PCM Master Timing

Note:

- (1) Assumes normal system clock operation. Figures will vary during low power modes, when system clock speeds are reduced.

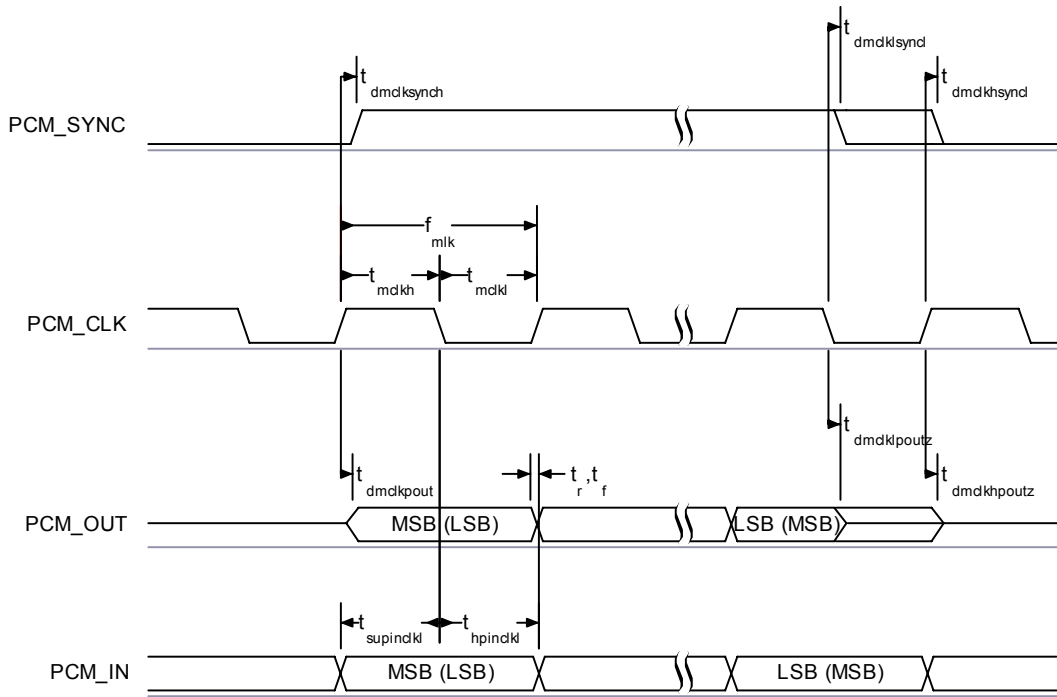


Figure 10.26: PCM Master Timing Long Frame Sync

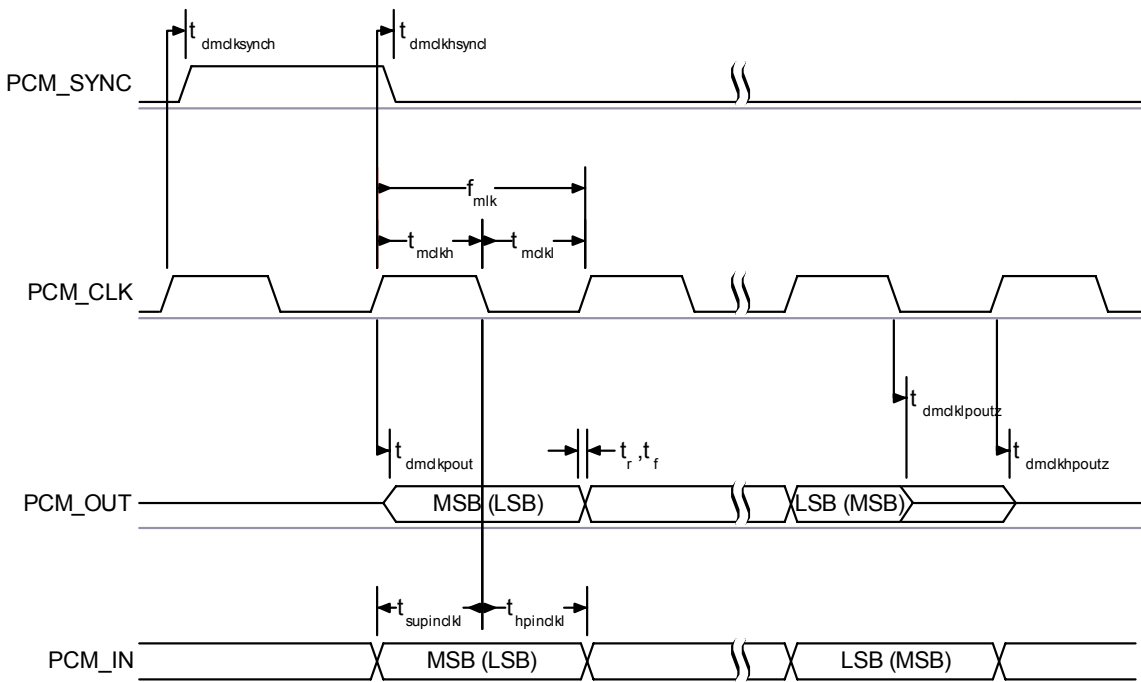


Figure 10.27: PCM Master Timing Short Frame Sync

10.7.9 PCM Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
f_{sclk}	PCM clock frequency (Slave mode: input)	64	-	2048	kHz
f_{sclk}	PCM clock frequency (GCI mode)	128	-	4096	kHz
t_{sckl}	PCM_CLK low time	200	-	-	ns
t_{sckh}	PCM_CLK high time	200	-	-	ns
$t_{hscklsynch}$	Hold time from PCM_CLK low to PCM_SYNC high	30	-	-	ns
$t_{suscklsynch}$	Set-up time for PCM_SYNC high to PCM_CLK low	30	-	-	ns
t_{dpout}	Delay time from PCM_SYNC or PCM_CLK whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
$t_{dscklhout}$	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
t_{dpoutz}	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsckl}$	Set-up time for PCM_IN valid to CLK low	30	-	-	ns
$t_{hpinsckl}$	Hold time for PCM_CLK low to PCM_IN invalid	30	-	-	ns

Table 10.10: PCM Slave Timing

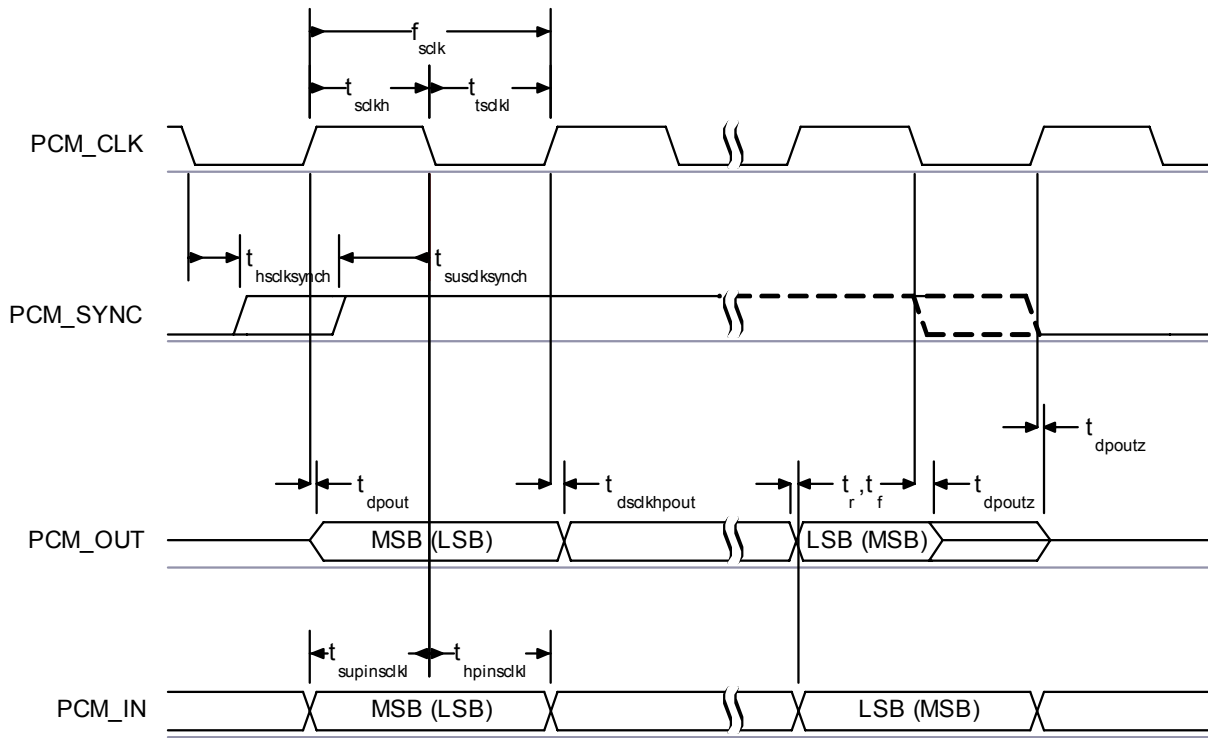


Figure 10.28: PCM Slave Timing Long Frame Sync

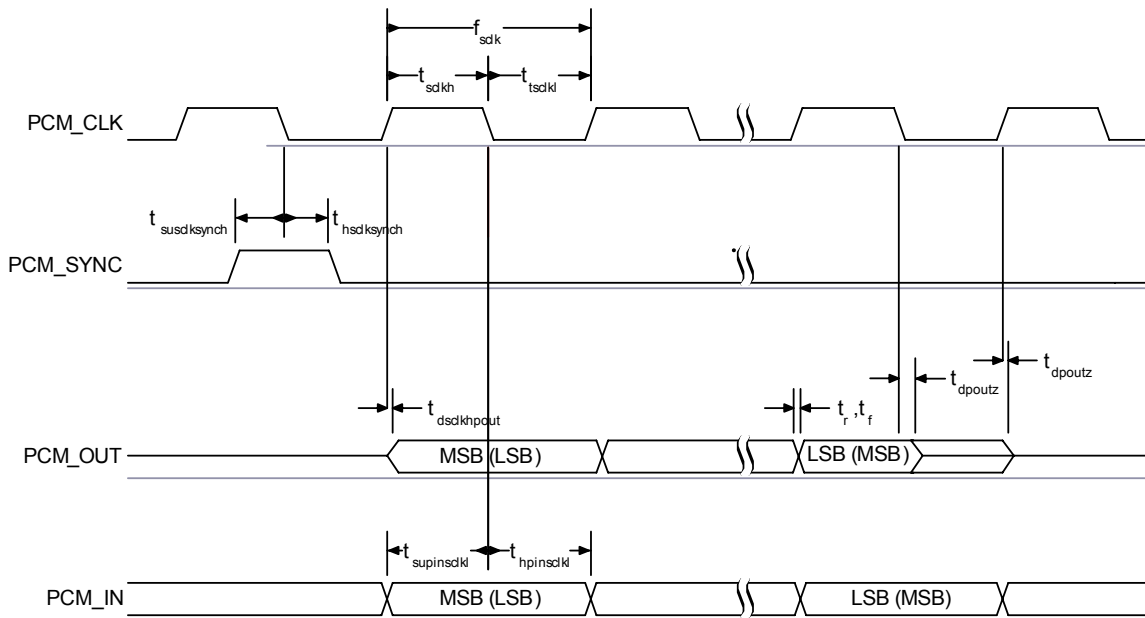


Figure 10.29: PCM Slave Timing Short Frame Sync

10.7.10 PCM_CLK and PCM_SYNC Generation

BlueCore4-ROM has two methods of generating PCM_CLK and PCM_SYNC in master mode. The first is generating these signals by Direct Digital Synthesis (DDS) from BlueCore4-ROM internal 4MHz clock. Using this mode limits PCM_CLK to 128, 256 or 512kHz and PCM_SYNC to 8kHz. The second is generating PCM_CLK and PCM_SYNC by DDS from an internal 48MHz clock which allows a greater range of frequencies to be generated with low jitter but consumes more power. This second method is selected by setting bit '48M_PCM_CLK_GEN_EN' in PSKEY_PCM_CONFIG32. When in this mode and with long frame sync, the length of PCM_SYNC can be either 8 or 16 cycles of PCM_CLK, determined by 'LONG_LENGTH_SYNC_EN' in PSKEY_PCM_CONFIG32.

The Equation 10.10 describes PCM_CLK frequency when being generated using the internal 48MHz clock:

$$f = \frac{\text{CNT_RATE}}{\text{CNT_LIMIT}} \times 24\text{MHz}$$

Equation 10.10: PCM_CLK Frequency When Being Generated Using the Internal 48MHz clock

The frequency of PCM_SYNC relative to PCM_CLK can be set using following equation:

$$f = \frac{\text{PCM_CLK}}{\text{SYNC_LIMIT} \times 8}$$

Equation 10.11: PCM_SYNC Frequency Relative to PCM_CLK

CNT_RATE, CNT_LIMIT and SYNC_LIMIT are set using PSKEY_PCM_LOW_JITTER_CONFIG. As an example, to generate PCM_CLK at 512kHz with PCM_SYNC at 8kHz, set PSKEY_PCM_LOW_JITTER_CONFIG to 0x08080177.

10.7.11 PCM Configuration

The PCM configuration is set using two PS Keys, PSKEY_PCM_CONFIG32 and PSKEY_PCM_LOW_JITTER_CONFIG. The following tables detail these PS Keys. PSKEY_PCM_CONFIG32. The default for this key is 0x00800000 i.e. first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tri-stating of PCM_OUT. PSKEY_PCM_LOW_JITTER_CONFIG is described in Table 10.12.

Name	Bit Position	Description
-	0	Set to 0.
SLAVE_MODE_EN	1	0 selects Master mode with internal generation of PCM_CLK and PCM_SYNC. 1 selects Slave mode requiring externally generated PCM_CLK and PCM_SYNC. This should be set to 1 if 48M_PCM_CLK_GEN_EN (bit 11) is set.
SHORT_SYNC_EN	2	0 selects long frame sync (rising edge indicates start of frame), 1 selects short frame sync (falling edge indicates start of frame).
-	3	Set to 0.
SIGN_EXTEND_EN	4	0 selects padding of 8 or 13-bit voice sample into a 16-bit slot by inserting extra LSBs, 1 selects sign extension. When padding is selected with 13-bit voice sample, the 3 padding bits are the audio gain setting; with 8-bit samples the 8 padding bits are zeroes.
LSB_FIRST_EN	5	0 transmits and receives voice samples MSB first, 1 uses LSB first.
TX_TRISTATE_EN	6	0 drives PCM_OUT continuously, 1 tri-states PCM_OUT immediately after the falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is not active.
TX_TRISTATE_RISING_EDGE_EN	7	0 tristates PCM_OUT immediately after the falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is also not active. 1 tristates PCM_OUT after the rising edge of PCM_CLK.
SYNC_SUPPRESS_EN	8	0 enables PCM_SYNC output when master, 1 suppresses PCM_SYNC whilst keeping PCM_CLK running. Some CODECS utilise this to enter a low power state.
GCI_MODE_EN	9	1 enables GCI mode.
MUTE_EN	10	1 forces PCM_OUT to 0.
48M_PCM_CLK_GEN_EN	11	0 sets PCM_CLK and PCM_SYNC generation via DDS from internal 4 MHz clock, as for BlueCore4-ROM. 1 sets PCM_CLK and PCM_SYNC generation via DDS from internal 48 MHz clock.
LONG_LENGTH_SYNC_EN	12	0 sets PCM_SYNC length to 8 PCM_CLK cycles and 1 sets length to 16 PCM_CLK cycles. Only applies for long frame sync and with 48M_PCM_CLK_GEN_EN set to 1.
-	[20:16]	Set to 0b00000.
MASTER_CLK_RATE	[22:21]	Selects 128 (0b01), 256 (0b00), 512 (0b10) kHz PCM_CLK frequency when master and 48M_PCM_CLK_GEN_EN (bit 11) is low.
ACTIVE_SLOT	[26:23]	Default is '0001'. Ignored by firmware.
SAMPLE_FORMAT	[28:27]	Selects between 13 (0b00), 16 (0b01), 8 (0b10) bit sample with 16 cycle slot duration or 8 (0b11) bit sample with 8 cycle slot duration.

Table 10.11: PSKEY_PCM_CONFIG32 Description

Name	Bit Position	Description
CNT_LIMIT	[12:0]	Sets PCM_CLK counter limit.
CNT_RATE	[23:16]	Sets PCM_CLK count rate.
SYNC_LIMIT	[31:24]	Sets PCM_SYNC division relative to PCM_CLK.

Table 10.12: PSKEY_PCM_LOW_JITTER_CONFIG Description

10.8 I/O Parallel Ports

Fifteen lines of programmable bi-directional input/outputs (I/O) are provided. PIO[11:8] and PIO[3:0] are powered from VDD_PIO. PIO[7:4] are powered from VDD_PADS. AIO [2:0] are powered from VDD_USB.

PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs. All PIO lines are configured as inputs with weak pull-downs at reset.

PIO[0] and PIO[1] are normally dedicated to RXEN and TXEN respectively, but they are available for general use.

Any of the PIO lines can be configured as interrupt request lines or as wake-up lines from sleep modes. PIO[6] or PIO [2] can be configured as a request line for an external clock source. This is useful when the clock to BlueCore4-ROM is provided from a system application specific integrated circuit (ASIC).

BlueCore4-ROM has three general purpose analogue interface pins, AIO[0], AIO[1] and AIO[2]. These are used to access internal circuitry and control signals. One pin is allocated to decoupling for the on-chip band gap reference voltage, the other three may be configured to provide additional functionality.

Auxiliary functions available via these pins include an 8-bit ADC and an 8-bit DAC. Typically the ADC is used for battery voltage measurement. Signals selectable at these pins include the band gap reference voltage and a variety of clock signals; 48, 24, 16, 8MHz and the XTAL clock frequency. When used with analogue signals the voltage range is constrained by the analogue supply voltage (1.8V). When configured to drive out digital level signals (clocks) generated from within the analogue part of the device, the output voltage level is determined by VDD_MEM (1.8V).

10.8.1 PIO Defaults for BTv2.0 + EDR HCI Level Bluetooth Stack

CSR cannot guarantee that these terminal functions remain the same. Please refer to the software release note for the implementation of these PIO lines, as they are firmware build specific.

10.9 I²C Interface

PIO[8:6] can be used to form a Master I²C interface. The interface is formed using software to drive these lines. Therefore it is suited only to relatively slow functions such as driving a dot matrix liquid crystal display (LCD), keyboard scanner or EEPROM.

Note:

PIO[7:6] dual functions, UART bypass and EEPROM support, therefore devices using an EEPROM cannot support UART bypass mode

PIO lines need to be pulled-up through 2.2kΩ resistors.

For connection to EEPROMs, refer to CSR documentation on I²C EEPROMS for use with BlueCore. This provides information on the type of devices which are currently supported.

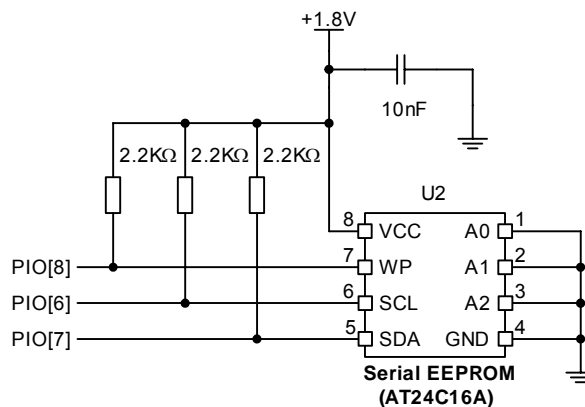


Figure 10.30: Example EEPROM Connection

10.10 TCXO Enable OR Function

An OR function exists for clock enable signals from a host controller and BlueCore4-ROM where either device can turn on the clock without having to wake up the other device. PIO[3] can be used as the Host clock enables input and PIO[2] can be used as the OR output with the TCXO enable signal from BlueCore4-ROM.

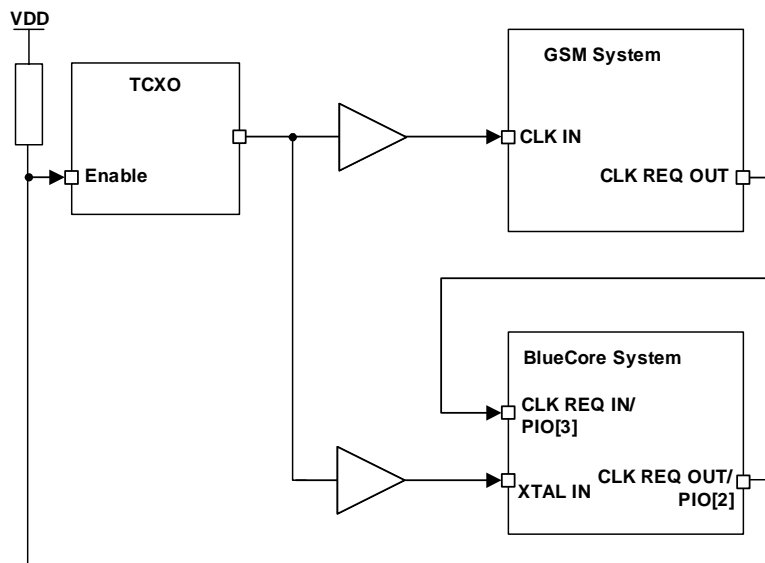


Figure 10.31: Example TXCO Enable OR Function

On reset and up to the time the PIO has been configured, PIO[2] will be tri-stated. Therefore, the developer must ensure that the circuitry connected to this pin is pulled via a 470k Ω resistor to the appropriate power rail. This ensures that the TCXO is oscillating at start up.

10.11 RESET and RESETB

BlueCore4-ROM may be reset from several sources: RESET or RESETB pins, power on reset, a UART break character or via a software configured watchdog timer.

The RESET pin is an active high reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESET being active. CSR recommends that RESET is applied for a period greater than 5ms. The RESETB pin is the active low version of RESET and is 'Ored' on-chip with the active high RESET with either causing the reset function.

The power on reset occurs when the VDD_CORE supply falls below typically 1.5V and is released when VDD_CORE rises above typically 1.6V.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-stated. The PIOs have weak pull-downs.

Following a reset, BlueCore4-ROM assumes the maximum XTAL_IN frequency, which ensures that the internal clocks run at a safe (low) frequency until BlueCore4-ROM is configured for the actual XTAL_IN frequency. If no clock is present at XTAL_IN, the oscillator in BlueCore4-ROM free runs, again at a safe frequency.

10.11.1 Pin States on Reset

Table 10.13 shows the pin states of BlueCore4-ROM on reset.

Pin Name	State: BlueCore4-ROM
PIO[11:0]	Input with weak pull-down
PCM_OUT	Tri-stated with weak pull-down
PCM_IN	Input with weak pull-down
PCM_SYNC	Input with weak pull-down
PCM_CLK	Input with weak pull-down
UART_TX	Output tri-stated with weak pull-up
UART_RX	Input with weak pull-down
UART_RTS	Output tri-stated with weak pull-up
UART_CTS	Input with weak pull-down
USB_DP	Input with weak pull-down
USB_DN	Input with weak pull-down
SPI_CSB	Input with weak pull-up
SPI_CLK	Input with weak pull-down
SPI_MOSI	Input with weak pull-down
SPI_MISO	Output tri-stated with weak pull-down
AIO[2:0]	Output, driving low
RESET	Input with weak pull-down
RESETB	Input with weak pull-up
TEST_EN	Input with strong pull-down
AUX_DAC	High impedance
TX_A	High impedance
TX_B	High impedance
RF_IN	High impedance
XTAL_IN	High impedance, 250k to XTAL_OUT
XTAL_OUT	High impedance, 250k to XTAL_IN

Table 10.13: Pin States of BlueCore4-ROM on Reset

10.11.2 Status after Reset

The chip status after a reset is as follows:

- Warm Reset: Baud rate and RAM data remain available
- Cold Reset⁽¹⁾: Baud rate and RAM data not available

Note:

⁽¹⁾ Cold Reset constitutes one of the following:

- Power cycle
- System reset (firmware fault code)
- Reset signal, see Section 10.11.

10.12 Power Supplies

BlueCore4-ROM contains a 1.8V regulator which may be used to power the 1.8V supplies of the device. The device pin VREG_EN is used to enable and disable the regulator. Alternatively an external 1.8V voltage source may be used.

10.12.1 Supply Domains and Sequencing

The 1.8V supplies are VDD_ANA, VDD_VCO, VDD_RADIO and VDD_CORE. It is recommended that the 1.8V supplies are all powered at the same time. The order of powering the 1.8V supplies relative to the other IO supplies (VDD_PIO, VDD_PADS, VDD_USB) is not important, however if the IO supplies are powered before the 1.8V supplies all digital IO will have a weak pull-down irrespective of the reset state.

10.12.2 External Voltage Source

If the 1.8V rails of BlueCore4-ROM are supplied from an external voltage source, it is recommended that VDD_VCO, VDD_RADIO, and VDD_ANA, should have less than 10mV rms noise levels between 0 to 10MHz. Single tone frequencies are also to be avoided.

The transient response of any regulator used should be 20 μ s or less. It is essential that the power rail recovers quickly at the start of a packet, where the power consumption will jump to high levels (see average current consumption section).

10.12.3 Linear Regulator

The on-chip 1.8V linear regulator may be used to power the 1.8V dependent supplies. It is advised that a smoothing circuit using a series connected 2.2 μ F low ESR capacitor and a 2.2 Ω resistor to ground is placed on the output of the regulator VDD_ANA.

The regulator is switched into a low power mode when the device is sent into deep-sleep mode.

When this regulator is not used the terminal VREG_IN must be connected to VDD_ANA or left unconnected.

10.12.4 VREG_EN Pin

The regulator enable pin, VREG_EN, can be used to enable and disable the BlueCore4-ROM device if one of the on-chip regulators is being used. The pin is active high, and has a weak pull-up to the active regulator input.

11 Application Schematic

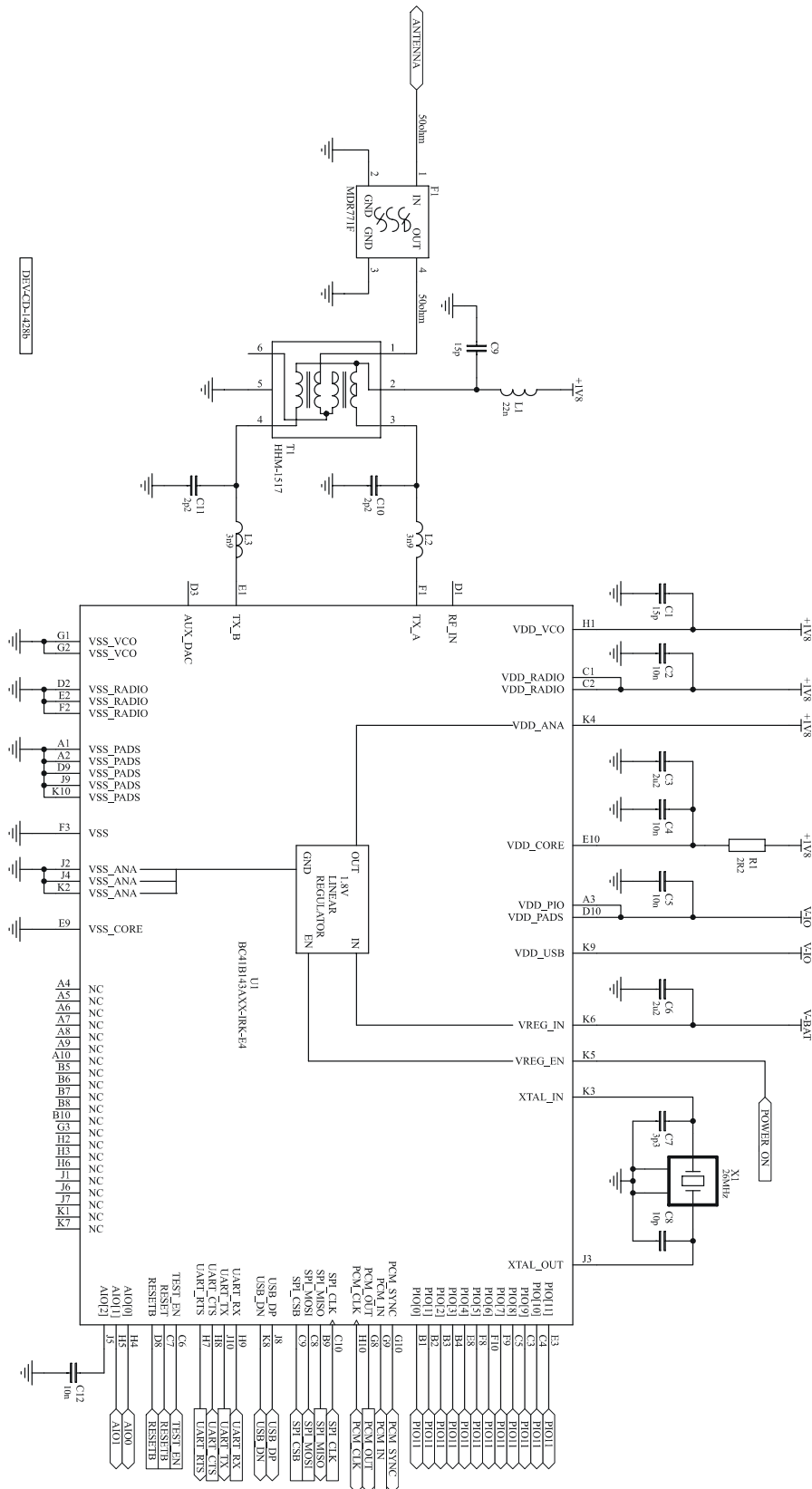
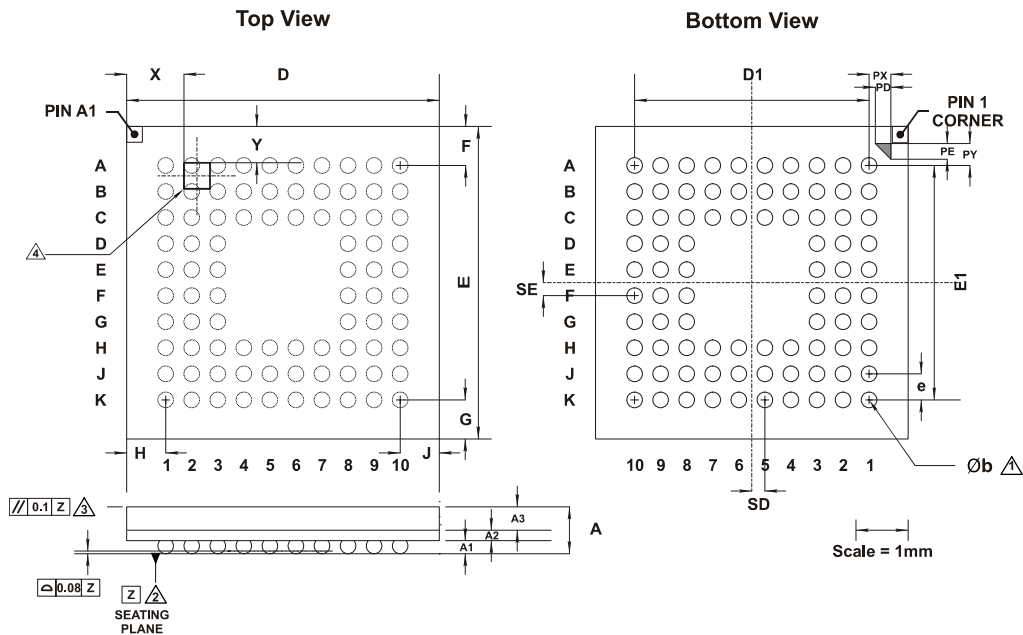


Figure 11.1: Application Circuit for Radio Characteristics Specification with 6 x 6mm VFBGA Package

12 Package Dimensions

12.1 6 x 6mm VFBGA 84-Ball Package



Description		84-Ball Very-Thin Fine-Pitch Ball Grid Array (VFBGA)		
Size		6 x 6 x 1mm		
Pitch		0.5mm		
Dimension	Minimum	Typical	Maximum	Notes
A	0.8	0.9	1.0	⚠ Dimension b is measured at the maximum solder ball diameter parallel to datum plane Z
A1	0.2	0.25	0.3	
A2		0.22		
A3		0.45		
b	0.25	0.30	0.35	⚠ Datum Z is defined by the spherical crowns of the solder balls
D	5.90	6.00	6.10	
E	5.90	6.00	6.10	⚠ Parallelism measurement shall exclude any effect of mark on top surface of package
e		0.50		
D1		4.50		⚠ Polarity Mark. The dimensions of the polarity mark are 0.5 x 0.5mm.
E1		4.50		
F	0.700	0.750	0.800	
G	0.700	0.750	0.800	
H	0.700	0.750	0.800	
J	0.700	0.750	0.800	
PD		0.300		
PX		0.420		
PE		0.300		
PY		0.420		
SD		0.25		
SE		0.25		
X		1.10		
Y		0.70		
JEDEC	MO-225			
Unit	mm			

Figure 12.1: BlueCore4-ROM 84-Ball VFBGA Package Dimensions

13 Solder Profiles

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder re-flow. The four zones are described in Table 13.1

Preheat Zone	This zone raises the temperature at a controlled rate, typically 1-2.5°C/s.
Equilibrium Zone	This zone brings the board to a uniform temperature and also activates the flux. The duration in this zone (typically 2-3 minutes) will need to be adjusted to optimise the out gassing of the flux.
Reflow Zone	The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint
Cooling Zone	The cooling rate should be fast, to keep the solder grains small which will give a longer lasting joint. Typical rates will be 2-5°C/s.

Table 13.1: Soldering Profile Zones

13.1 Solder Re-Flow Profile for Devices with Lead-Free Solder Balls

Composition of the solder ball: Sn 95.5%, Ag 4.0%, Cu 0.5%

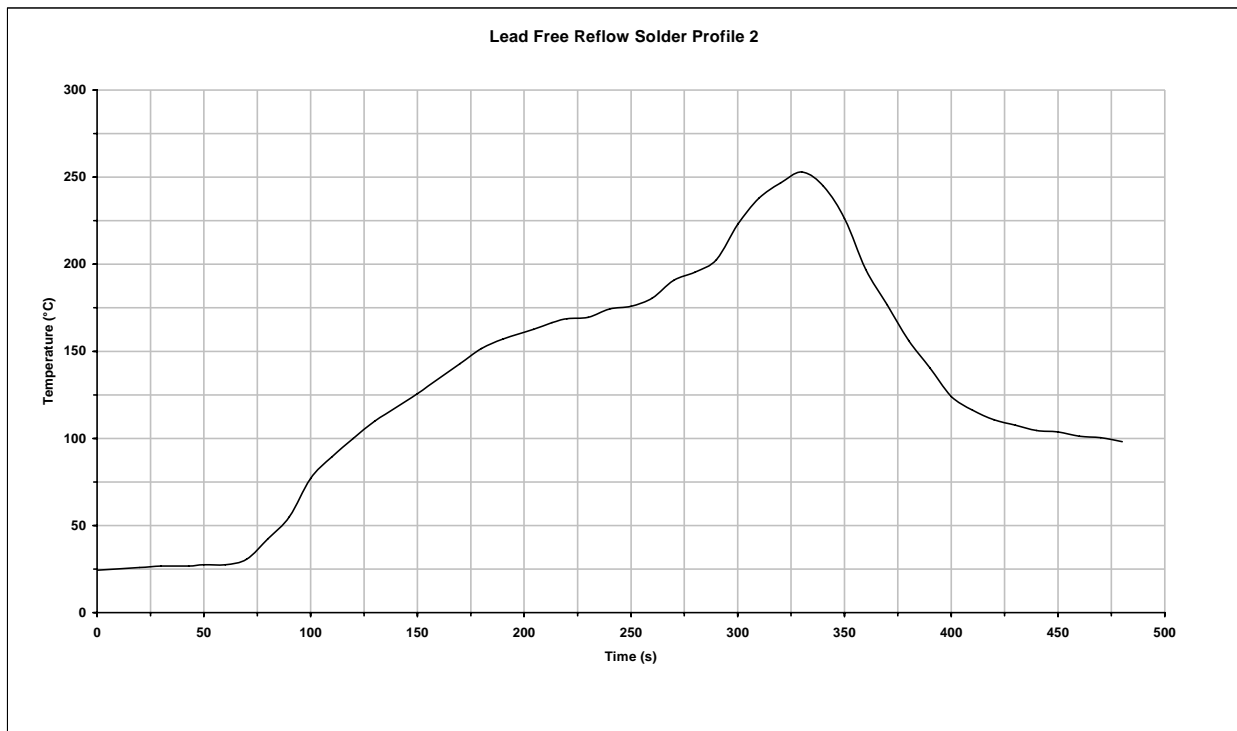


Figure 13.1: Typical Lead-Free Re-flow Solder Profile

Key features of the profile:

- Initial Ramp = 1-2.5°C/sec to 175°C±25°C equilibrium
- Equilibrium time = 60 to 180 seconds
- Ramp to Maximum temperature (250°C) = 3°C/sec max.
- Time above liquidus temperature (217°C): 45-90 seconds
- Device absolute maximum reflow temperature: 260°C

Devices will withstand the specified profile. Lead-free devices will withstand up to three reflows to a maximum temperature of 260°C.

14 Ordering Information

14.1 BlueCore4-ROM

Interface Version	Package			Order Number
	Type	Size	Shipment Method	
UART and USB	84-Ball VFBGA (Pb free)	6 x 6mm x 1mm	Tape and reel	BC41B143A05-IRK-E4

Minimum Order Quantity

2kpcs Taped and Reeled

15 Tape and Reel Information

Tape and reel is in accordance with EIA-481-2.

15.1 Tape Orientation and Dimensions

The general orientation of the BGA in the tape is as shown in Figure 15.1.

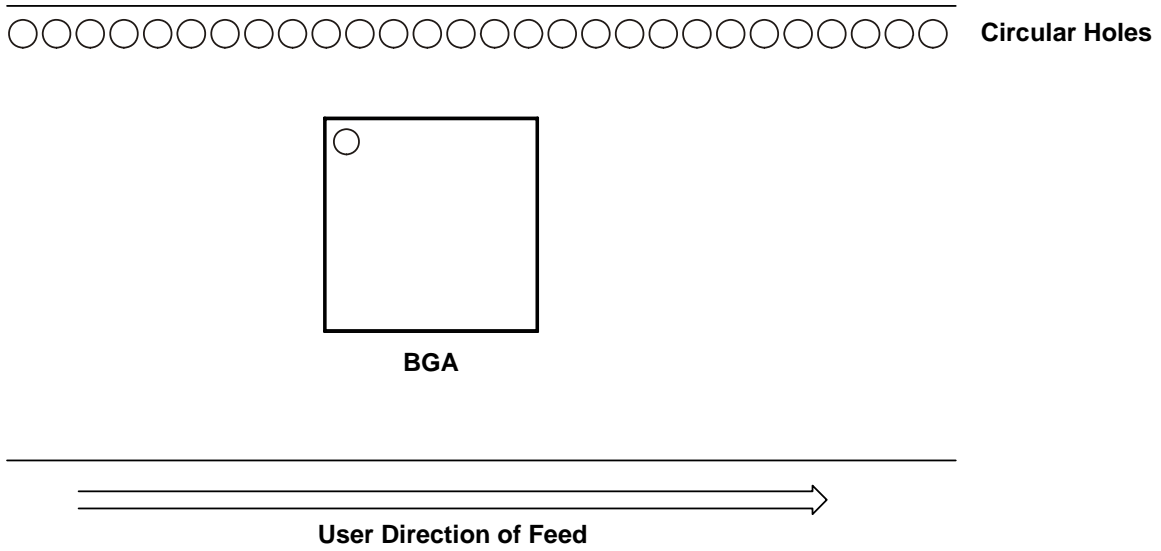
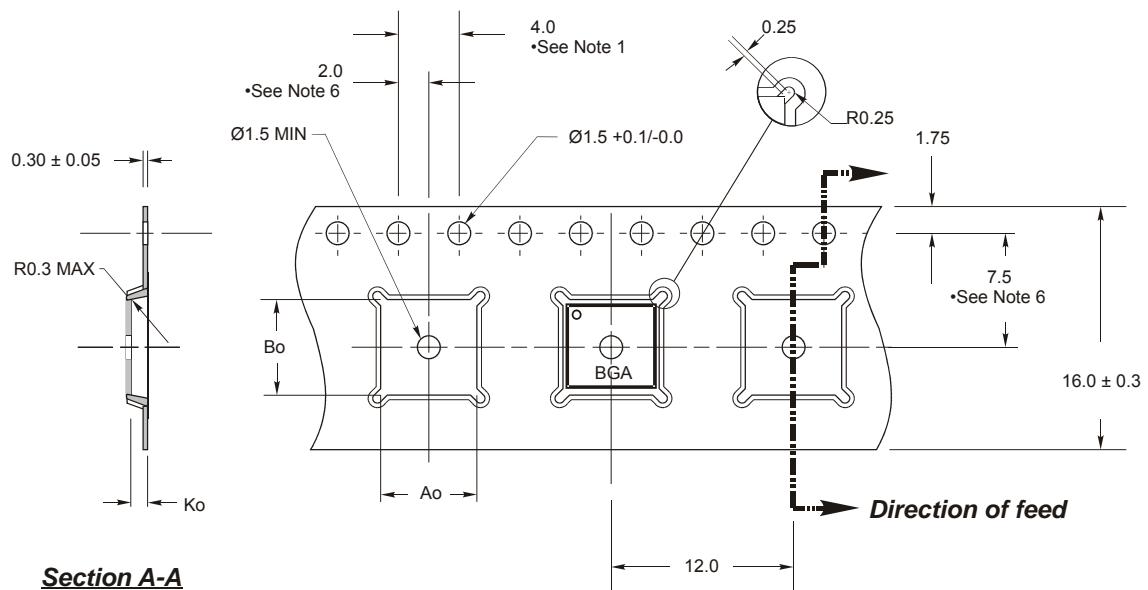


Figure 15.1: Tape and Reel Orientation

As a detailed example, the diagram shown in Figure 15.2 outlines the dimensions of the tape used for 6 x 6mm x 1mm VFBGA devices:



Notes:

1. 10 sprocket hole pitch cumulative tolerance ± 0.2 .
2. Camber not to exceed 1mm in 100mm.
3. Material: PS + C.
4. A_o and B_o measured as indicated.
5. K_o measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

$A_o = 6.3$ mm
 $B_o = 6.3$ mm
 $K_o = 1.1$ mm

Figure 15.2: Tape Dimensions

The cover tape has a total peel strength of 0.1N to 1.3N. The direction of the pull should be opposite the direction of the carrier tape such that the cover tape makes an angle of between 165° and 180° with the top of the carrier tape. The carrier and/or cover tape should be pulled with a velocity of 300±10mm during peeling.

Maximum component rotation inside the cavity is 10° in accordance with EIA-481-2. The cavity pitch tolerance (dimension P1) is ± 0.1 mm.

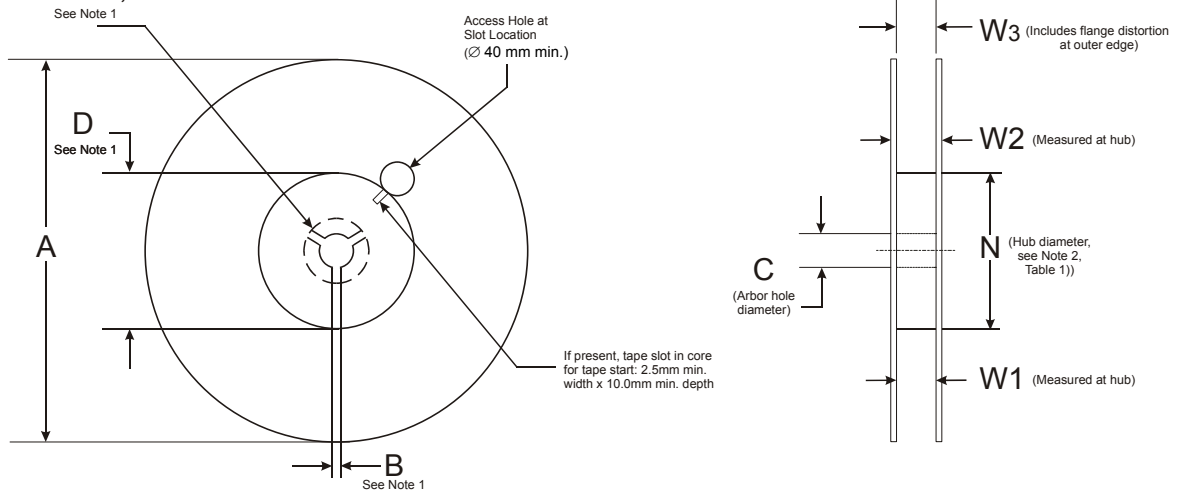
The reel is made of high impact injection moulded polystyrene. The carrier tape is made of polystyrene with carbon. The cover tape is made of antistatic polyester film and an antistatic heat activated adhesive coating.

15.2 Reel Information

Reel dimensions

(All dimensions in millimeters)

Full Radius,



Notes:

1. Drive spokes optional; if used, dimensions B and D shall apply.
2. Maximum weight of reel and contents 13.6kg.

Figure 15.3: Reel Dimensions

Tape Width	B Min	C	D Min	N Min	W1
16mm	1.5mm	13.0+0.5/-0.2mm	20.2mm	50mm	16.4+2.0/-0.0mm

Table 15.1: Reel Dimensions

Reel Diameter, A		
330mm		
Tape Size	W2 Max	W3
16mm	22.4mm	15.9mm Min 19.4mm Max

Table 15.2: Diameter Dependent Dimensions

15.3 Dry Pack Information

The primary packed product is dry packed in accordance with Joint IPC / JEDEC J-STD-033.

All materials used in dry packing conform to EIA-541 and EIA-583.

Some illustrative views of reel dry packs are shown in Figure 15.4.

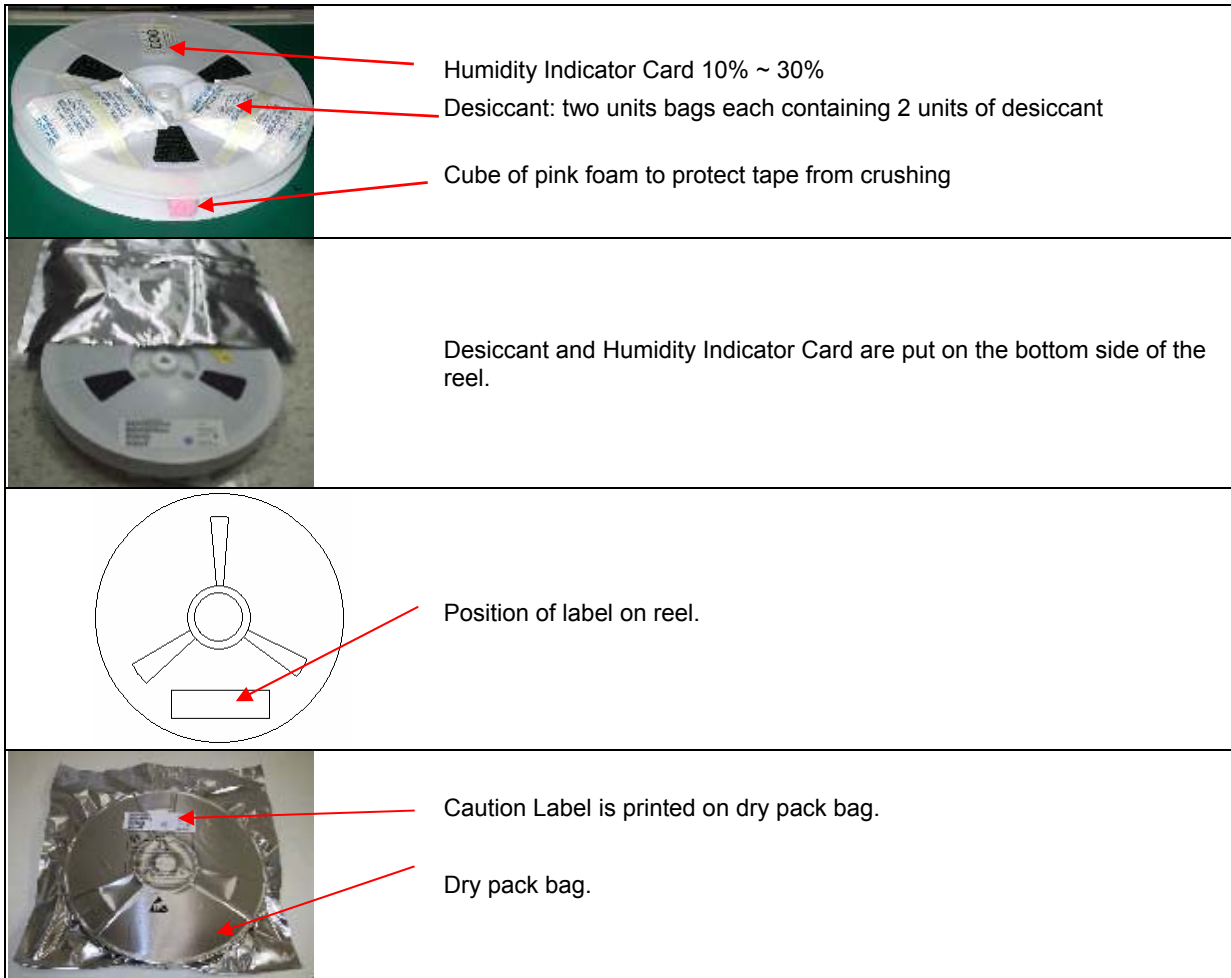


Figure 15.4: Tape and Reel Packaging

Devices shipped in dry-pack bags will withstand storage in normal environmental conditions, such as 30°C and 70% RH for a minimum of one year as long as the dry-pack bag has not become punctured. Humidity indicators inside the dry-pack bag will confirm this when the bag is opened.

15.4 Baking Conditions

Devices may, if necessary, be re-baked at 125°C for 24 hours. If devices are still on the reel, which cannot withstand such high temperatures, they should be baked at 45°C for 192 hours at relative humidity less than 5%.

Solder wettability of parts will be unaffected by three such bakes.

15.5 Product Information

Example product information labels are shown in Figure 15.5.

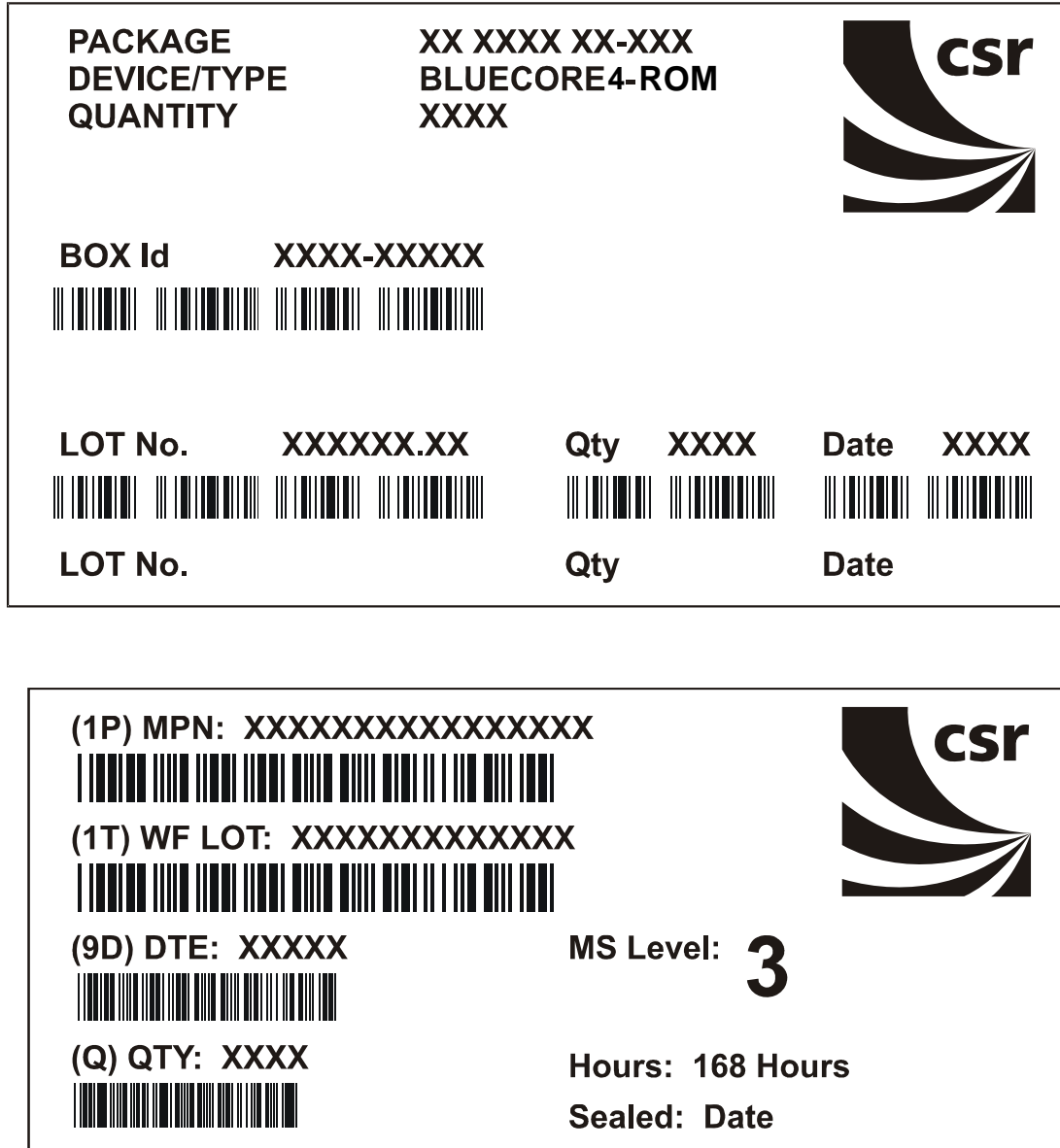


Figure 15.5: Product Information Labels

A product information label is placed on each reel, primary package and shipment package

16 Contact Information

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To contact a CSR representative, go to <http://www.csr.com/contacts.htm>

17 Document References

Document:	Reference, Date:
Specification of the Bluetooth System	v1.2, 05 November 2003
Specification of the Bluetooth System	V2.0 + EDR, 04 November 2004
Universal Serial Bus Specification	v2.0, 27 April 2000
Selection of I ² C EEPROMS for Use with BlueCore	bcore-an-008Pb, 30 September 2003
RF Test Specification v2.0.E.2	v2.0.E.2, 04 November 2004

Terms and Definitions

8DPSK	8 phase Differential Phase Shift Keying
$\pi/4$ DQPSK	$\pi/4$ rotated Differential Quaternary Phase Shift Keying
BlueCore™	Group term for CSR's range of Bluetooth chips
Bluetooth™	Set of technologies providing audio and data transfer over short-range radio connections
CSR	Cambridge Silicon Radio
ACL	Asynchronous Connection-Less. A Bluetooth data packet.
ADC	Analogue to Digital Converter
AGC	Automatic Gain Control
A-law	Audio encoding standard
API	Application Programming Interface
ASIC	Application Specific Integrated Circuit
BCSP	BlueCore™ Serial Protocol
BER	Bit Error Rate. Used to measure the quality of a link
BIST	Built-In Self-Test
BMC	Burst Mode Controller
CMOS	Complementary Metal Oxide Semiconductor
CODEC	Coder Decoder
CSB	Chip Select (Active Low)
CSR	Cambridge Silicon Radio
CTS	Clear to Send
CVSD	Continuous Variable Slope Delta Modulation
DAC	Digital to Analogue Converter
dBm	Decibels relative to 1mW
DC	Direct Current
DEVm	Differential Error Vector Magnitude
DFU	Device Firmware Upgrade
DPSK	Differential Phase Shift Keying
DQPSK	Differential Quaternary Phase Shift Keying
ESR	Equivalent Series Resistance
FSK	Frequency Shift Keying
GSM	Global System for Mobile communications
HCI	Host Controller Interface
IQ Modulation	In-Phase and Quadrature Modulation
IF	Intermediate Frequency
IIR	Infinite Impulse Response
ISDN	Integrated Services Digital Network
ISM	Industrial, Scientific and Medical
ksps	KiloSamples Per Second
L2CAP	Logical Link Control and Adaptation Protocol (protocol layer)
LC	Link Controller
LCD	Liquid Crystal Display
LFBGA	Low profile Fine Ball Grid Array
LNA	Low Noise Amplifier

LPF	Low Pass Filter
LSB	Least-Significant Bit
μ-law	Audio Encoding Standard
MCU	MicroController Unit
MMU	Memory Management Unit
MISO	Master In Serial Out
MOSI	Master Out Slave In
Mbps	Mega bits per second
OHCI	Open Host Controller Interface
PA	Power Amplifier
PCM	Pulse Code Modulation. Refers to digital voice data
PIO	Parallel Input Output
PLL	Phase Lock Loop
ppm	parts per million
PS Key	Persistent Store Key
RAM	Random Access Memory
REB	Read enable (Active Low)
REF	Reference. Represents dimension for reference use only.
RF	Radio Frequency
RFCOMM	Protocol layer providing serial port emulation over L2CAP
RISC	Reduced Instruction Set Computer
rms	root mean squared
RoHS	The Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC)
RSSI	Receive Signal Strength Indication
RTS	Ready To Send
RX	Receive or Receiver
SCO	Synchronous Connection-Oriented. Voice oriented Bluetooth packet
SD	Secure Digital
SDK	Software Development Kit
SDP	Service Discovery Protocol
SPI	Serial Peripheral Interface
TBA	To Be Announced
TBD	To Be Defined
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus or Upper Side Band (depending on context)
VCO	Voltage Controlled Oscillator
VM	Virtual Machine
W-CDMA	Wideband Code Division Multiple Access
WEB	Write Enable (Active Low)
www	world wide web

Document History

Date:	Revision	Reason for Change:
JUL 04	a	Original publication of Advance Information Product Data Sheet (CSR reference: BC41B143A-ds-001Pa)
OCT 04	b	Corrected H1 and H2 ball assignments in section 2.2. (CSR reference: BC41B143A-ds-001Pb)
JAN 05	c	Corrected synthesiser information in Key Features. Updated Contact Information section. Changed EDR specification to latest release.
MAY 05	d	Amended footnote to Linear Regulator table concerning VREG_IN in Electrical Characteristics.
JULY 05	e	<p>Data Sheet raised to Production status.</p> <p>Major changes include:</p> <ul style="list-style-type: none"> ▪ Electrical Characteristics and Power Consumption updated ▪ Basic Data Rate Radio Characteristics updated ▪ Enhanced Data Rate Radio Characteristics updated ▪ Typical Radio Performance – Basic Data Rate section added ▪ Application Schematic added

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