



# Speed-Switching Clock Generator with Power Fail

MAX7391

## General Description

The MAX7391 replaces ceramic resonators, crystals, and supervisory functions for microcontrollers in 3.3V and 5V applications.

The MAX7391 provides a clock source, reset, and power-fail functions. The programmable power-fail function provides early warning of power failure and is configurable to detect either an external voltage or the VCC supply to the device.

The clock output can be switched between normal and half-speed operation. This functionality allows the microcontroller to operate at reduced power and may be used to extend the time available to perform house-keeping tasks, such as writing data to flash during a power failure. Connecting the power-fail output to the SPEED input reduces clock speed automatically during power-fail events.

The MAX7391 clock output is factory programmed to a frequency in the 1MHz to 16MHz range. Four standard frequencies are available. Other frequencies are available upon request. The maximum operating supply current is 5.5mA (typ) with a clock frequency of 12MHz.

Unlike typical crystal and ceramic resonator oscillator circuits, the MAX7391 is resistant to EMI and vibration, and operates reliably at high temperatures. The high-output drive current and absence of high-impedance nodes make the oscillator invulnerable to dirty or humid operating conditions.

The MAX7391 is available in an 8-pin  $\mu$ MAX<sup>®</sup> package. The MAX7391 standard operating temperature range is from -40°C to +125°C.

## Applications

White Goods  
Automotive  
Appliances and Controls  
Handheld Products  
Portable Equipment  
Microcontroller Systems

**Typical Application Circuit, Functional Diagram, and Selector Guide appear at end of data sheet.**

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## Features

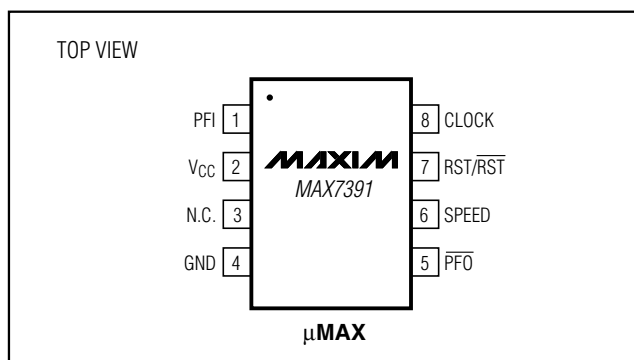
- ◆ Robust Microcontroller Clock and Supervisory Functions in a Single Package
- ◆ Integrated Reset and Power-Fail Functions
- ◆ Speed Select
- ◆ +2.7V to +5.5V Operation
- ◆ Factory-Trimmed Oscillator
- ◆ Reset Valid Down to 1.1V Supply Voltage
- ◆  $\pm 10$ mA Clock-Output Drive Current
- ◆  $\pm 4\%$  Total Accuracy for -40°C to +125°C
- ◆  $\pm 2.75\%$  Total Accuracy for 0°C to +85°C
- ◆ 5.5mA Operating Current (12MHz Version)
- ◆ -40°C to +125°C Temperature Range
- ◆ Surface-Mount Package
- ◆ 1MHz to 16MHz Factory Preset Frequency Range

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX7391srff	-40°C to +125°C	8 $\mu$ MAX	U8-1

**Note:** "s" is a placeholder for the reset output type. Insert the symbol found in Table 2 in the place of "s." "r" is a placeholder for the power-on reset (POR) voltage. Insert the symbol found in Table 1 in the place of "r." "ff" is a placeholder for the nominal output frequency. Insert the symbol found in Table 3 in the place of "ff." For example, MAX7391CMTP describes a device with 4.38V reset level, open-collector  $\overline{RST}$  output, and a clock output frequency of 8MHz.

## Pin Configuration



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## ABSOLUTE MAXIMUM RATINGS

V<sub>CC</sub> to GND .....-0.3V to +6.0V  
 All Other Pins to GND .....-0.3V to (V<sub>CC</sub> + 0.3V)  
 CLOCK, RST/ $\overline{\text{RST}}$ , PFO Output Current ..... $\pm 50\text{mA}$   
 Continuous Power Dissipation  
 8-Pin  $\mu\text{MAX}$  (derate 4.5mW/°C over T<sub>A</sub> = +70°C).....362mW

Operating Temperature Range .....-40°C to +125°C  
 Junction Temperature .....+150°C  
 Storage Temperature Range .....-65°C to +150°C  
 Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(Typical Application Circuit, V<sub>CC</sub> = +2.7V to +5.5V, T<sub>A</sub> = -40°C to +125°C, 1MHz to 16MHz output frequency range, typical values at V<sub>CC</sub> = +5.0V, T<sub>A</sub> = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER REQUIREMENTS</b>						
Operating Supply Voltage	V <sub>CC</sub>		2.7		5.5	V
Valid RST/ $\overline{\text{RST}}$ Supply Voltage	V <sub>CCR</sub>	Minimum supply voltage for valid RST/ $\overline{\text{RST}}$ output, T <sub>A</sub> = 0°C to +85°C			1.1	V
Operating Supply Current	I <sub>CC</sub>	f <sub>CLOCK</sub> = 12MHz			5.5	mA
		f <sub>CLOCK</sub> = 8MHz			4.5	
<b>LOGIC INPUT: SPEED</b>						
Input Leakage Current	I <sub>LEAK</sub>	Input is high			0.5	μA
Logic-Input High Voltage	V <sub>IH</sub>		0.7 x V <sub>CC</sub>			V
Logic-Input Low Voltage	V <sub>IL</sub>				0.3 x V <sub>CC</sub>	V
<b>PUSH-PULL LOGIC OUTPUTS: RST/<math>\overline{\text{RST}}</math></b>						
Output High	V <sub>OH</sub>	I <sub>SOURCE</sub> = 1mA	V <sub>CC</sub> - 1.5			V
Output Low	V <sub>OL</sub>	I <sub>SINK</sub> = 3mA		0.05	0.4	V
<b>OPEN-DRAIN LOGIC OUTPUTS: RST, PFO</b>						
Output Low	V <sub>OLO</sub>	I <sub>SINK</sub> = 3mA		0.05	0.4	V
<b>OUTPUT: CLOCK</b>						
CLOCK Output High Voltage	V <sub>OHC</sub>	I <sub>SOURCE</sub> = 5mA	V <sub>CC</sub> - 0.3			V
CLOCK Output Low Voltage	V <sub>OLC</sub>	I <sub>SINK</sub> = 5mA			0.3	V
CLOCK Accuracy	f <sub>CLOCK</sub>	Table 3, V <sub>CC</sub> = +5.0V	-4		+4	%

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## ELECTRICAL CHARACTERISTICS (continued)

(Typical Application Circuit,  $V_{CC} = +2.7V$  to  $+5.5V$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ , 1MHz to 16MHz output frequency range, typical values at  $V_{CC} = +5.0V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Frequency Temperature Coefficient		$V_{CC} = +5.0V$ (Note 2)		140	400	ppm/ $^{\circ}C$
Clock Frequency Supply Voltage Coefficient		$T_A = +25^{\circ}C$ (Note 2)		0.67	1	%/V
CLOCK Duty Cycle		(Note 2)	45	50	55	%
CLOCK Output Jitter		Observation for 20s using a 500MHz oscilloscope		310		ps RMS
Output Rise Time	$t_R$	$C_{LOAD} = 10pF$ , 10% to 90% of full scale (Note 2)		2.5	7.0	ns
Output Fall Time	$t_F$	$C_{LOAD} = 10pF$ , 90% to 10% of full scale (Note 2)		2.5	7.5	ns
<b>INTERNAL POWER-ON RESET</b>						
Reset Voltage	$V_{TH+}$	$V_{CC}$ rising, Table 1	$T_A = +25^{\circ}C$	$V_{TH}$ - 1.5%	$V_{TH}$ + 1.5%	V
			$T_A = -40^{\circ}C$ to $+125^{\circ}C$	$V_{TH}$ - 2.5%	$V_{TH}$ + 2.5%	
	$V_{TH-}$	$V_{CC}$ falling		0.98 x $V_{TH+}$		
Reset Timeout Period	$t_{RST}$	Figure 1	86	135	250	$\mu s$
<b>POWER FAIL</b>						
Power-Fail Select Threshold	$V_{SEL}$	PFI input	0.65 x $V_{CC}$		0.85 x $V_{CC}$	V
$V_{CC}$ Monitoring Threshold (Internal Threshold)	$V_{ITH}$	$V_{CC}$ rising	4.06	4.38	4.60	V
Internal Threshold Hysteresis	$V_{IHYST}$	$V_{CC}$ falling	1.0	2	4.0	% $V_{ITH}$
PFI Monitoring Threshold (External Threshold)	$V_{ETH}$	PFI rising	0.9	1.1	1.4	V
External Threshold Hysteresis	$V_{EHYST}$	PFI falling	1.0	3.5	8.0	% $V_{ETH}$

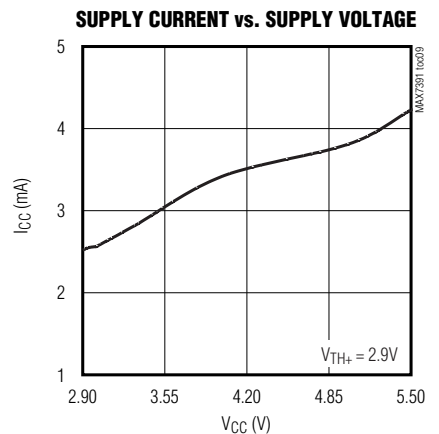
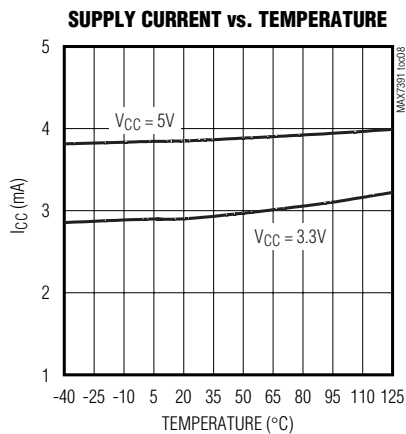
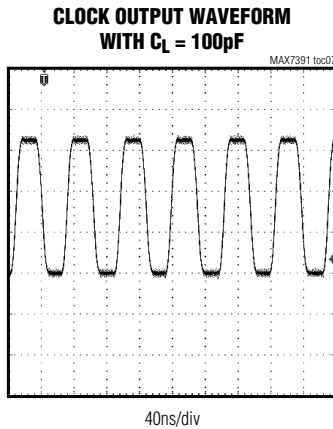
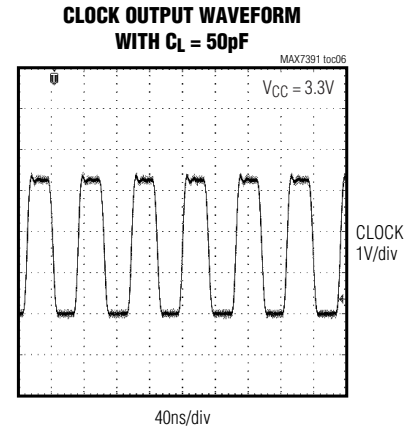
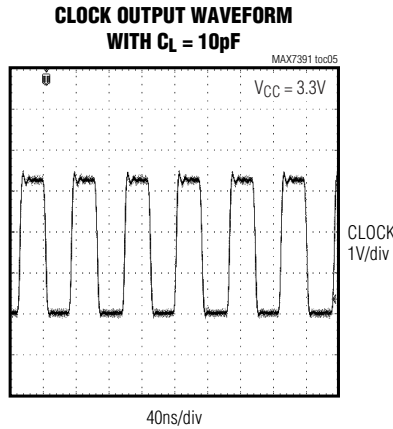
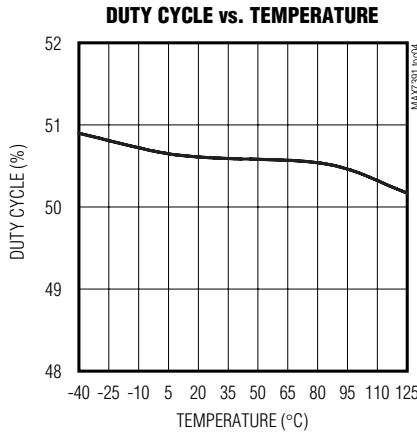
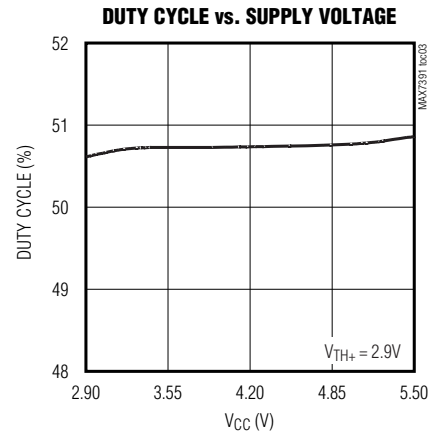
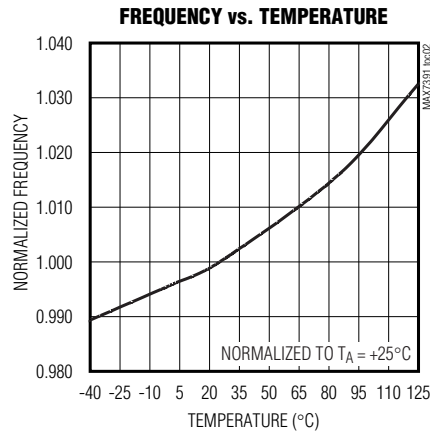
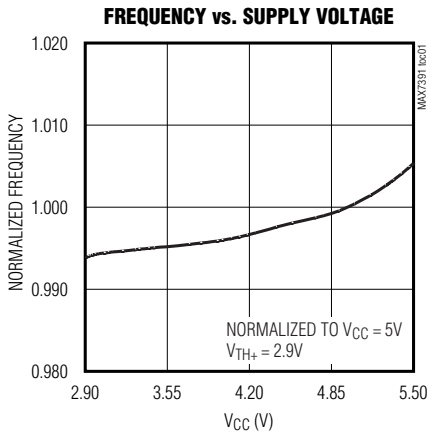
**Note 1:** All parameters are tested at  $T_A = +25^{\circ}C$ . Specifications over temperature are guaranteed by design.

**Note 2:** Guaranteed by design. Not production tested.

# Speed-Switching Clock Generator with Power Fail

## Typical Operating Characteristics

(Typical Application Circuit,  $V_{CC} = +5V$ ,  $f_{CLOCK} = 16MHz$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



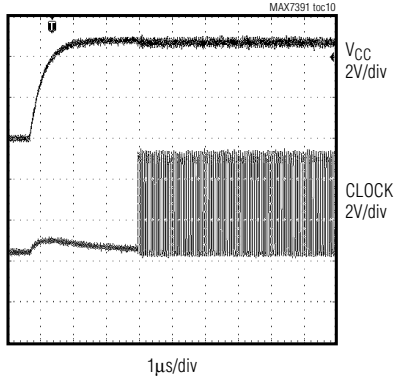
# Speed-Switching Clock Generator with Power Fail

MAX7391

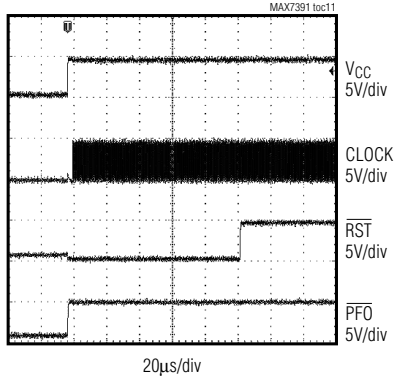
## Typical Operating Characteristics (continued)

(Typical Application Circuit,  $V_{CC} = +5V$ ,  $f_{CLOCK} = 16MHz$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

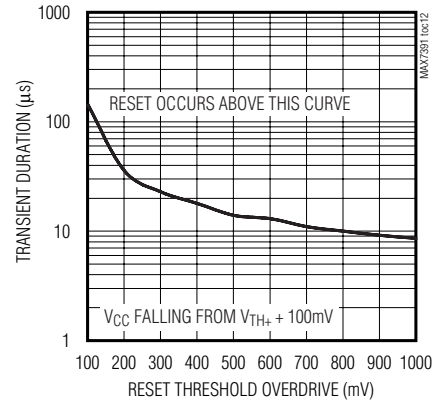
**CLOCK SETTLING TIME FROM START**



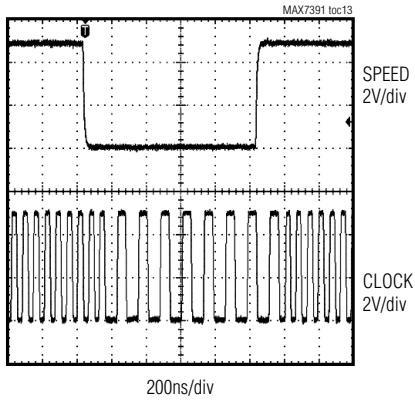
**POWER-ON RESET BEHAVIOR**



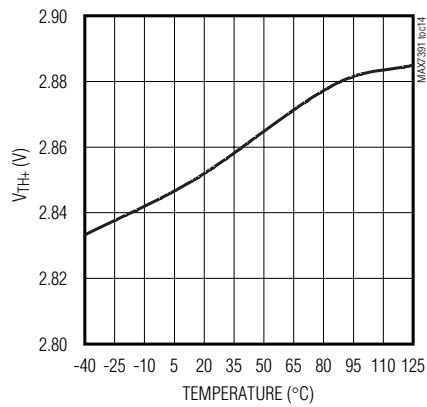
**MAXIMUM  $V_{CC}$  TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE**



**CLOCK RESPONSE TO SPEED SELECT INPUT**



**RISING THRESHOLD vs. TEMPERATURE**



# Speed-Switching Clock Generator with Power Fail

## Pin Description

PIN	NAME	FUNCTION
1	PFI	Power-Fail Input. PFI monitors the condition of either an external supplied voltage or $V_{CC}$ . See the <i>Power Fail</i> section for more details.
2	$V_{CC}$	Power Input. Connect $V_{CC}$ to the power supply. Bypass $V_{CC}$ to GND with a 0.1 $\mu$ F capacitor. Install the bypass capacitor as close to the device as possible.
3	N.C.	No Connection
4	GND	Ground
5	$\overline{PFO}$	Power-Fail Output. Open-drain output asserts when the voltage being monitored drops below the power-fail threshold voltage.
6	SPEED	Clock-Speed Select Input. Connect SPEED high for the factory-trimmed clock output frequency. Connect SPEED low to reduce the clock output frequency by half.
7	RST/ $\overline{RST}$	Reset Output. Reset output is available in one of three configurations: push-pull RST, push-pull $\overline{RST}$ , or open-drain $\overline{RST}$ . The reset output occurs if any combination of the following conditions occurs: reset output is asserted during power-up, and whenever $V_{CC}$ is below the reset threshold level; for devices with WDI, reset output asserts when WDI does not receive a rising or falling edge within the watchdog timeout period.
8	CLOCK	Clock Output

## Detailed Description

The MAX7391 replaces ceramic resonators, crystals, and supervisory functions for microcontrollers in 3.3V and 5V applications.

The MAX7391 provides a clock source, reset, and power-fail functions. The power-fail output provides early warning of power failure. The power-fail threshold is configurable to detect either an external voltage or the  $V_{CC}$  supply voltage to the device.

The clock output can be switched between normal and half-speed operation. This functionality allows the microcontroller to operate at reduced power and may be used to extend the time available to perform house-keeping tasks, such as writing data to flash, during a power failure. Connecting the power-fail output ( $\overline{PFO}$ ) to the SPEED input reduces clock speed automatically during power-fail events.

The integrated reset provides the power-supply monitoring functions necessary to ensure correct microcontroller operation. The reset circuit has built-in power-supply transient immunity and provides both power-on reset and power-fail or brownout reset functionality. Two standard factory-trimmed reset levels are available.

A power-fail function is provided for power-supply voltage monitoring and can provide advance notice of an impending power failure. The power-fail input monitors external power-supply voltages through an external resistive divider. Connect PFI to  $V_{CC}$  to monitor  $V_{CC}$ .

## Clock Output (CLOCK)

The push-pull clock output (CLOCK) drives a ground-connected 1k $\Omega$  load or a positive supply connected 500 $\Omega$  load to within 300mV of either supply rail. CLOCK remains stable over the full operating voltage range and does not generate short output cycles during either power-on or power-off. A typical startup characteristic is shown in the *Typical Operating Characteristics* section.

The clock output frequency is reduced by a factor of two by taking SPEED low. This functionality allows the microcontroller to operate at reduced power and may be used to extend the time available to perform house-keeping tasks, such as writing data to flash during power failure.

## Reset

The reset function drives the microcontroller reset input to prevent operation in the cases of the initial power-on setting, low power-supply voltages, and the failed watchdog operations. Three reset output versions are available: push-pull RST, push-pull  $\overline{RST}$ , and open-drain  $\overline{RST}$ . The reset timeout period ( $t_{RST}$ ) is nominally 135s.

## Power-On Reset (POR)

The internal power-on reset (POR) circuit detects the power-supply voltage ( $V_{CC}$ ) level at startup. The POR circuit starts the oscillator when  $V_{CC}$  exceeds the reset rising threshold level ( $V_{TH+}$ ). The reset output remains asserted from the time  $V_{CC}$  crosses the  $V_{TH+}$  and continues to be asserted for the reset timeout period ( $t_{RST}$ ). Upon completion of the reset timeout, the reset output is released. See Figure 1.

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## Low-Voltage Lockout

The reset output asserts whenever  $V_{CC}$  drops below the reset falling threshold,  $V_{TH-}$ . The difference between the reset rising and falling threshold values is  $V_{TH+} - (V_{TH-})$ . The nominal hysteresis value is 2% of the reset rising threshold value. The reset detection circuitry provides filtering to prevent triggering on negative voltage spikes. See the *Typical Operating Characteristics* for a plot of maximum transient duration without causing a reset pulse vs. reset comparator overdrive.

Figure 1 shows the reset output ( $\overline{RST}/RST$ ) behavior during power-up and brownout.

## Power Fail

The power-fail function provides early warning of a power failure. The power-fail comparator detects the condition of either an external voltage or the  $V_{CC}$  supply voltage.

Internal ( $V_{CC}$ ) detection is configured by connecting PFI to  $V_{CC}$ . The internal  $V_{CC}$  rising threshold ( $V_{ITH}$ ) is set at 4.38V. The open-drain  $\overline{PFO}$  asserts low if the  $V_{CC}$

supply voltage drops below the  $V_{CC}$  falling threshold value ( $V_{IHYST}$ ). The  $V_{CC}$  falling threshold is nominally 2% below the  $V_{CC}$  rising threshold.

External power-fail detection is selected when the applied voltage on PFI ( $V_{PFI}$ ) is less than  $0.65 \times V_{CC}$  ( $V_{SEL}$  minimum). When the voltage on PFI is more than  $0.85 \times V_{CC}$  ( $V_{SEL}$  maximum), the device switches to internal monitoring. External power-fail detection is normally used with a resistive divider from the supply being monitored. See the *Typical Application Circuit*. For a 3.3V supply, the voltage on PFI needs to be set externally and less than  $0.65 \times V_{CC}$  ( $V_{SEL}$  minimum). To set the voltage on PFI externally, choose R1 and R2 so that:

$$V_{PFI} = \frac{R2 \times \text{PowerSupply}}{R2 + R1}$$

See Figure 1 for  $\overline{PFO}$  behavior during power-up and brownout.

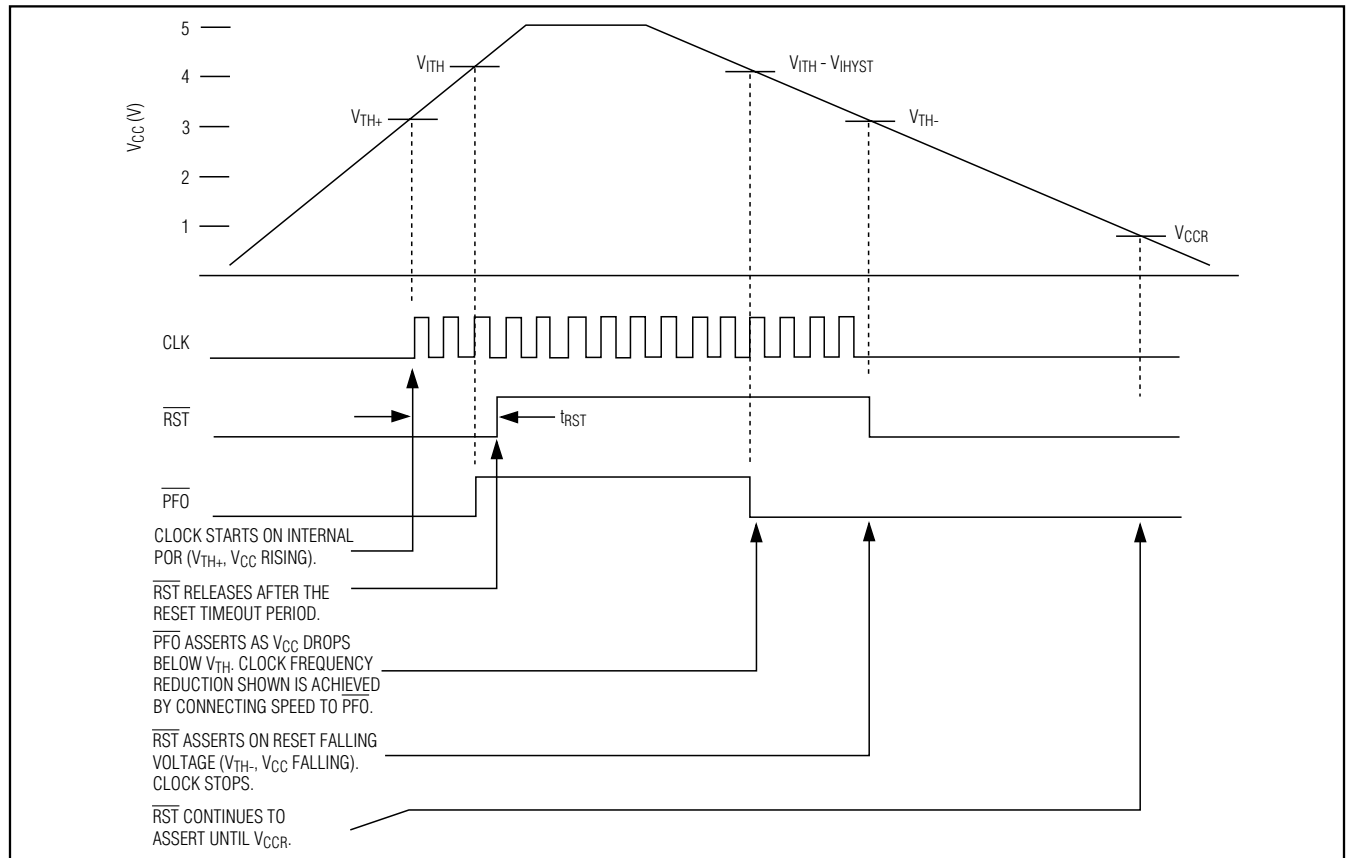


Figure 1.  $\overline{RST}/RST$  and  $\overline{PFO}$  Behavior During Power-Up and Brownout

# Speed-Switching Clock Generator with Power Fail

## Selector Guide

PART	FREQUENCY RANGE (MHz)	RESET FUNCTION	WATCHDOG INPUT (WDI) / WATCHDOG OUTPUT (WDO)	POWER-FAIL INPUT (PFI)/POWER-FAIL OUTPUT (PFO)	SPEED	PIN-PACKAGE
MAX7387	1 to 32	Yes	Yes/yes	Yes/yes	—	10 $\mu$ MAX
MAX7388	1 to 32	Yes	Yes/no	No/yes	—	8 $\mu$ MAX
MAX7389	1 to 32	Yes	Yes/yes	—	—	8 $\mu$ MAX
MAX7390	1 to 32	Yes	Yes/no	—	Yes	8 $\mu$ MAX
MAX7391	1 to 32	Yes	—	Yes/yes	Yes	8 $\mu$ MAX

**Note:** Other versions with different features are available. Refer to the MAX7387/MAX7388 and MAX7389/MAX7390 data sheets.

## Applications Information

### Interfacing to a Microcontroller Clock Input

The clock output is a push-pull, CMOS logic output, which directly drives any microprocessor ( $\mu$ P) or microcontroller ( $\mu$ C) clock input. There are no impedance-matching issues when using the MAX7391. Operate the MAX7391 and  $\mu$ C (or other clock input device) from the same supply voltage level. Refer to the microcontroller data sheet for clock-input compatibility with external clock signals. Table 3 lists clock output frequency.

The MAX7391 requires no biasing components or load capacitance. When using the MAX7391 to retrofit a crystal oscillator, remove all biasing components from the oscillator input.

**Table 1. POR Voltage**

POWER-ON RESET VOLTAGE ( $V_{TH}$ )	r
<b>4.38</b>	<b>M</b>
3.96	J
3.44	N
3.34	P
3.13	Q
<b>2.89</b>	<b>S</b>
2.82	V
2.5	X

**Note:** Standard values are shown in bold. Contact factory for other POR voltages.

**Table 2. Reset Output Type**

OUTPUT TYPE	s
Push-pull RST	A
Push-pull $\overline{\text{RST}}$	B
<b>Open collector <math>\overline{\text{RST}}</math></b>	<b>C</b>

**Note:** Standard values are shown in bold. Contact factory for other output types.

### Power-Supply Considerations

The MAX7391 operates with power-supply voltages in the 2.7V to 5.5V range. Good power-supply decoupling is needed to maintain the power-supply rejection performance of the MAX7391. Bypass  $V_{CC}$  to GND with a 0.1 $\mu$ F surface-mount ceramic capacitor. Mount the bypass capacitor as close to the device as possible. If possible, mount the MAX7391 close to the microcontroller's decoupling capacitor so that additional decoupling is not required.

A larger-value bypass capacitor is recommended if the MAX7391 is to operate with a large capacitive load. Use a bypass capacitor value of at least 1000 times that of the output load capacitance.

### Output Jitter

The MAX7391's jitter performance is given in the *Electrical Characteristics* table as a peak-to-peak value obtained by observing the output of the device for 20s with a 500MHz oscilloscope. Jitter measurements are approximately proportional to the period of the output frequency of the device. Thus, a 4MHz part has approximately twice the jitter value of an 8MHz part.

The jitter performance of all clock sources degrades in the presence of mechanical and electrical interference. The MAX7391 is immune to vibration, shock, and EMI influences, and thus provides a considerably more robust clock source than crystal- or ceramic-resonator-based oscillator circuits.

**Table 3. Clock Output Frequency**

CLOCK FREQUENCY ( $f_{CLOCK}$ ) (MHz)	ff
4	RD
8	TP
12	VB
16	WB

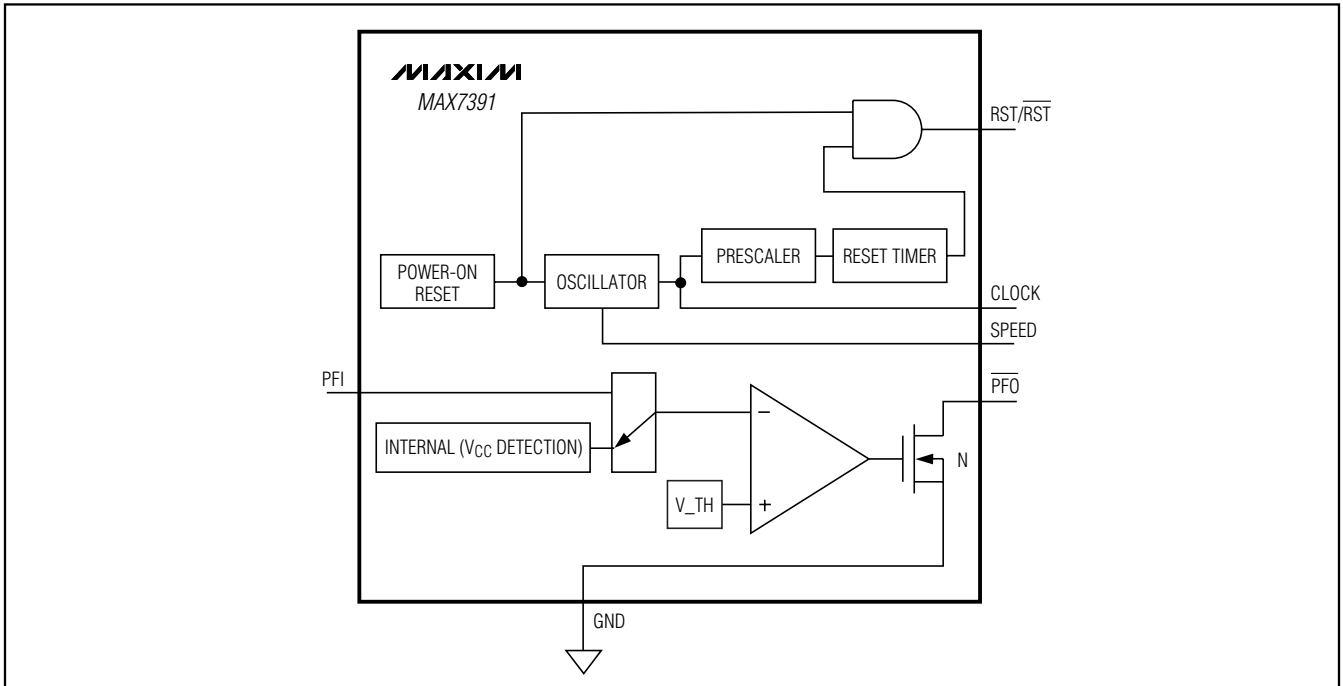
**Note:** Contact factory for other frequencies.



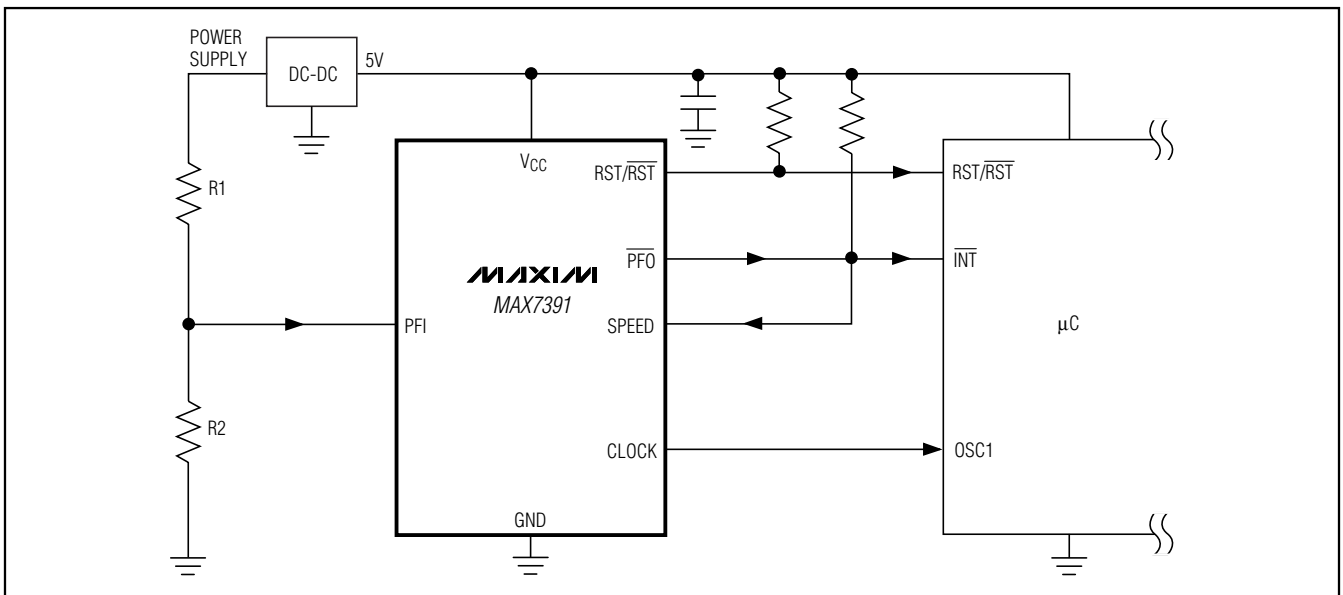
# Speed-Switching Clock Generator with Power Fail

## Functional Diagram

MAX7391



## Typical Application Circuit



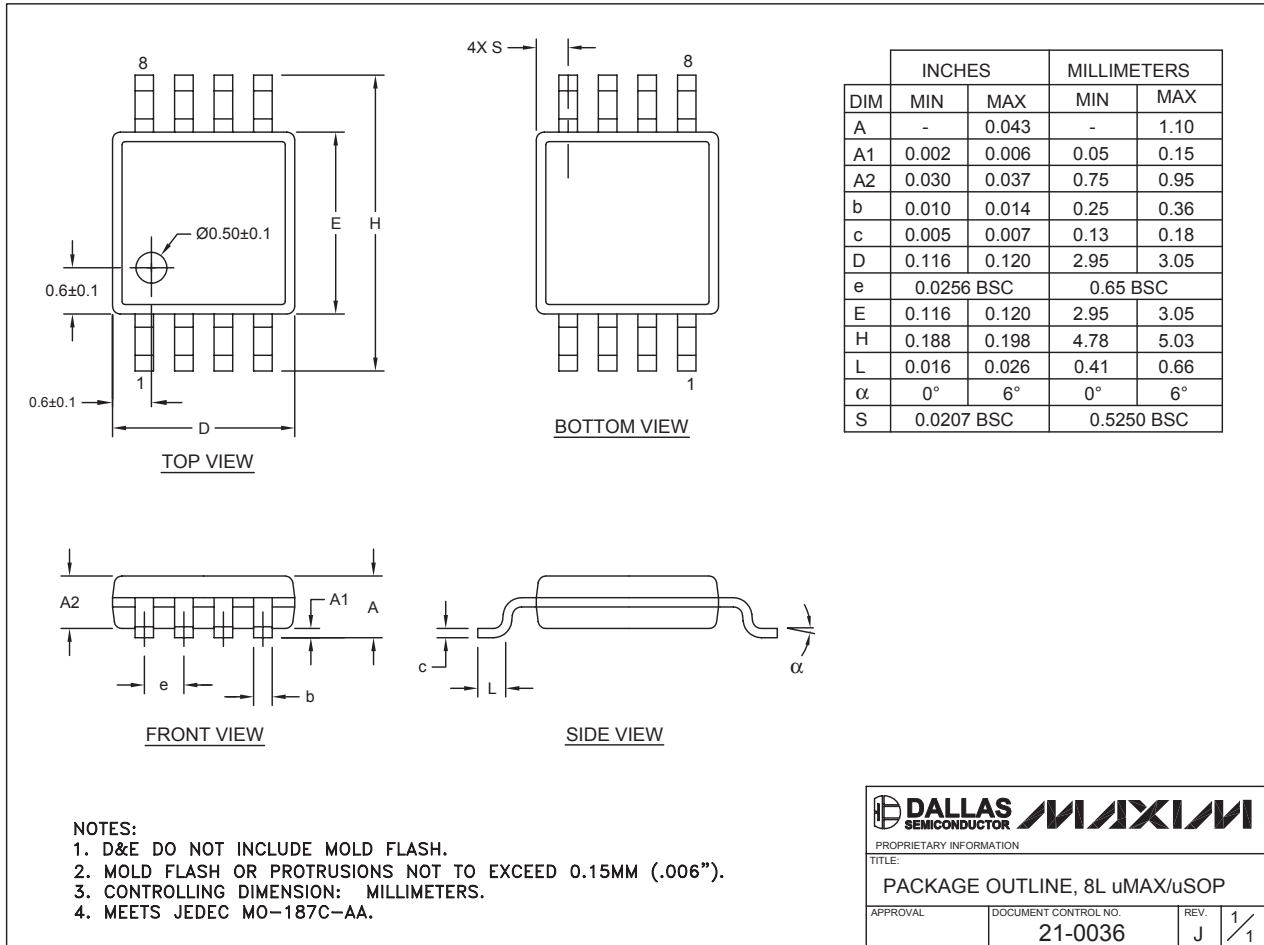
## Chip Information

PROCESS: BICMOS

# Speed-Switching Clock Generator with Power Fail

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



8LUMAXDEPS

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