MIC22705

1MHz, 7A Integrated Switch High-Efficiency Synchronous Buck Regulator

General Description

The Micrel MIC22705 is a high-efficiency, 7A integrated switch synchronous buck (step-down) regulator. The MIC22705 is optimized for highest efficiency, achieving more than 95% efficiency while still switching at 1MHz. The ultra-high speed control loop keeps the output voltage within regulation even under the extreme transient load swings commonly found in FPGAs and low-voltage ASICs. The output voltage is pre-bias safe and can be adjusted down to 0.7V to address all low-voltage power needs.

The MIC22705 offers a full range of sequencing and tracking options. The Enable/Delay (EN/DLY) pin, combined with the Power Good (PG) pin, allows multiple outputs to be sequenced in any way during turn-on and turn-off. The Ramp Control™ (RC) pin allows the device to be connected to another product in the MIC22xxx and/or MIC68xxx family, to keep the output voltages within a certain ΔV on start-up.

The MIC22705 is available in a 24-pin 4mm x 4mm MLF® with a junction operating range from –40°C to +125°C.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

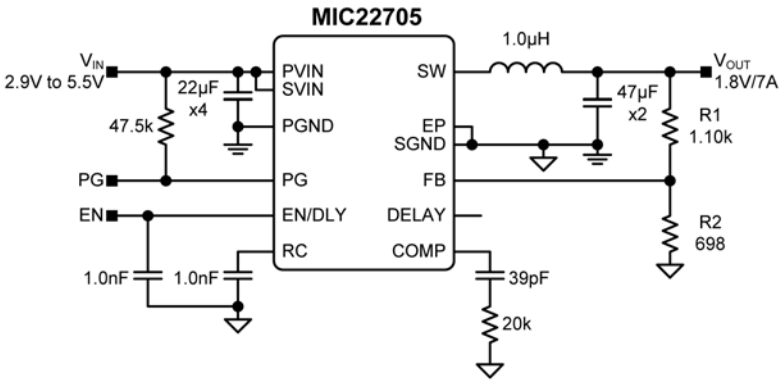
Features

- Input voltage range: 2.9V to 5.5V
- Output voltage adjustable down to 0.7V
- Output load current up to 7A
- Safe start-up into a pre-biased load
- Full sequencing and tracking capability
- Power Good output
- Efficiency > 95% across a broad load range
- Ultra-fast transient response
- Easy RC compensation
- 100% maximum duty cycle
- Fully-integrated MOSFET switches
- Thermal-shutdown and current-limit protection
- 24-pin 4mm x 4mm MLF®
- –40°C to +125°C junction temperature range

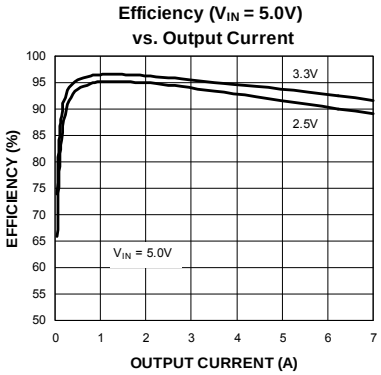
Applications

- High power density point-of-load conversion
- Servers, routers, and base stations
- DVD recorders / Blu-ray players
- Computing peripherals
- FPGAs, DSP and low voltage ASIC power

Typical Application



MIC22705 7A 1MHz Synchronous Output Converter



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MLF and *Micro*LeadFrame are registered trademarks of Amkor Technology, Inc.

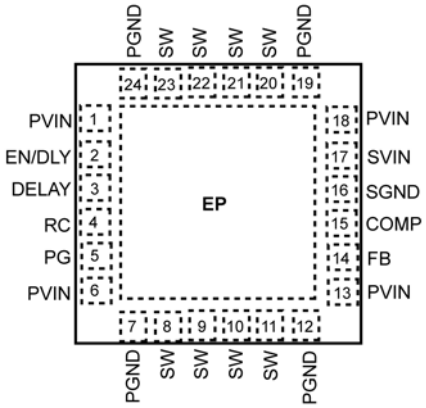
Ordering Information

Part Number	Voltage	Junction Temperature Range	Package	Lead Finish
MIC22705YML	Adjustable	–40°C to +125°C	24-Pin 4x4 MLF®	Pb-Free

Note:

1. Other Voltage available. Contact Micrel for details.

Pin Configuration



24-Pin 4mm × 4mm MLF® (ML)

Pin Description

Pin Number	Pin Name	Description
1, 6, 13, 18	PVIN	Power Supply Voltage (Input): The PVIN pins are the input supply to the internal P-Channel Power MOSFET. A 22µF ceramic is recommended for bypassing at each PVIN pin. The SVIN pin must be connected to a PVIN pin.
2	EN/DLY	Enable/Delay (Input): This pin is internally fed with a 1µA current source from SVIN. A delayed turn on is implemented by adding a capacitor to this pin. The delay is proportional to the capacitor value. The internal circuits are held off until EN/DLY reaches the enable threshold of 1.24V. This pin is pulled low when the input voltage is lower than the UVLO threshold.
3	DELAY	Delay (Input): Capacitor to ground sets internal delay timer. Timer delays Power Good (PG) output at turn-on and ramp down at turn-off.
4	RC	Ramp Control: A capacitor from the RC pin-to-ground determines slew rate of output voltage during start-up. The RC pin is internally fed with a 1µA current source. The output voltage tracks the RC pin voltage. The slew rate is proportional by the internal 1µA source and RC pin capacitor. This feature can be used for tracking capability as well as soft start.
5	PG	PG (Output): This is an open drain output that indicates when the output voltage is below 90% of its nominal voltage. The PG flag is asserted without delay when the enable is set low or when the output goes below the 90% threshold.
14	FB	Feedback: Input to the error amplifier. The FB pin is regulated to 0.7V. A resistor divider connecting the feedback to the output is used to adjust the desired output voltage.

Pin Description (Continued)

Pin Number	Pin Name	Description
15	COMP	Compensation Pin (Input): The MIC22705 uses an internal compensation network containing a fixed-frequency zero (phase lead response) and pole (phase lag response) which allows the external compensation network to be much simplified for stability. The addition of a single capacitor and resistor to the COMP pin will add the necessary pole and zero for voltage mode loop stability using low-value, low-ESR ceramic capacitors.
16	SGND	Signal Ground: Internal signal ground for all low power circuits.
17	SVIN	Signal Power Supply Voltage (Input): This pin is connected externally to the PVIN pin. A 2.2µF ceramic capacitor from the SVIN pin to SGND must be placed next to the IC.
7, 12, 19, 24	PGND	Power Ground: Internal ground connection to the source of the internal N-Channel MOSFETs.
8, 9, 10, 11, 20, 21, 22, 23	SW	Switch (Output): This is the connection to the drain of the internal P-Channel MOSFET and drain of the N-Channel MOSFET. This is a high-frequency, high-power connection; therefore traces should be kept as short and as wide as practical.
EP	GND	Exposed Pad (Power): Must be connected to the GND plane for full output power to be realized.

Absolute Maximum Ratings[1, 2]

PV_{IN} to PGND ..... –0.3V to 6V
SV_{IN} to PGND .....–0.3V to PV_{IN}
V_{SW} to PGND .....–0.3V to PV_{IN}
V_{DELAY} to PGND .....–0.3V to PV_{IN}
$V_{EN/DLY}$ to PGND ..... -0.3V to PV_{IN}
V_{PG} to PGND .....–0.3V to PV_{IN}
Junction Temperature ..... 150°C
PGND to SGND ..... –0.3V to 0.3V
Storage Temperature Range .....–65°C to +150°C
Lead Temperature (soldering, 10s)..... 260°C

Operating Ratings[3]

Supply Voltage (PV_{IN}/SV_{IN}) ..... 2.9V to 5.5V
Power Good Voltage (V_{PG}).....0V to PV_{IN}
Enable Input ($V_{EN/DLY}$).....0V to PV_{IN}
Junction Temperature (T_J) .....–40°C ≤ T_J ≤ +125°C
Package Thermal Resistance
4mm x 4mm MLF®-24 (θ_{JC}).....14°C/W
4mm x 4mm MLF®-24 (θ_{JA}).....40°C/W

Electrical Characteristics[4]

SV_{IN} = PV_{IN} = $V_{EN/DLY}$ = 3.3V, V_{OUT} = 1.8V, T_A = 25°C, unless noted. Bold values indicate –40°C< T_J < +125°C.

Parameter	Condition	Min.	Typ.	Max.	Units
Power Input Supply					
Input Voltage Range (PV_{IN})		**2.9**		**5.5**	V
Undervoltage Lockout Trip Level	PV_{IN} Rising	**2.55**	2.75	**2.9**	V
UVLO Hysteresis			420		mV
Quiescent Supply Current	V_{FB} = 0.9V (not switching)		0.85	**1.3**	mA
Shutdown Current	$V_{EN/DLY}$ = 0V		5	**10**	µA
Reference					
Feedback Reference Voltage		**0.686**	0.7	**0.714**	V
Load Regulation	I_{OUT} = 100mA to 7A		0.2		%
Line Regulation	V_{IN} = 2.9V to 5.5V; I_{OUT} = 100mA		0.2		%
FB Bias Current	V_{FB} = 0.5V		10		nA
Enable Control					
EN/DLY Threshold Voltage		**1.14**	1.24	**1.34**	V
EN Hysteresis			10		mV
EN/DLY Bias Current	$V_{EN/DLY}$ = 0.5V; V_{IN} = 2.9V and V_{IN} = 5.5V	**0.7**	1.0	**1.3**	µA
RC Ramp Control					
RC Pin Source Current	V_{RC} = 0.35V	**0.7**	1.0	**1.3**	µA
Oscillator					
Switching Frequency		0.8	1.0	1.2	MHz
Maximum Duty Cycle	V_{FB} ≤ 0.5V	100			%
Short Current Protection					
Current Limit	V_{FB} = 0.5V	**7**	11	**21**	A

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. Devices are ESD sensitive. Handling precautions recommended.
3. The device is not guaranteed to function outside its operating rating.
4. Specification for packaged product only.

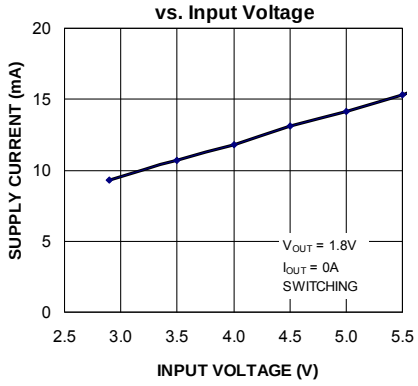
Electrical Characteristics[4] (Continued)

V_{IN} = PV_{IN} = $V_{EN/DLY}$ = 3.3V, V_{OUT} = 1.8V, T_A = 25°C, unless noted. Bold values indicate –40°C< T_J < +125°C.

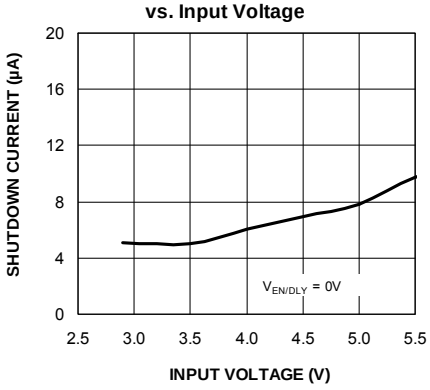
Parameter	Condition	Min.	Typ.	Max.	Units
Internal FETs					
Top-MOSFET $R_{DS(ON)}$	V_{FB} = 0.5V, I_{SW} = 1A		30		mΩ
Bottom-MOSFET $R_{DS(ON)}$	V_{FB} = 0.9V, I_{SW} = -1A		25		mΩ
SW Leakage Current	PV_{IN} = 5.5V, V_{SW} = 5.5V, V_{EN} = 0V			**60**	µA
V_{IN} Leakage Current	PV_{IN} = 5.5V, V_{SW} = 0V, V_{EN} = 0V			**25**	
Power Good (PG)					
PG Threshold	Threshold % of V_{FB} from V_{REF}	–7.5	–10	–12.5	%
Hysteresis			2.0		%
PG Output Low Voltage	I_{PG} = 5mA (sinking), $V_{EN/DLY}$ = 0V		144		mV
PG Leakage Current	V_{PG} = 5.5V; V_{FB} = 0.9V		1.0	**2.0**	µA
PG DELAY Pin Source Current	V_{PG} = 0V; V_{FB} = 0.9V	**0.7**	1.0	**1.3**	µA
Thermal Protection					
Over-temperature Shutdown	T_J Rising		160		°C
Over-temperature Shutdown Hysteresis			20		°C

Typical Characteristics

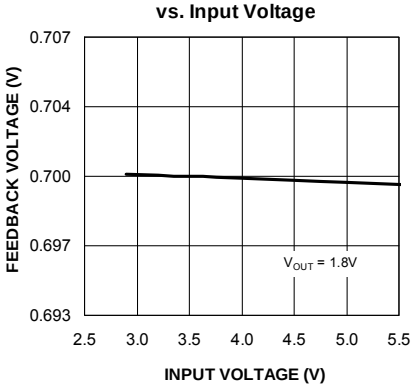
V_{IN} Operating Supply Current vs. Input Voltage



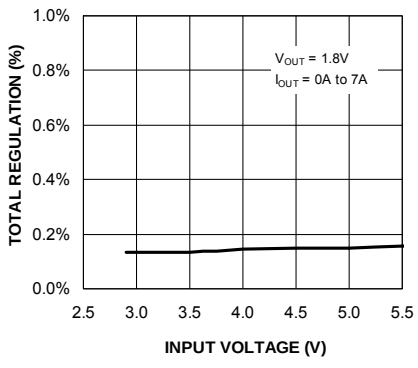
V_{IN} Shutdown Current vs. Input Voltage



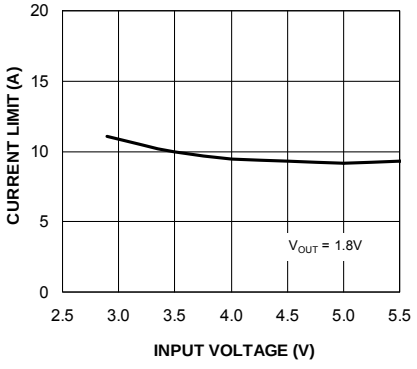
Feedback Voltage vs. Input Voltage



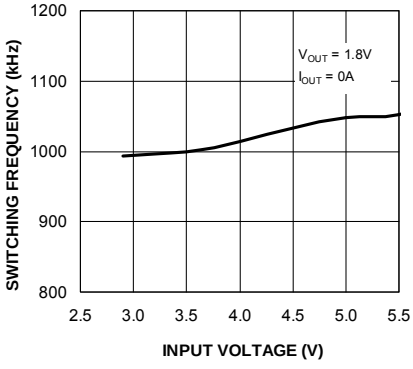
Load Regulation vs. Input Voltage



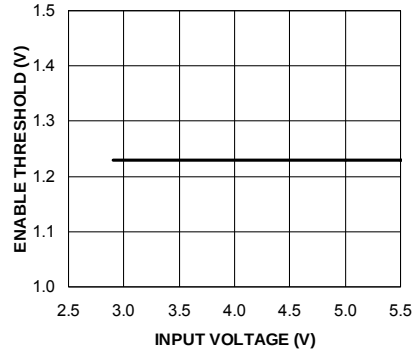
Current Limit vs. Input Voltage



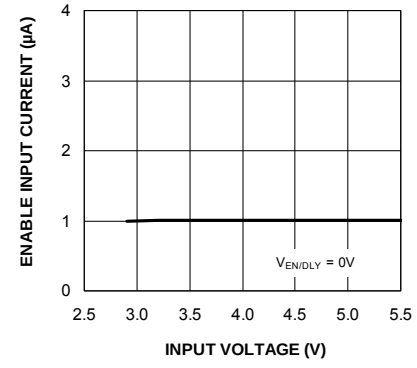
Switching Frequency vs. Input Voltage



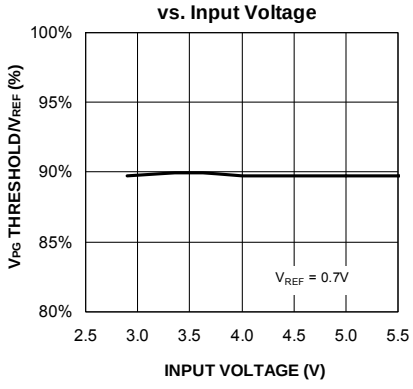
Enable Threshold vs. Input Voltage



Enable Input Current vs. Input Voltage

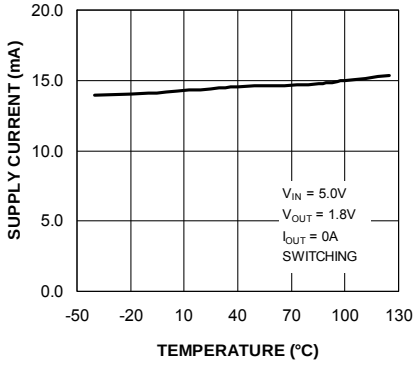


Power Good Threshold/V_{REF} Ratio vs. Input Voltage

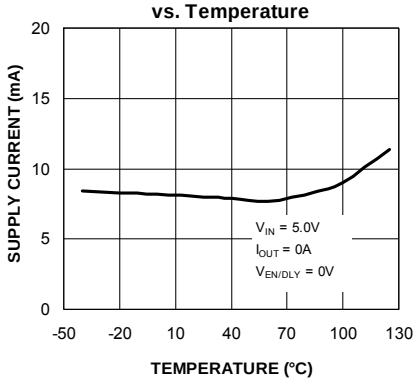


Typical Characteristics (Continued)

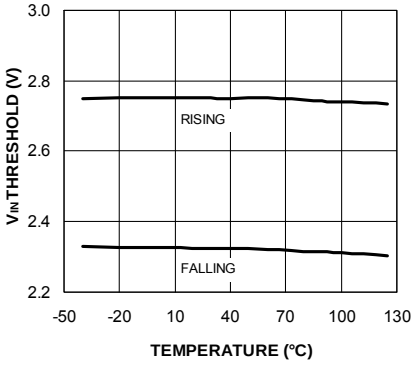
V_{IN} Operating Supply Current vs. Temperature



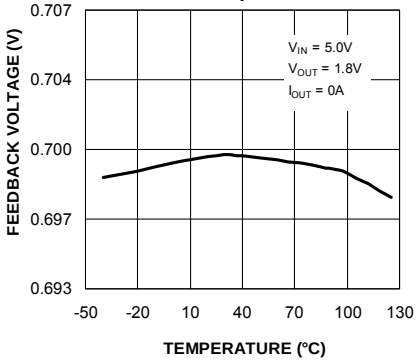
V_{IN} Shutdown Current vs. Temperature



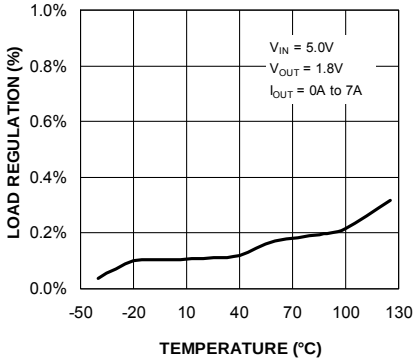
V_{IN} UVLO Threshold vs. Temperature



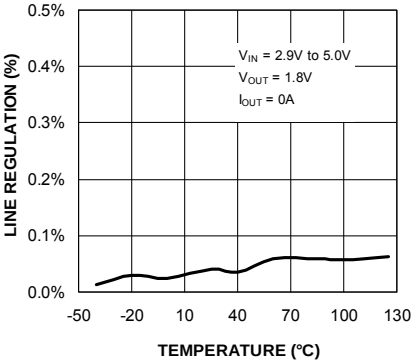
Feedback Voltage vs. Temperature



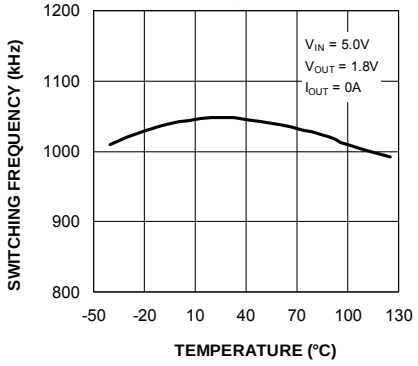
Load Regulation vs. Temperature



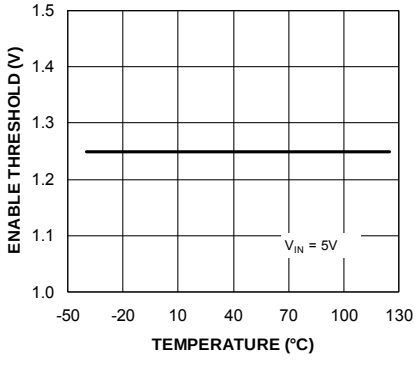
Line Regulation vs. Temperature



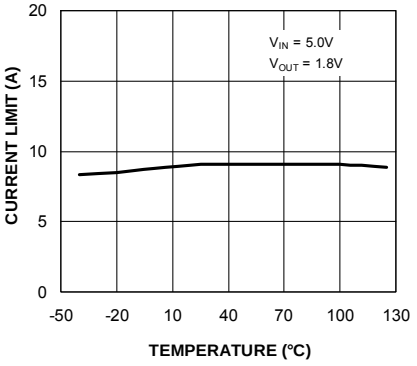
Switching Frequency vs. Temperature



Enable Threshold vs. Temperature

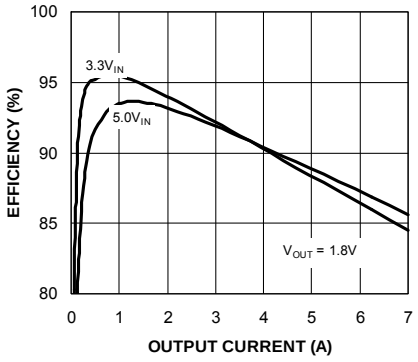


Current Limit vs. Temperature

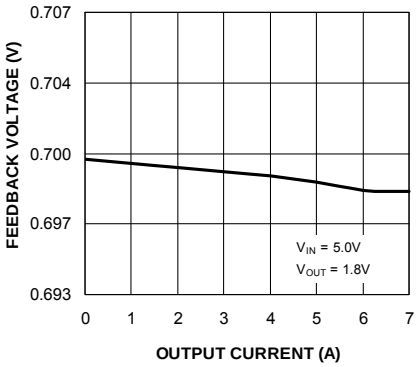


Typical Characteristics (Continued)

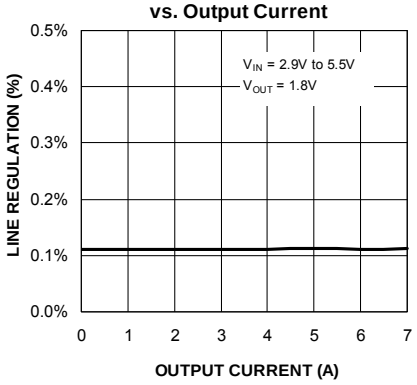
Efficiency vs. Output Current



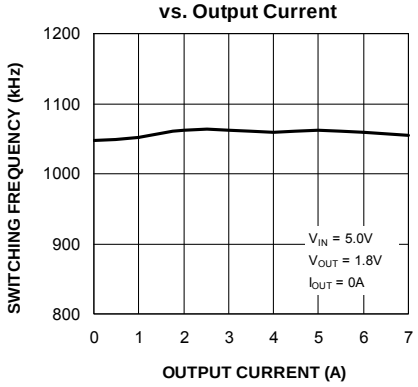
Feedback Voltage vs. Output Current



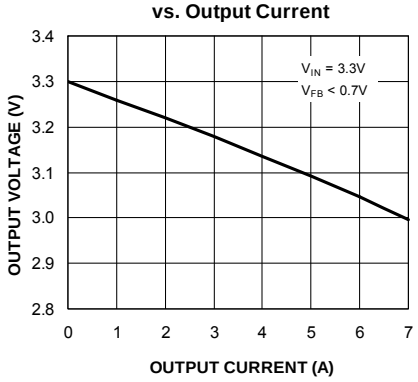
Line Regulation vs. Output Current



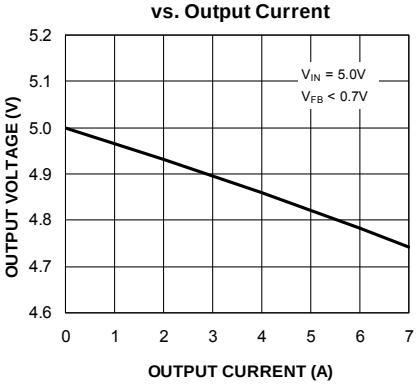
Switching Frequency vs. Output Current



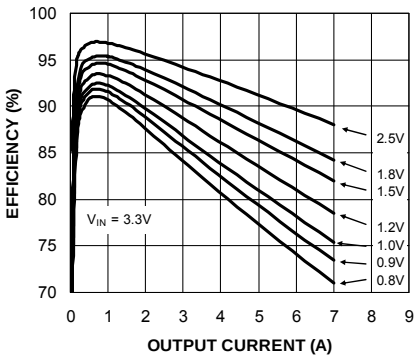
Output Voltage (V_{IN} = 3.3V) vs. Output Current



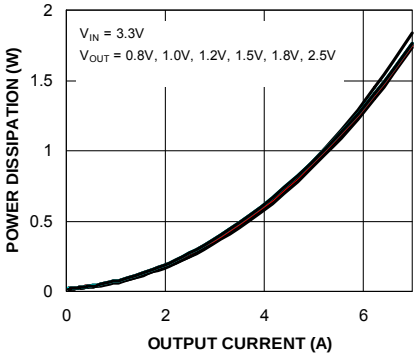
Output Voltage (V_{IN} = 5.0V) vs. Output Current



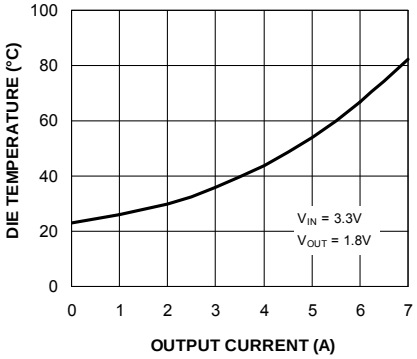
Efficiency (V_{IN} = 3.3V) vs. Output Current



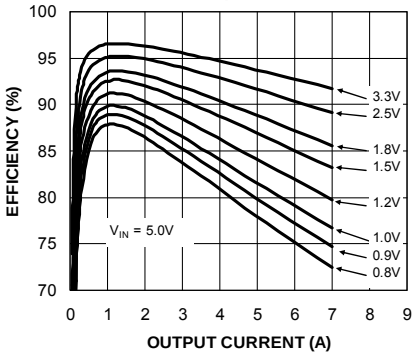
IC Power Dissipation vs. Output Current (V_{IN} = 3.3V)

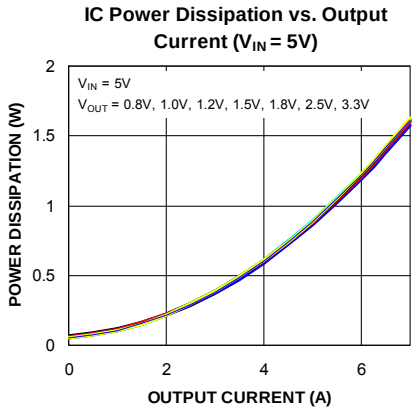


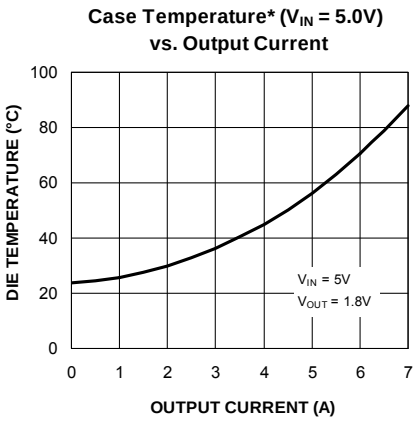
Case Temperature* (V_{IN} = 3.3V) vs. Output Current



Typical Characteristics (Continued)



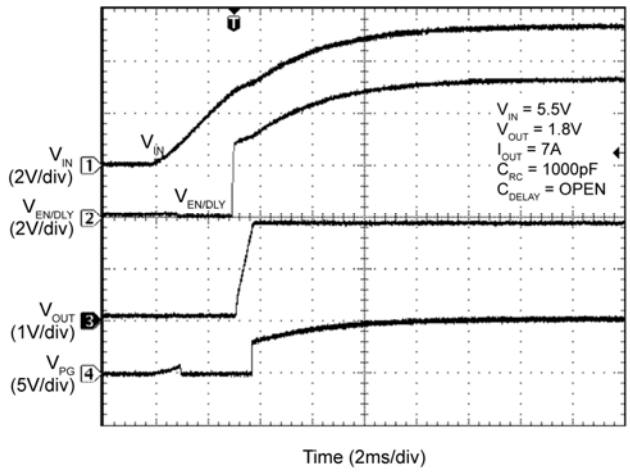




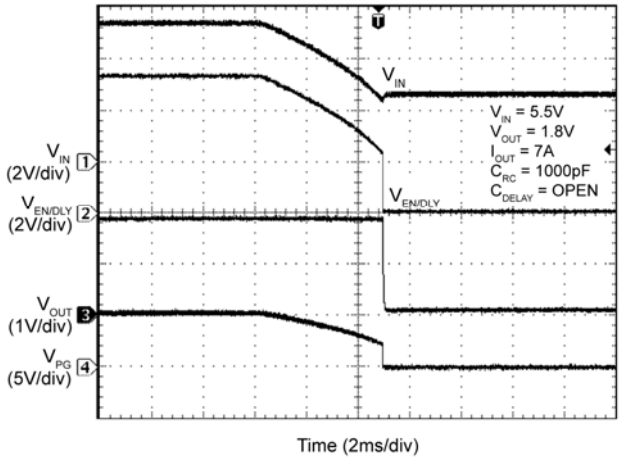
Die Temperature* : The temperature measurement was taken at the hottest point on the MIC22705 case and mounted on a five-square inch PCB (see *Thermal Measurement*s section). Actual results will depend upon the size of the PCB, ambient temperature, and proximity to other heat-emitting components.

Functional Characteristics

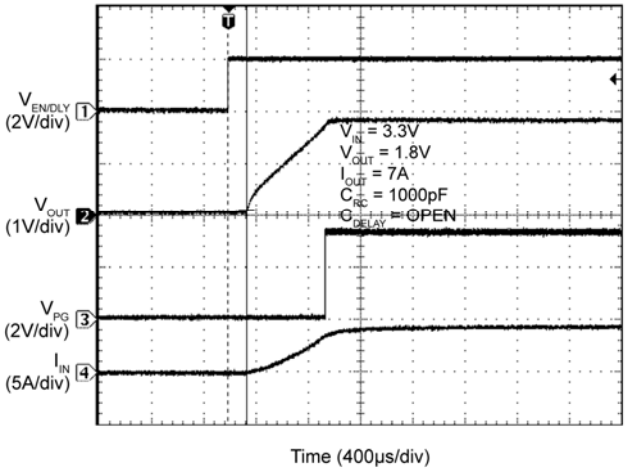
V_{IN} Turn-On



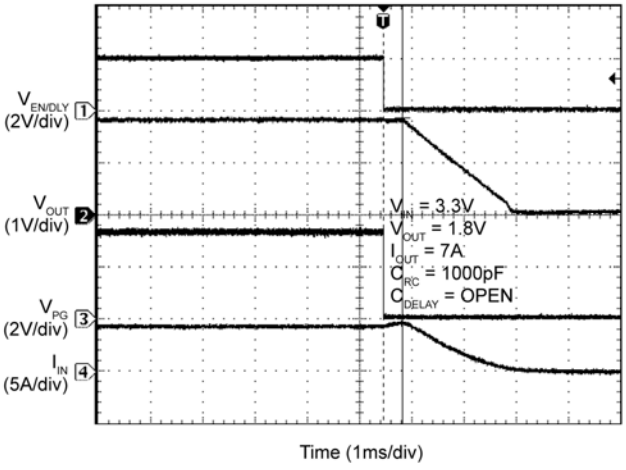
V_{IN} Turn-Off



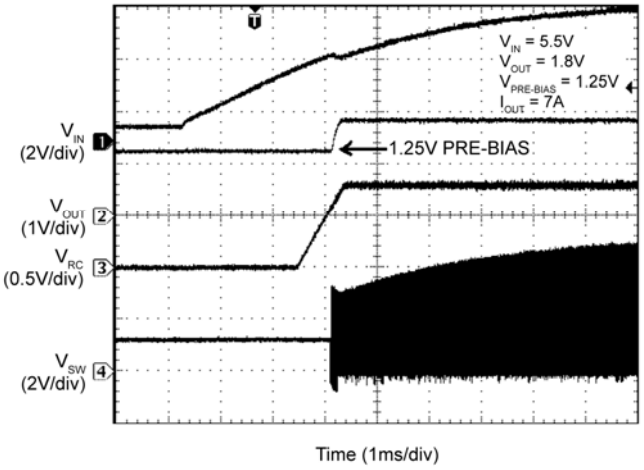
Enable Turn-On Delay/Rise Time



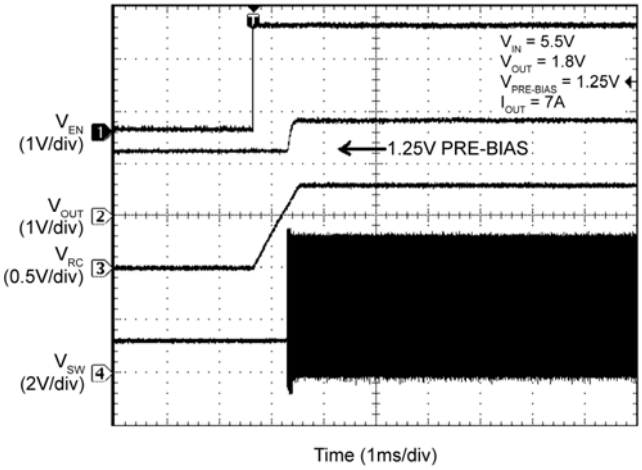
Enable Turn-Off



V_{IN} Start-Up with Pre-Biased Output

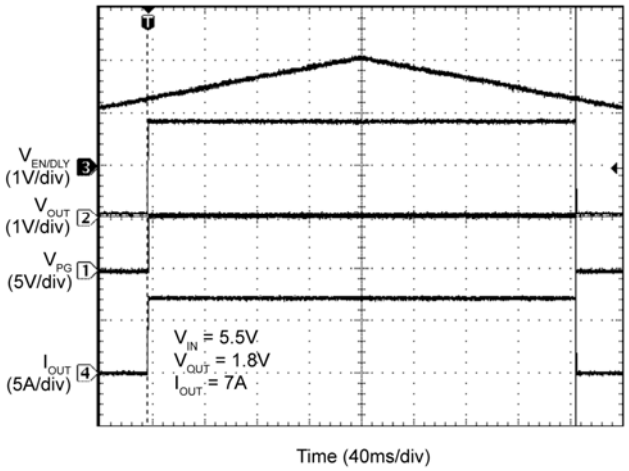


Enable Start-Up with Pre-Biased Output

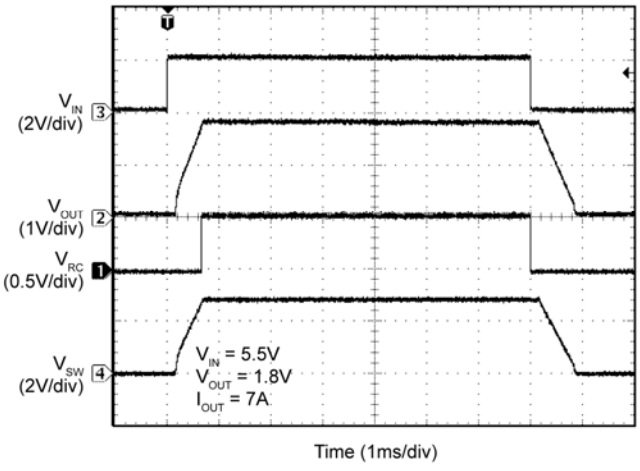


Functional Characteristics (Continued)

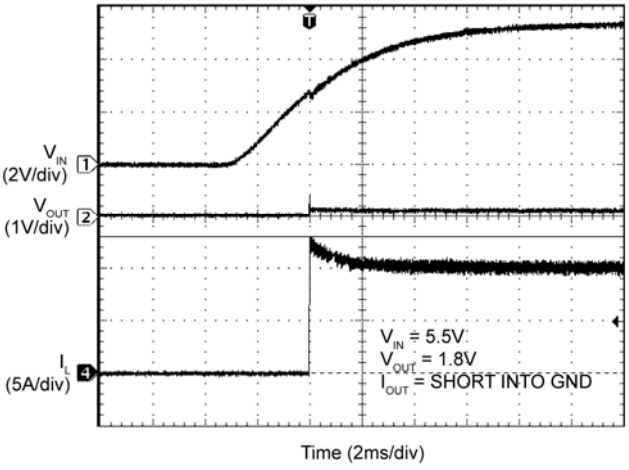
Enable Threshold



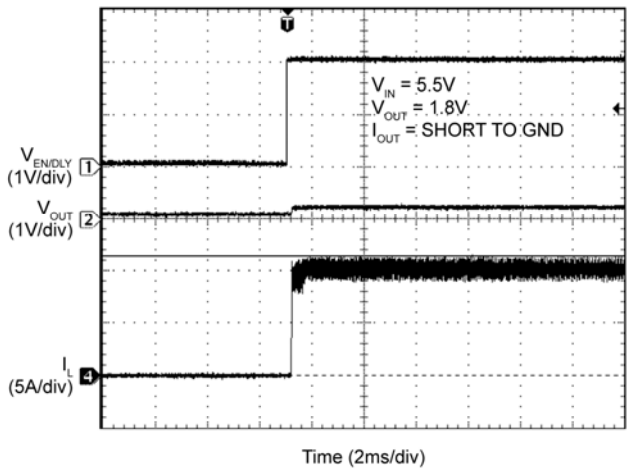
Enable Turn-On/Off



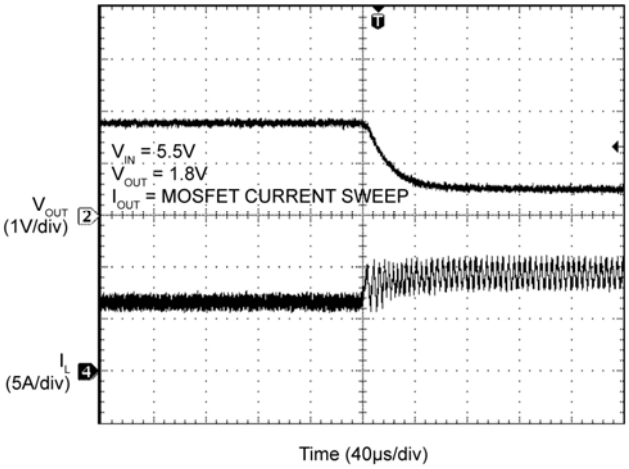
Power-Up Into Short Circuit



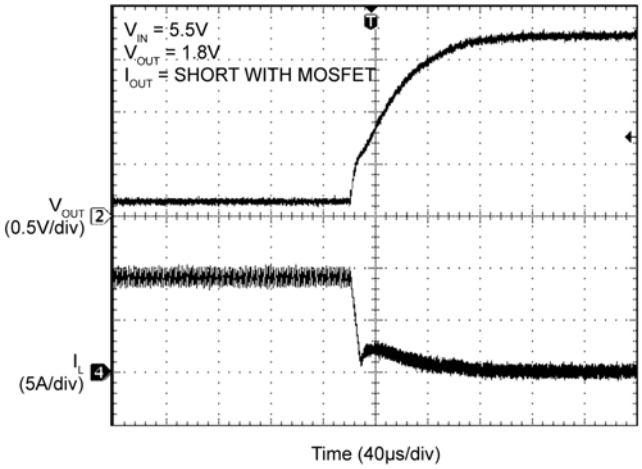
Enabled Into Short Circuit



Output Current-Limit Threshold

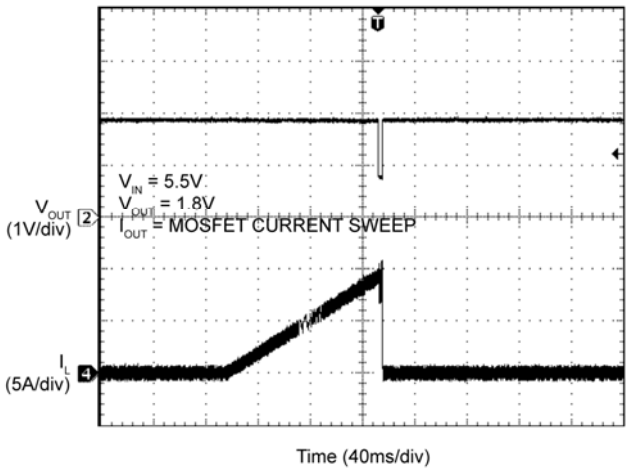


Output Recovery from Short Circuit

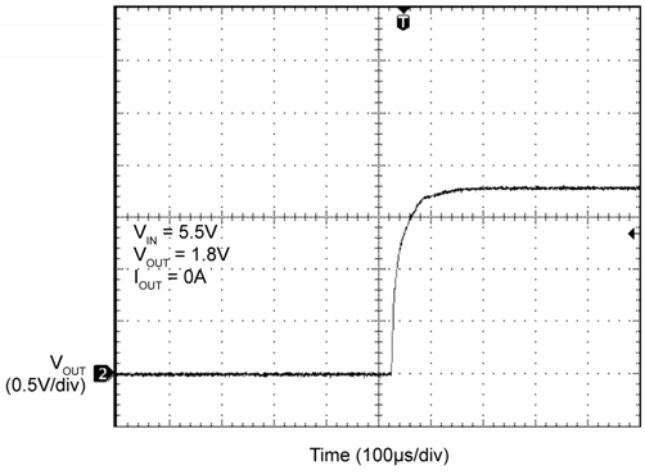


Functional Characteristics (Continued)

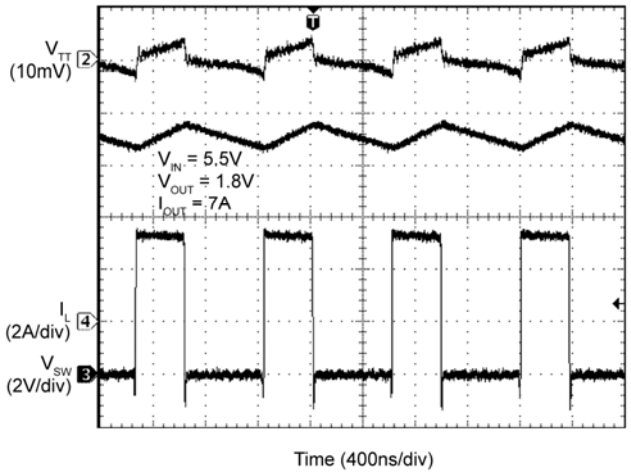
Peak Current-Limit Threshold



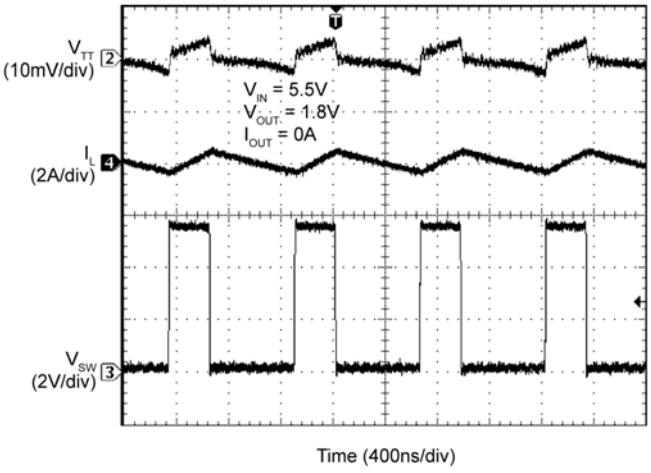
Thermal Shutdown Recovery



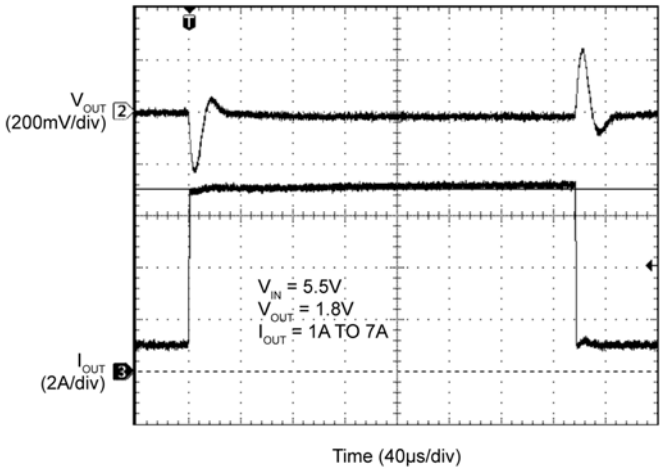
Switching Waveforms
I_{OUT} = 7A



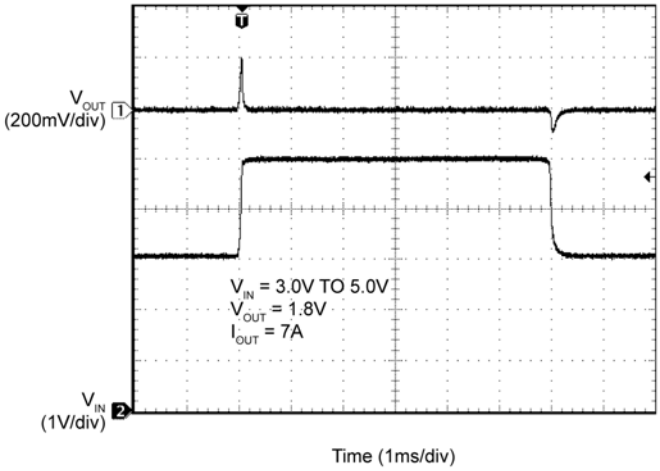
Switching Waveforms
I_{OUT} = 0A



Load Transient Response



Line Transient Response



Functional Diagram

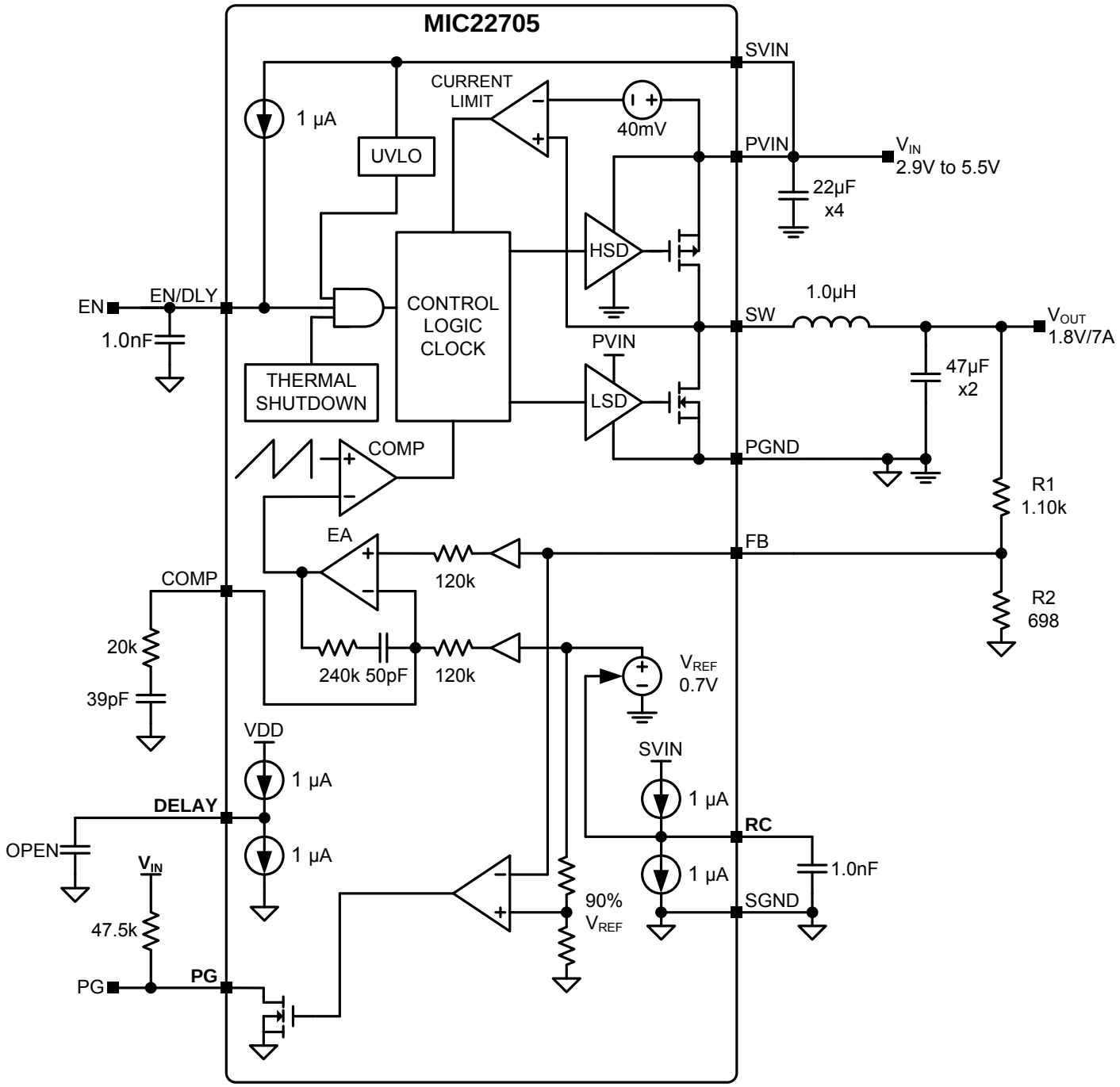


Figure 1. MIC22705 Functional Diagram

Application Information

The MIC22705 is a 7A Synchronous step down regulator IC with a fixed 1MHz, voltage mode PWM control scheme. The other features include tracking and sequencing control for controlling multiple output power systems, power on reset.

The MIC22705 is a voltage mode, Pulse-Width Modulation (PWM) controller. By controlling the ratio of the on-to-off time, or duty cycle, a regulated DC output voltage is achieved. As load or supply voltage changes, so does the duty cycle to maintain a constant output voltage. In cases where the input supply runs into a dropout condition, the MIC22705 will run at 100% duty cycle.

The MIC22705 provides constant switching at 1MHz with synchronous internal MOSFETs. The internal MOSFETs include a high-side P-Channel MOSFET from the input supply to the switch pin and an N-Channel MOSFET from the switch pin-to-ground. Since the low-side N-Channel MOSFET provides the current during the off cycle, very-low amount of power is dissipated during the off period.

The PWM control provides fixed-frequency operation. By maintaining a constant switching frequency, predictable fundamental and harmonic frequencies are achieved. Other methods of regulation, such as burst and skip modes, have frequency spectrums that change with load that can interfere with sensitive communication equipment.

Component Selection

Input Capacitor

A 22µF X5R or X7R dielectrics ceramic capacitor is recommended on each of the PVIN pins for bypassing. A Y5V dielectrics capacitor should not be used. Aside from losing most of their capacitance over temperature, they also become resistive at high frequencies. This reduces their ability to filter out high-frequency noise.

Output Capacitor

The MIC22705 was designed specifically for the use of ceramic output capacitors. The 100µF output capacitor can be increased to improve transient performance. Since the MIC22705 is in voltage mode, the control loop relies on the inductor and output capacitor for compensation. For this reason, do not use excessively large output capacitors. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from the undesirable effect of their wide variation in capacitance over temperature, become resistive at high frequencies. Using Y5V or Z5U capacitors can cause instability in the MIC22705.

Inductor Selection

Inductor selection will be determined by the following (not necessarily in the order of importance):

- Inductance
- Rated current value
- Size requirements
- DC resistance (DCR)

The MIC22705 is designed for use with a 0.47µH to 4.7µH inductor.

Maximum current ratings of the inductor are generally given in two methods: permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% loss in inductance. Ensure the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin that the peak current will not saturate the inductor. The ripple current can add as much as 1.2A to the output current level. The RMS rating should be chosen to be equal or greater than the current limit of the MIC22705 to prevent overheating in a fault condition. For best electrical performance, the inductor should be placed very close to the SW nodes of the IC. For this reason, the heat of the inductor is somewhat coupled to the IC, so it offers some level of protection if the inductor gets too hot. It is important to test all operating limits before settling on the final inductor choice.

The size requirements refer to the area and height requirements that are necessary to fit a particular design. Please refer to the inductor dimensions on their datasheet.

DC resistance is also important. While DCR is inversely proportional to size, DCR can represent a significant efficiency loss. Refer to the “Efficiency Considerations” sub-section for a more detailed description.

Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power consumed.

$$\text{Efficiency } \% = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \right) \times 100$$

Maintaining high efficiency serves two purposes. First, it decreases power dissipation in the power supply, reducing the need for heat sinks and thermal design considerations and it decreases consumption of current for battery powered applications. Reduced current draw from a battery increases the devices operating time, critical in hand held devices.

There are mainly two loss terms in switching converters: static losses and switching losses. Static losses are simply the power losses due to VI or I^2R. For example, power is dissipated in the high side switch during the on cycle. Power loss is equal to the high-side MOSFET $RDS_{(ON)}$ multiplied by the RMS switch current squared (I_{SW}^2). During the off-cycle, the low-side N-Channel MOSFET conducts, also dissipating power. Similarly, the inductor's DCR and capacitor's ESR also contribute to the I^2R losses. Device operating current also reduces efficiency by the product of the quiescent (operating) current and the supply voltage. The current required to drive the gates on and off at a constant 1MHz frequency and the switching transitions make up the switching losses.

Figure 2 illustrates an efficiency curve. The portion, from 0A to 0.4A, efficiency losses are dominated by quiescent current losses, gate drive, transition and core losses. In this case, lower supply voltages yield greater efficiency in that they require less current to drive the MOSFETs and have reduced input power consumption.

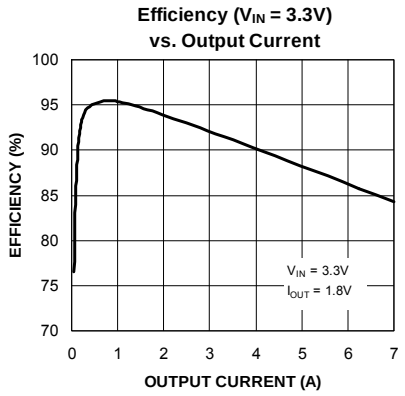


Figure 2. Efficiency Curve

The region, 1A to 7A, efficiency loss is dominated by MOSFET $RDS_{(ON)}$ and inductor DC losses. Higher input supply voltages will increase the gate-to-source voltage on the internal MOSFETs, thereby reducing the internal $RDS_{(ON)}$. This improves efficiency by decreasing DC losses in the device. All but the inductor losses are inherent to the device. In which case, inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated as follows:

$$L_{PD} = I_{OUT}^2 \times DCR$$

From that, the loss in efficiency due to inductor resistance can be calculated as follows:

$$\text{Efficiency Loss} = \left[1 - \left(\frac{V_{OUT} \times I_{OUT}}{(V_{OUT} \times I_{OUT}) + L_{PD}}\right)\right] \times 100$$

Efficiency loss due to DCR is minimal at light loads and gains significance as the load is increased. Inductor selection becomes a trade-off between efficiency and size in this case.

Alternatively, under lighter loads, the ripple current due to the inductance becomes a significant factor. When light load efficiencies become more critical, a larger inductor value maybe desired. Larger inductances reduce the peak-to-peak inductor ripple current, which minimize losses.

Compensation

The MIC22705 has a combination of internal and external stability compensation to simplify the circuit for small, high-efficiency designs. In such designs, voltage mode conversion is often the optimum solution. Voltage mode is achieved by creating an internal 1MHz ramp signal and using the output of the error amplifier to modulate the pulse width of the switch node, thereby maintaining output voltage regulation. With a typical gain bandwidth of 100kHz – 200kHz, the MIC22705 is capable of extremely fast transient responses.

The MIC22705 is designed to be stable with a typical application using a 1µH inductor and a 100µF ceramic (X5R) output capacitor. These values can be varied dependent upon the tradeoff between size, cost and efficiency, keeping the LC natural frequency $\left(\frac{1}{2 \times \pi \times \sqrt{L \times C}}\right)$ ideally less than 26 kHz to ensure stability can be achieved. The minimum recommended inductor value is 0.47µH and minimum recommended output capacitor value is 22µF. The tradeoff between changing these values is that with a larger inductor, there is a reduced peak-to-peak current which yields a greater efficiency at lighter loads. A larger output capacitor will improve transient response by providing a larger hold up reservoir of energy to the output.

The integration of one pole-zero pair within the control loop greatly simplifies compensation. The optimum values for C_{COMP} (in series with a 20k resistor) are shown below.

C→ / L↓	22µF – 47µF	47µF – 100µF	100µF – 470µF
0.47µH	0* – 10pF	22pF	33pF
1µH	0† – 15pF	15 – 22pF	33pF
2.2µH	15 – 33pF	33 – 47pF	100 – 220pF
* VOUT > 1.2V, † VOUT > 1V			

Feedback

The MIC22705 provides a feedback pin to adjust the output voltage to the desired level. This pin connects internally to an error amplifier. The error amplifier then compares the voltage at the feedback to the internal 0.7V reference voltage and adjusts the output voltage to maintain regulation. The resistor divider network for a desired V_{OUT} is given by:

$$R2 = \frac{R1}{\left(\frac{V_{OUT}}{V_{REF}} - 1\right)}$$

where V_{REF} is 0.7V and V_{OUT} is the desired output voltage. A 10kΩ or lower resistor value from the output to the feedback (R1) is recommended since large feedback resistor values increase the impedance at the feedback pin, making the feedback node more susceptible to noise pick-up. A small capacitor (50pF – 100pF) across the lower resistor can reduce noise pick-up by providing a low impedance path to ground.

Enable/Delay (EN/DLY) Pin

Enable/Delay (EN/DLY) sources 1µA out of the IC to allow a startup delay to be implemented. The delay time is simply the time it takes 1µA to charge $C_{EN/DLY}$ to 1.25V. Therefore:

$$t_{EN/DLY} = \frac{1.24 \times C_{EN/DLY}}{1 \times 10^{-6}}$$

Delay Pin (DELAY)

The delay (DELAY) pin also has a 1µA trimmed current source and a 1µA current sink which acts with an external capacitor to delay the operation of the Power Good (PG) output. This can be used also in sequencing outputs in a sequenced system, but with the addition of a conditional delay between supplies; allowing a first up, last down power sequence.

After enable (EN/DLY) is driven high, V_{OUT} will start to rise (rate determined by RC capacitor). As the FB voltage goes above 90% of its nominal set voltage, DELAY begins to rise as the 1µA source charges the external capacitor. When the threshold of 1.24V is crossed, PG is asserted high and DLY continues to charge to a voltage V_{DD}. When FB falls below 90% of nominal, POR is asserted low immediately. However, if EN/DLY is driven low, PG will fall immediately to the low state and DELAY will begin to fall as the external capacitor is discharged by the 1µA current sink. When the threshold of $V_{DD} - 1.24V$ is crossed, V_{OUT} will begin to fall at a rate determined by the RC capacitor. As the voltage change in both cases is 1.24V, both rising and falling delays are matched at $t_{PG} = \frac{1.24 \times C_{DELAY}}{1 \times 10^{-6}}$.

RC Pin (Soft-Start)

The RC pin provides a trimmed 1µA current source/sink for accurate ramp up (soft-start). This allows the MIC22705 to be used in systems requiring voltage tracking or ratio-metric voltage tracking at startup.

There are two ways of using the RC pin:

1. Externally driven from a voltage source
2. Externally attached capacitor sets output ramp up/down rate

In the first case, driving RC with a voltage from 0V to V_{REF} will program the output voltage between 0 and 100% of the nominal set voltage.

In the second case, the external capacitor sets the ramp up and ramp down time of the output voltage. The time is given by $t_{RAMP} = \frac{0.7 \times C_{RC}}{1 \times 10^{-6}}$ where t_{RAMP} is the time from 0 to 100% nominal output voltage.

Current Limit

The MIC22705 is protected against overload in two stages. The first is to limit the current in the P-channel switch; the second is over temperature shutdown.

Current is limited by measuring the current through the high-side MOSFET during its power stroke and immediately switching off the driver when the preset limit is exceeded.

The circuit in Figure 4 describes the operation of the current limit circuit. Since the actual RDS_{ON} of the P-Channel MOSFET varies part-to-part, over temperature and with input voltage, simple IR voltage detection is not employed. Instead, a smaller copy of the Power MOSFET (Reference FET) is fed with a constant current which is a directly proportional to the factory set current limit. This sets the current limit as a current ratio and thus, is not dependant upon the RDS_{ON} value. Current limit is set to nominal value. Variations in the scale factor K between the Power PFET and the reference PFET used to generate the limit threshold account for a relatively small inaccuracy.

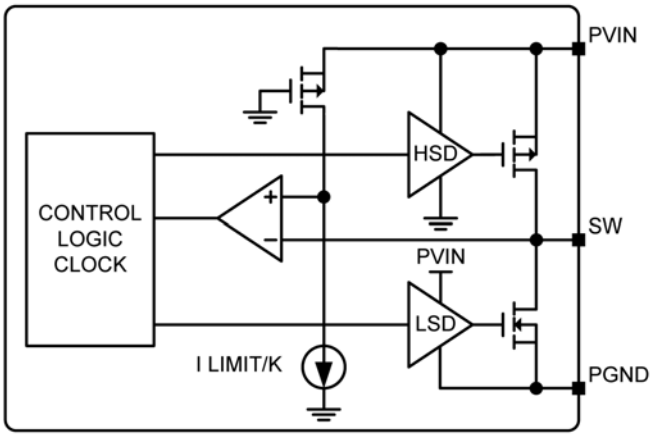


Figure 4. Current-Limit Detail

Thermal Considerations

The MIC22705 is packaged in a MLF® 4mm x 4mm – a package that has excellent thermal-performance equaling that of the larger TSSOP packages. This maximizes heat transfer from the junction to the exposed pad (ePAD) which connects to the ground plane. The size of the ground plane attached to the exposed pad determines the overall thermal resistance from the junction to the ambient air surrounding the printed circuit board. The junction temperature for a given ambient temperature can be calculated using:

$$T_J = T_{AMB} + P_{DISS} \times R\theta_{JA}$$

where:

- P_{DISS} is the power dissipated within the MLF® package and is at 7A load. $R\theta_{JA}$ is a combination of junction-to-case thermal resistance ($R\theta_{JC}$) and Case-to-Ambient thermal resistance ($R\theta_{CA}$), since thermal resistance of the solder connection from the ePAD to the PCB is negligible; $R\theta_{CA}$ is the thermal resistance of the ground plane-to-ambient, so $R\theta_{JA} = R\theta_{JC} + R\theta_{CA}$.
- T_{AMB} is the operating ambient temperature.

Example:

The evaluation board has two copper planes contributing to an $R\theta_{JA}$ of approximately 25°C/W. The worst case $R\theta_{JC}$ of the MLF® 4x4 is 14°C/W.

$$R\theta_{JA} = R\theta_{JC} + R\theta_{CA}$$
$$R\theta_{JA} = 14 + 25 = 39°C/W$$

To calculate the junction temperature for a 50°C ambient:

$$T_J = T_{AMB} + P_{DISS} \times R\theta_{JA}$$
$$T_J + 50 + (1.8 \times 39)$$
$$T_J = 120°C$$

Thermal Measurements

Measuring the IC's case temperature is recommended to ensure it is within its operating limits. Although this might seem like a very elementary task, it is easy to get erroneous results. The most common mistake is to use the standard thermal couple that comes with a thermal meter. This thermal couple wire gauge is large, typically 22 gauge, and behaves like a heatsink, resulting in a lower case measurement.

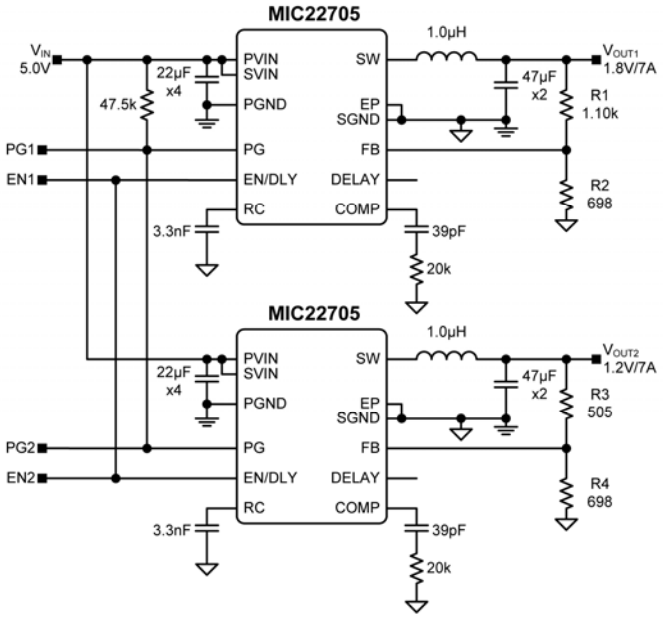
Two methods of temperature measurement are using a smaller thermal couple wire or an infrared thermometer. If a thermal couple wire is used, it must be constructed of 36 gauge wire or higher then (smaller wire size) to minimize the wire heat-sinking effect. In addition, the thermal couple tip must be covered in either thermal grease or thermal glue to make sure that the thermal couple junction is making good contact with the case of the IC. Omega brand thermal couple (5SC-TT-K-36-36) is adequate for most applications.

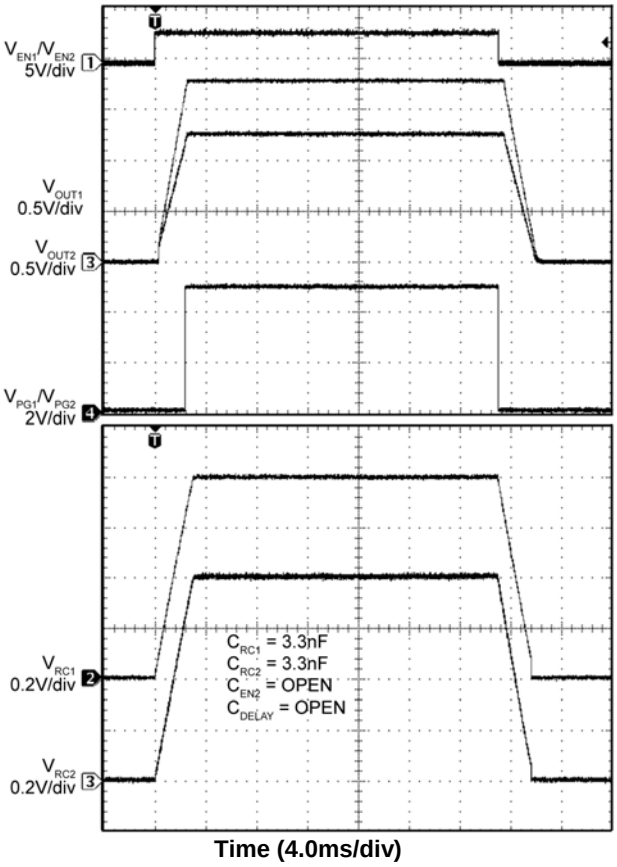
Wherever possible, an infrared thermometer is recommended. The measurement spot size of most infrared thermometers is too large for an accurate reading on a small form factor ICs. However, a IR thermometer from Optris has a 1mm spot size, which makes it a good choice for measuring the hottest point on the case. An optional stand makes it easy to hold the beam on the IC for long periods of time.

Sequencing and Tracking

There are four variations which are easily implemented using the MIC22705. The two sequencing variations are Delayed and Windowed. The two tracking variants are Normal and Ratio Metric. The following diagrams illustrate methods for connecting two MIC22705's to achieve these requirements.

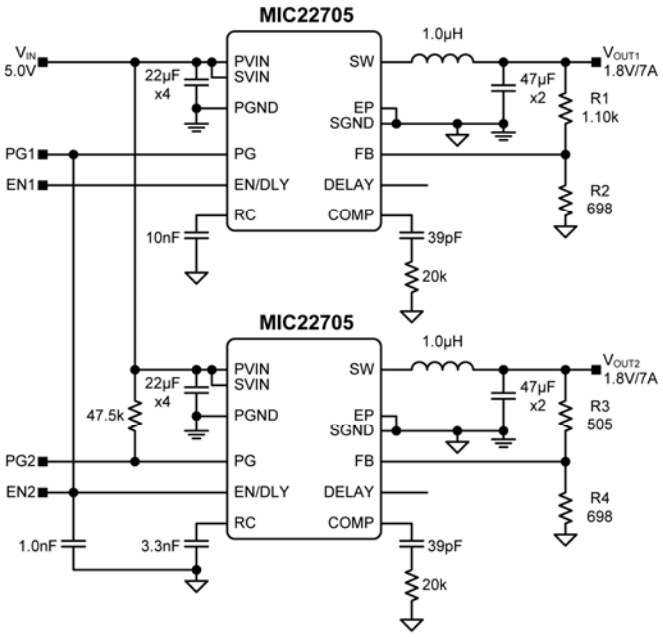
Window Sequencing:

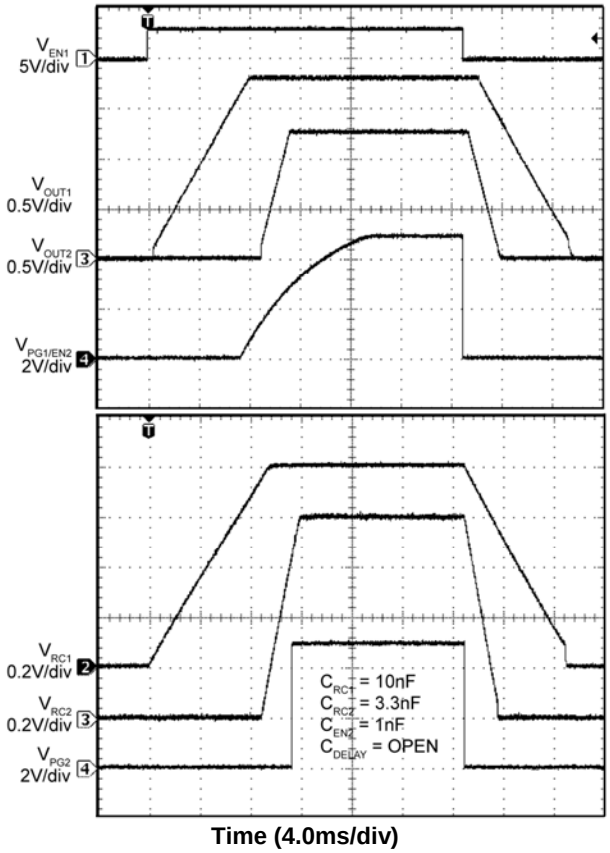




Time (4.0ms/div)

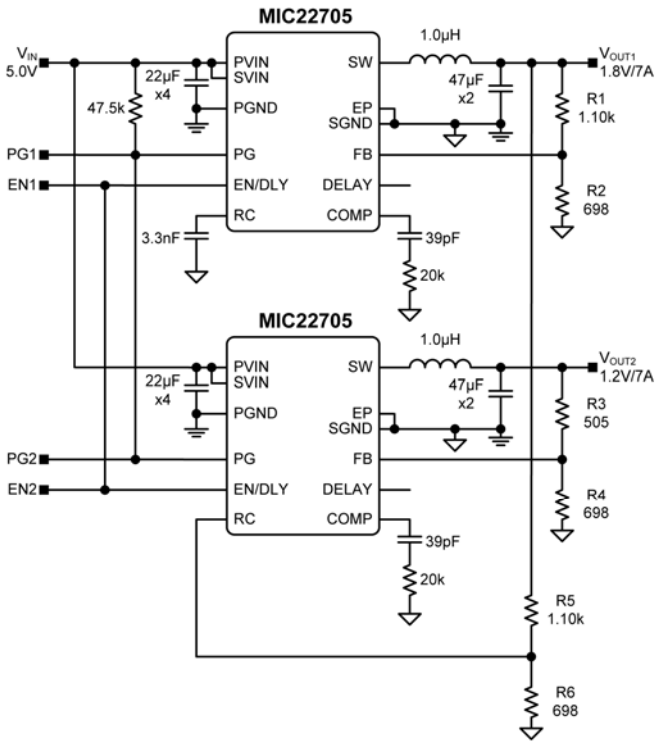
Delayed Sequencing:

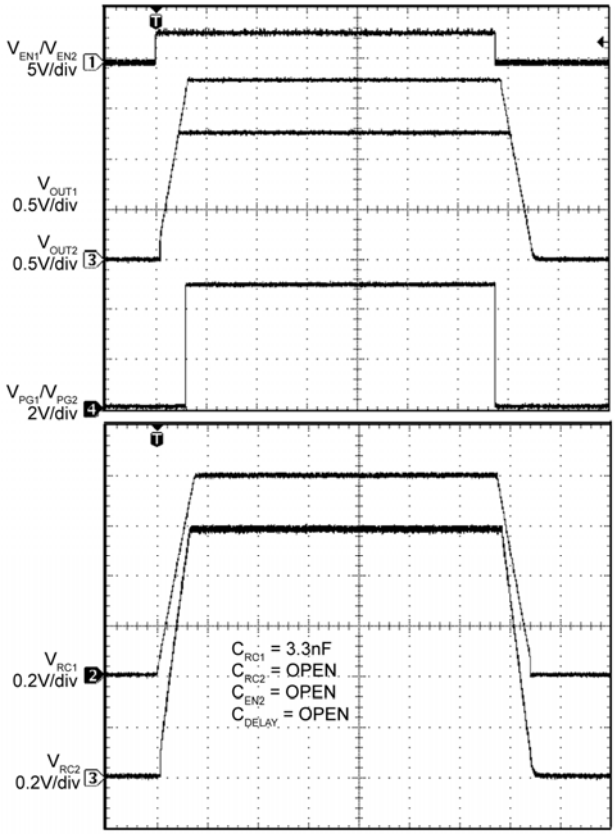




Time (4.0ms/div)

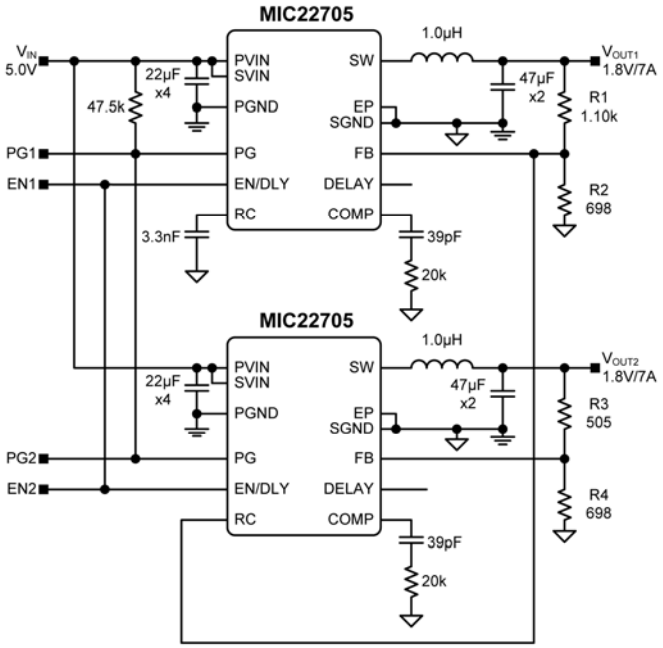
Normal Tracking:

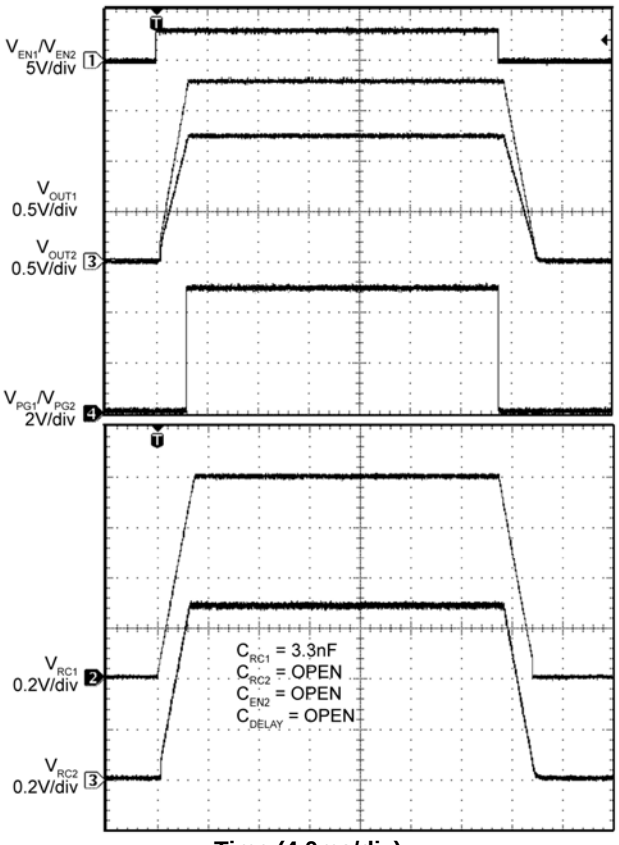




Time (4.0ms/div)

Ratio Metric Tracking:





Time (4.0ms/div)

PCB Layout Guidelines

Warning!!! To minimize EMI and output noise, follow these layout recommendations.

PCB Layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

The following guidelines should be followed to insure proper operation of the MIC22705 converter:

IC

- The 2.2µF ceramic capacitor, which is connected to the SVIN pin, must be located right at the IC. The SVIN pin is very noise sensitive and placement of the capacitor is very critical. Use wide traces to connect to the SVIN and SGND pins.
- The signal ground pin (SGND) must be connected directly to the ground planes. Do not route the SGND pin to the PGND Pad on the top layer.
- Place the IC close to the point of load (POL).
- Use fat traces to route the input and output power lines.
- Signal and power grounds should be kept separate and connected at only one location.

Input Capacitor

- A 22µF X5R or X7R dielectrics ceramic capacitor is recommended on each of the PVIN pins for bypassing.
- Place the input capacitors on the same side of the board and as close to the IC as possible.
- Keep both the PVIN pin and PGND connections short.
- Place several vias to the ground plane close to the input capacitor ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply with power is suddenly applied.

Inductor

- Keep the inductor connection to the switch node (SW) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (SW) away from the feedback (FB) pin.
- To minimize noise, place a ground plane underneath the inductor.
- The inductor can be placed on the opposite side of the PCB with respect to the IC. It does not matter whether the IC or inductor is on the top or bottom as long as there is enough air flow to keep the power components within their temperature limits. The input and output capacitors must be placed on the same side of the board as the IC.

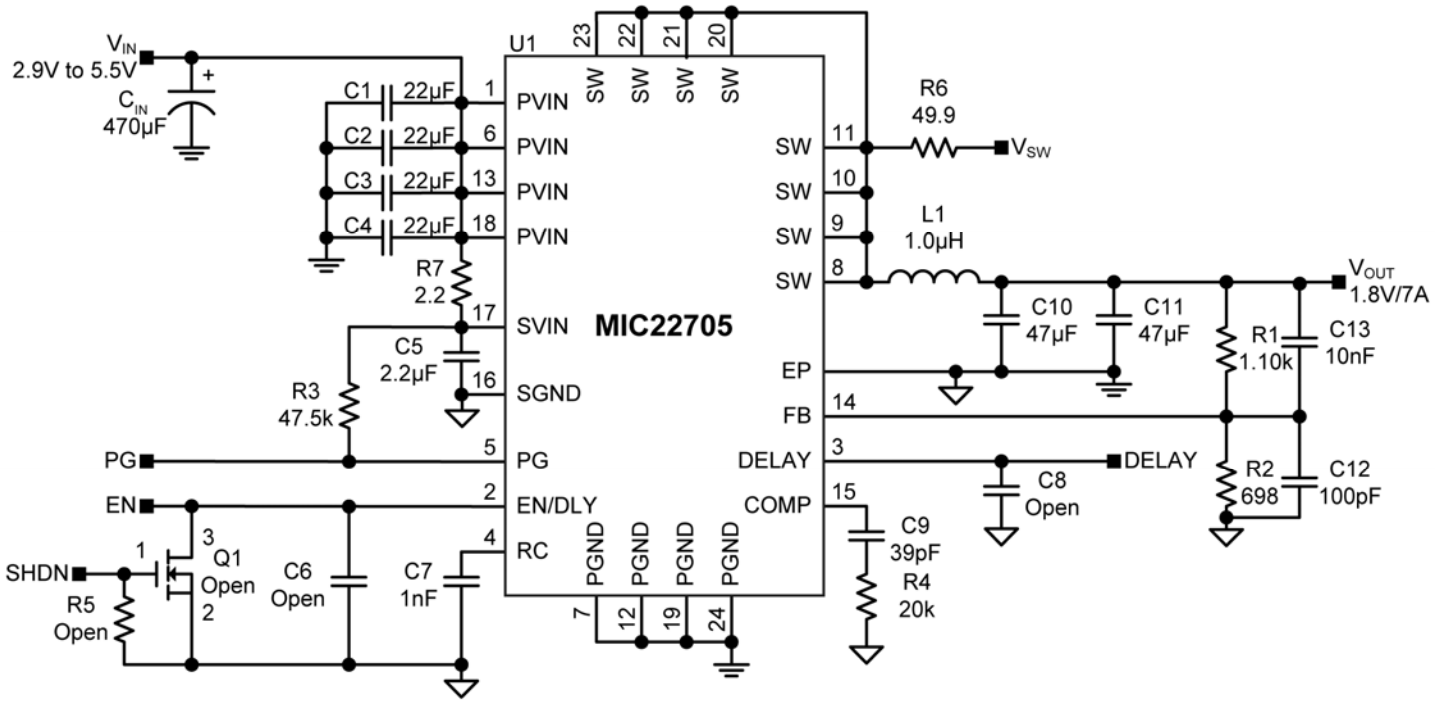
Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback divider network must be place close to the IC with the bottom of R2 connected to SGND.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high-current load trace can degrade the DC load regulation.

RC Snubber

- Place the RC snubber on either side of the board and as close to the SW pin as possible.

Evaluation Board Schematic



Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1, C2, C3, C4	C2012X5R0J226M	TDK[1]	22µF/6.3V, 0805, Ceramic Capacitor	5
	08056D226MAT	AVX[2]		
	GRM21BR60J226ME39L	Murata[3]		
C5	06036D225TAAT2A	AVX[2]	2.2µF/6.3V, Ceramic Capacitor, X5R, Size 0805	1
	GRM188R7160J225M	Murata[3]	2.2µF/6.3V, Ceramic Capacitor, X7R, Size 0805	
	C1608X5R0J225M	TDK[1]		
C13	GRM188R71H103KA01D	Murata[3]	10nF, 0603, Ceramic Capacitor	1
C7	Open(VJ0603Y102KXQCW1BC)	Vishay[4]	1nF, 0603, Ceramic Capacitor	1
	Open(GRM188R71H102KA01D)	Murata[3]	1nF/50V, X7R, 0603, Ceramic Capacitor	
	Open(C1608C0G1H102J)	TDK[1]	1nF/50V, COG, 0603, Ceramic Capacitor	
C6, C8	Open			
C9	GRM1555C1H390JZ01D	Murata[3]	39pF/50V, COG, 0402, Ceramic Capacitor	1
	VJ0402A390KXQCW1BC	BC Components[5]	39pF /10V, 0402, Ceramic Capacitor	
C10, C11	C3216X5R0J476M	TDK[1]	47µF/6.3V, X5R, 1206, Ceramic Capacitor	2
	GRM31CR60J476ME19	Murata[3]	47µF/6.3V, X5R, 1206, Ceramic Capacitor	
	GRM31CC80G476ME19L	Murata[3]	47µF/4V, X6S, 1206, Ceramic Capacitor	

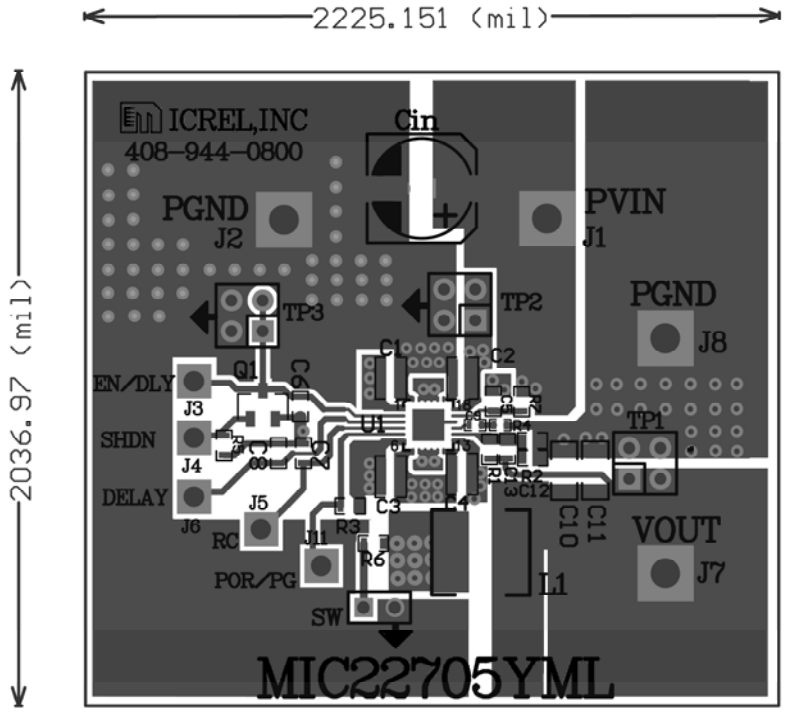
Bill of Materials (Continued)

Item	Part Number	Manufacturer	Description	Qty.
C12	VJ0402A101KXQCW1BC	Vishay[4]	100pF, 0603, Ceramic Capacitor	1
	GRM1555C1H101JZ01D	Murata[3]	100pF/50V, COG, 0402, Ceramic Capacitor	
L1	SPM6530T-1R0M120	TDK[1]	1µH, 12A, size 7x6.5x3mm	1
	HCP0704-1R0-R	Coiltronics[6]	1µH, 12A, size 6.8x6.8x4.2mm	
C_{IN}	BA1851A3477M	Epcos[7]	470µF/10V, Elect., 8×11.5	1
R1	CRCW06031101FKEYE3	Vishay[4]	Resistor, 1.1k, 0603, 1%	1
R2	CRCW04026980FKEYE3	Vishay[4]	Resistor, 698Ω, 0603, 1%	1
R3	CRCW06034752FKEYE3	Vishay[4]	Resistor, 47.5k, 0603, 1%	1
R4	CRCW04022002FKEYE3	Vishay[4]	Resistor, 20k, 0402, 1%	1
R5	Open(CRCW06031003FRT1)	Vishay[4]	Resistor, 100k, 0603, 1%	1
R6	CRCW060349R9FKEA	Vishay[4]	49.9Ω Resistor, 1%, Size 0603	1
R7	CRCW06032R20FKEA	Vishay[4]	2.2Ω Resistor, 1%, Size 0603	1
Q1	Open(2N7002E)		Signal MOSFET – SOT23-6	1
	Open(CMDPM7002A)	Central Semiconductor[8]		
U1	**MIC22705YML**	**Micrel, Inc.[6]**	**1MHz, 7A Integrated Switch High-Efficiency Synchronous Buck Regulator**	**1**

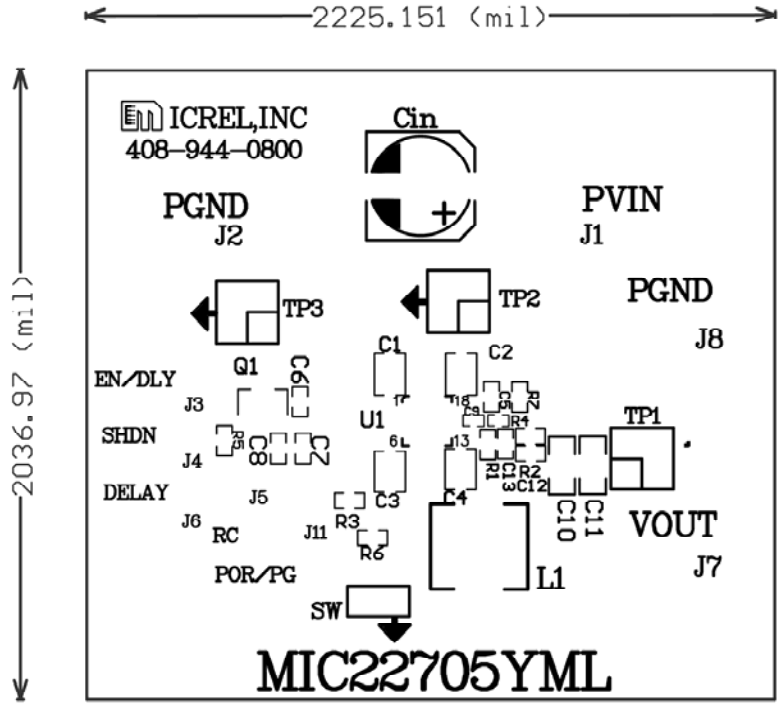
Notes:

1. TDK: www.tdk.com.
2. AVX.: www.avx.com.
3. Murata: www.murata.com.
4. Vishay Tel: www.vishay.com.
5. BC Components: www.bccomponents.com.
6. Coiltronics: www.coiltronics.com.
7. Epcos: www.epcos.com.
8. Central Semiconductor: www.centralsemi.com.
9. **Micrel, Inc.:** www.micrel.com.

PCB Layout Recommendations

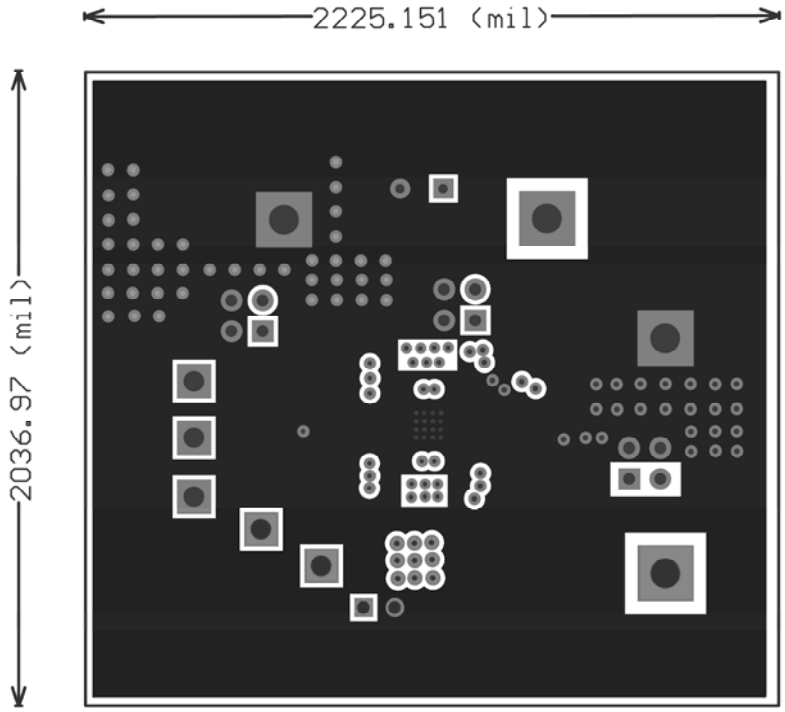


MIC22705 Evaluation Board Top Layer

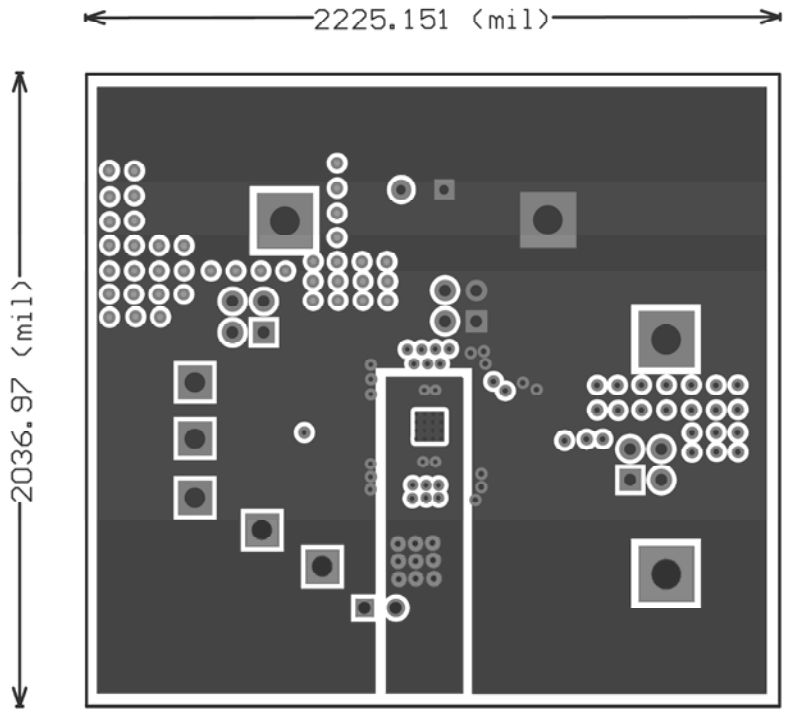


MIC22705 Evaluation Board Top Silk

PCB Layout Recommendations (Continued)

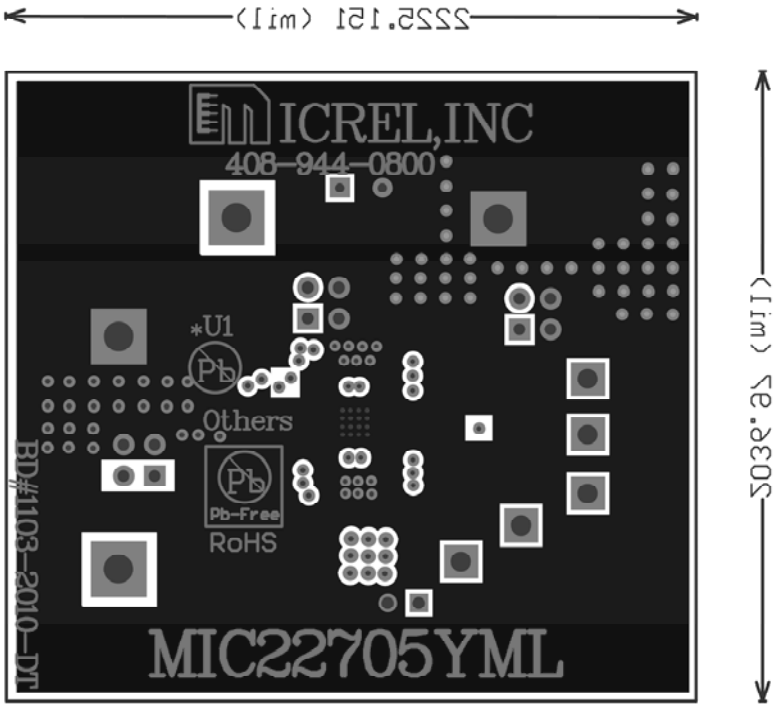


MIC22705 Evaluation Board Mid-Layer 1 (Ground Plane)

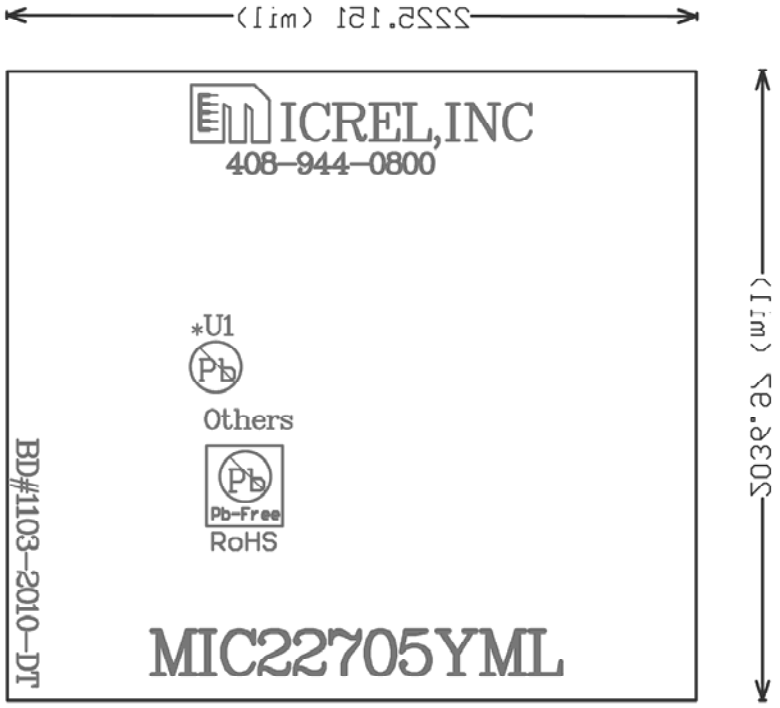


MIC22705 Evaluation Board Mid-Layer 2

PCB Layout Recommendations (Continued)

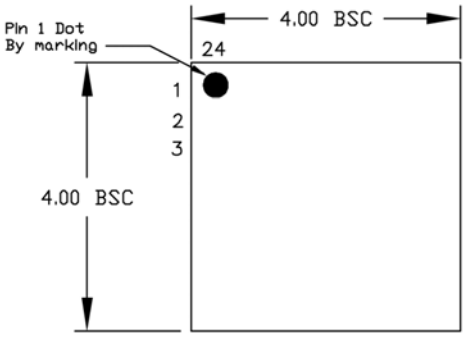


MIC22705 Evaluation Board Bottom Layer

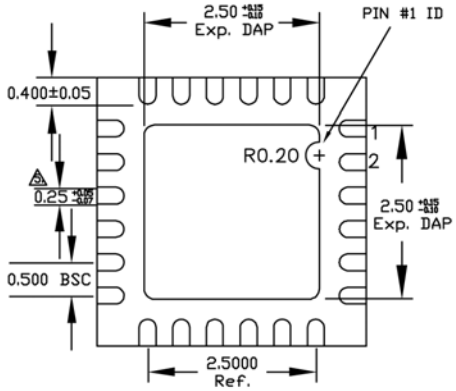


MIC22705 Evaluation Board Bottom Silk

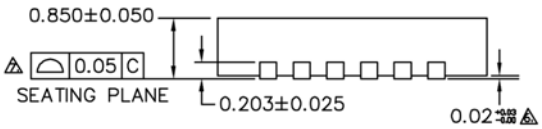
Package Information



TOP VIEW



BOTTOM VIEW

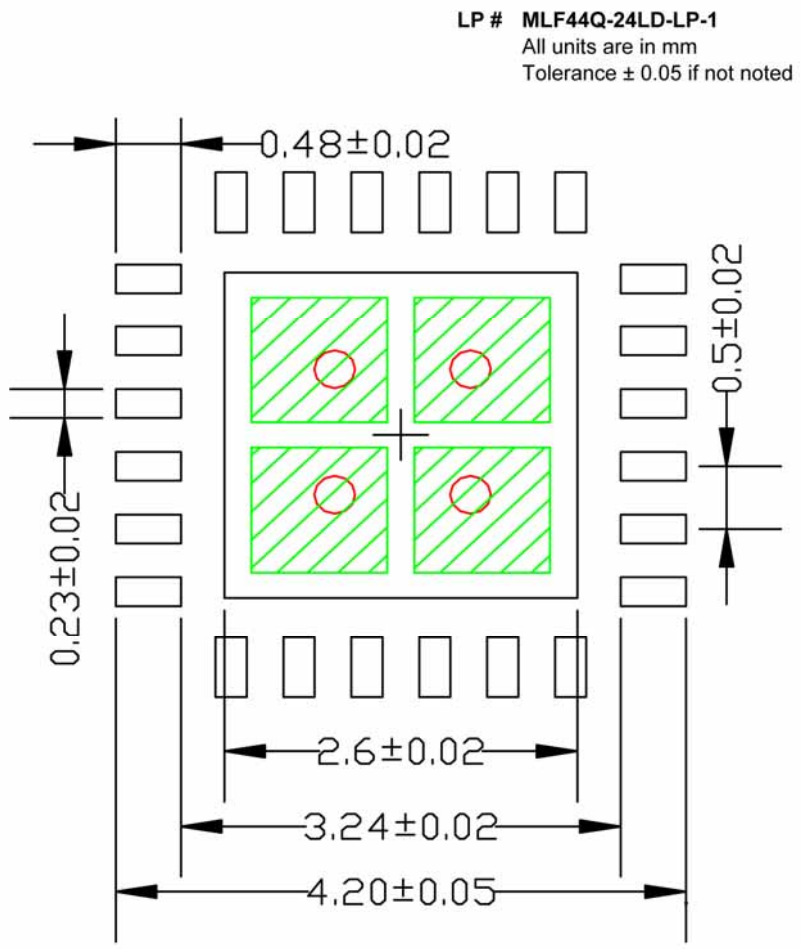


SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.
7. APPLIED FOR EXPOSED PAD AND TERMINALS.

24-Pin 4mm × 4mm MLF® (ML)

Recommended Landing Pattern



Red circle indicates Thermal Via. Size should be .300mm – .350mm in diameter, 1.00mm pitch, and it should be connected to GND plane for maximum thermal performance.

Green rectangle (with shaded area) indicates Solder Stencil Opening on exposed pad area. Size should be 1.00mm × 1.00mm in size, 1.20mm pitch.

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