5MHz, Dual Precision Rail-to-Rail Input-Output (RRIO) Op Amp

The ISL28236 is a low-power dual operational amplifier optimized for single supply operation from 2.4V to 5.5V, allowing operation from one lithium cell or two Ni-Cd batteries. The device features a gain-bandwidth product of 5MHz.

The ISL28236 features an Input Range Enhancement Circuit (IREC), which enables the amplifier to maintain CMRR performance for input voltages greater than the positive supply. The input signal is capable of swinging 0.25V above the positive supply and to the negative supply with only a slight degradation of the CMRR performance. The output operation is rail-to-rail.

The part typically draw less than 1mA supply current per amplifier while meeting excellent DC accuracy, AC performance, noise and output drive specifications. Operation is guaranteed over -40°C to +125°C temperature range.

Ordering Information

PART NUMBER (Note)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
ISL28236FBZ	28236 FBZ	8 Ld SOIC	MDP0027
ISL28236FBZ-T7*	28236 FBZ	8 Ld SOIC	MDP0027
Coming Soon ISL28236FUZ	8236Z	8 Ld MSOP	MDP0043
Coming Soon ISL28236FUZ-T7*	8236Z	8 Ld MSOP	MDP0043

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

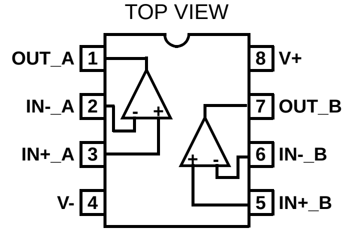
- 5MHz Gain Bandwidth Product @ A_V = 100
- 2mA Typical Supply Current
- 240µV Maximum Offset Voltage
- 6nA Typical Input Bias Current
- Down to 2.4V Single Supply Voltage Range
- Rail-to-rail Input and Output
- -40°C to +125°C Operation
- Pb-Free (RoHS compliant)

Applications

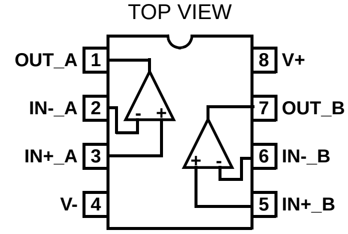
- Low-end Audio
- 4mA to 20mA Current Loops
- Medical Devices
- Sensor Amplifiers
- ADC Buffers
- DAC Output Amplifiers

Pinouts

ISL28236
(8 LD SOIC)
TOP VIEW



ISL28236
(8 LD MSOP)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage 5.75V
Supply Turn-on Voltage Slew Rate 1V/µs
Differential Input Current 5mA
Differential Input Voltage 0.5V
Input Voltage . . . . V- - 0.5V to V+ + 0.5V
ESD Rating
  Human Body Model 3kV
  Machine Model 300V

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
  8 Ld SO Package 120
  8 Ld MSOP Package 160
Storage Temperature Range . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . see link below
  http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Ambient Temperature Range . . . . -40°C to +125°C
Junction Temperature . . . . +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open, T_A = +25°C unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.** Temperature data established by characterization.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
DC SPECIFICATIONS						
V_{OS}	Input Offset Voltage	8 Ld SOIC	-240 **-250**	20	240 **250**	µV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage vs Temperature			0.4		µV/°C
I_{OS}	Input Offset Current	 T_A = -40°C to +125°C	-10 **-30**	2	10 **30**	nA
I_B	Input Bias Current	 T_A = -40°C to +125°C	-40 **-50**	6	40 **50**	nA
V_{CM}	Common-Mode Voltage Range	Guaranteed by CMRR	0		5	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 5V	90 **90**	115		dB
PSRR	Power Supply Rejection Ratio	V_+ = 2.4V to 5.5V	90 **90**	100		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 4V, R_L = 100kΩ to V_{CM}	600 **500**	1600		V/mV
		V_O = 0.5V to 4V, R_L = 1kΩ to V_{CM}		100		V/mV
V_{OUT}	Maximum Output Voltage Swing	Output low, R_L = 100kΩ to V_{CM}		1	10 **10**	mV
		Output low, R_L = 1kΩ to V_{CM}		47	70 **90**	mV
		Output high, R_L = 100kΩ to V_{CM}	4.99 **4.99**	4.997		V
		Output high, R_L = 1kΩ to V_{CM}	4.93 **4.91**	4.952		V
I_S	Supply Current			2	2.5 **2.6**	mA

Electrical Specifications $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, R_L = Open, $T_A = +25°C$ unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.** Temperature data established by characterization. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
I_O+	Short-Circuit Output Source Current	$R_L = 10\Omega$ to V_{CM}	50 **40**	70		mA
I_O-	Short-Circuit Output Sink Current	$R_L = 10\Omega$ to V_{CM}	50 **40**	70		mA
V_{SUPPLY}	Supply Operating Range	V_+ to V_-	2.4		5.5	V
AC SPECIFICATIONS						
GBW	Gain Bandwidth Product	$A_V = 100$, $R_F = 100k\Omega$, $R_G = R_L = 10k\Omega$ to V_{CM}		5		MHz
e_N	Input Noise Voltage Peak-to-Peak	f = 0.1Hz to 10Hz, $R_L = 10k\Omega$ to V_{CM}		0.4		μV_{P-P}
	Input Noise Voltage Density	$f_O = 1kHz$, $R_L = 10k\Omega$ to V_{CM}		15		nV/√Hz
i_N	Input Noise Current Density	$f_O = 10kHz$, $R_L = 10k\Omega$ to V_{CM}		0.35		pA/√Hz
CMRR at 120Hz	Input Common Mode Rejection Ratio	$V_{CM} = 0.1V_{P-P}$, $R_L = 10k\Omega$ to V_{CM}		90		dB
PSRR+ at 120Hz	Power Supply Rejection Ratio (V+)	V_+, $V_- = \pm1.2V$ and $\pm2.5V$, $V_{SOURCE} = 0.1V_{P-P}$, $R_L = 10k\Omega$ to V_{CM}		88		dB
PSRR- at 120Hz	Power Supply Rejection Ratio (V-)	V_+, $V_- = \pm1.2V$ and $\pm2.5V$ $V_{SOURCE} = 0.1V_{P-P}$, $R_L = 10k\Omega$ to V_{CM}		105		dB
Crosstalk at 10kHz	Channel A to Channel B	V_+, $V_- = \pm2.5V$; $A_V = 1$ $V_{SOURCE} = 0.4V_{P-P}$, $R_L = 10k\Omega$ to V_{CM}		140		dB
TRANSIENT RESPONSE						
SR	Slew Rate	$V_{OUT} = \pm1.5V$; $R_f = 50k\Omega$, $R_G = 50k\Omega$ to V_{CM}		±1.8		V/µs
t_r, t_f, Large Signal	Rise Time, 10% to 90%, V_{OUT}	$A_V = -1$, $V_{OUT} = 4V_{P-P}$, $R_L = 10k\Omega$ to V_{CM}		2.1		µs
	Fall Time, 90% to 10%, V_{OUT}	$A_V = -1$, $V_{OUT} = 4V_{P-P}$, $R_L = 10k\Omega$ to V_{CM}		2		µs
t_r, t_f, Small Signal	Rise Time, 10% to 90%, V_{OUT}	$A_V = +1$, $V_{OUT} = 100mV_{P-P}$, $R_L = 10k\Omega$ to V_{CM}		60		ns
	Fall Time, 90% to 10%, V_{OUT}	$A_V = +1$ $V_{OUT} = 100mV_{P-P}$, $R_L = 10k\Omega$ to V_{CM}		50		ns
t_S,	Settling Time to 0.01%; 4V Step	$V_{OUT} = 4V_{P-P}$; $R_L = 10k\Omega$ to V_{CM}		5.1		µs

NOTE:

2. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, R_L = Open

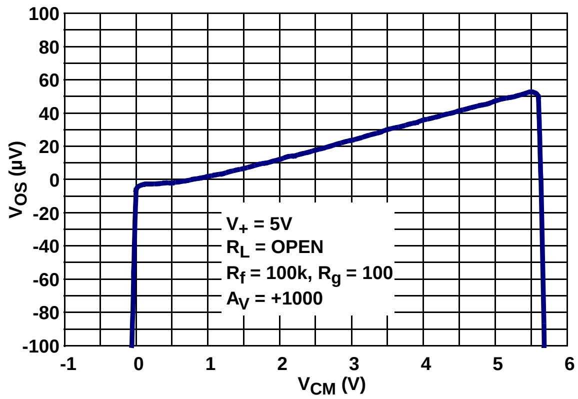


FIGURE 1. INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

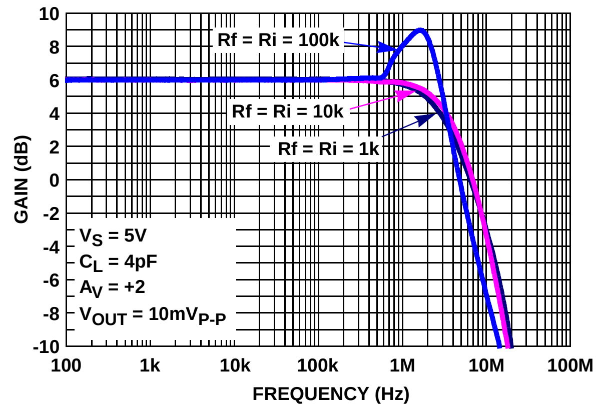


FIGURE 2. GAIN vs FREQUENCY vs FEEDBACK RESISTOR VALUES R_f/R_g

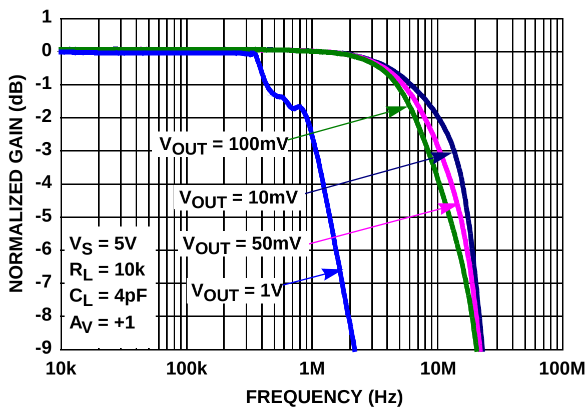


FIGURE 3. GAIN vs FREQUENCY vs V_{OUT}, R_L = 10k

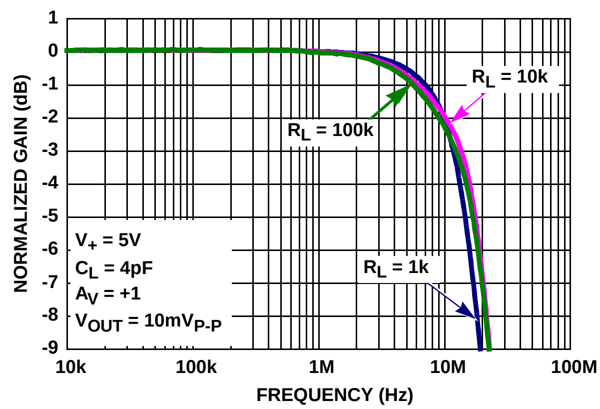


FIGURE 4. GAIN vs FREQUENCY vs R_L

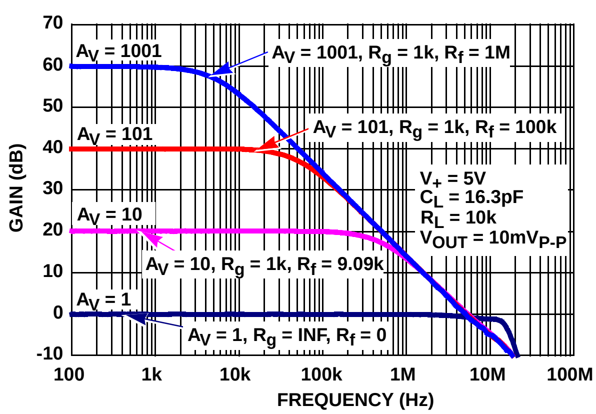


FIGURE 5. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

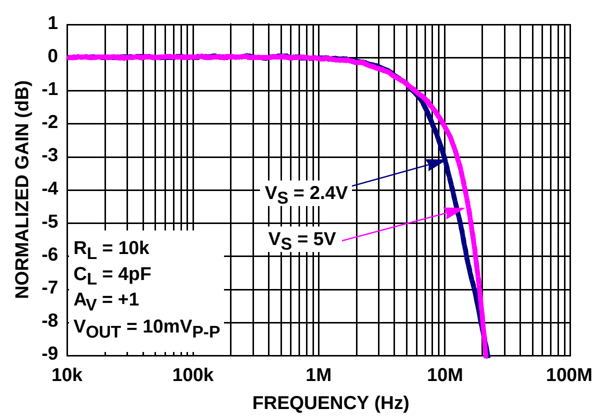


FIGURE 6. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

Typical Performance Curves $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, R_L = Open **(Continued)**

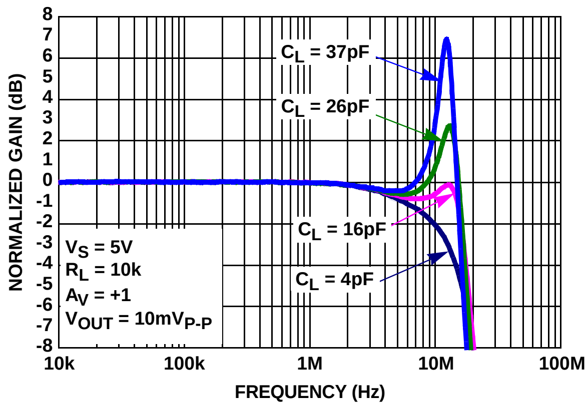


FIGURE 7. GAIN vs FREQUENCY vs C_L

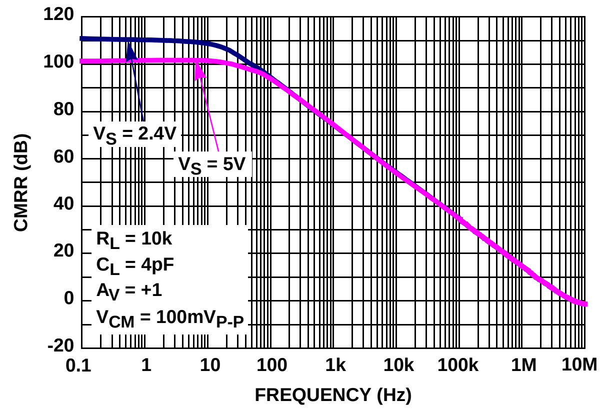


FIGURE 8. CMRR vs FREQUENCY; V_+ = 2.4V AND 5V

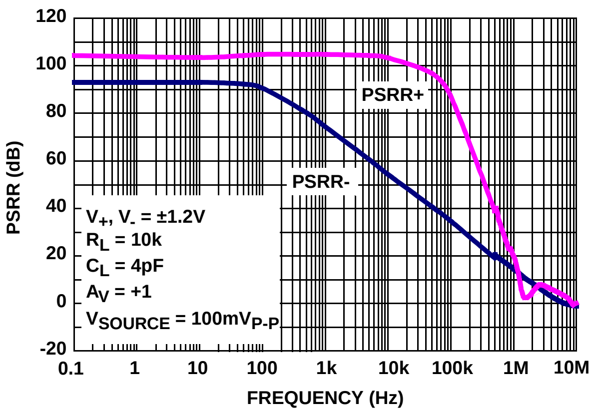


FIGURE 9. PSRR vs FREQUENCY, V_+, V_- = ±1.2V

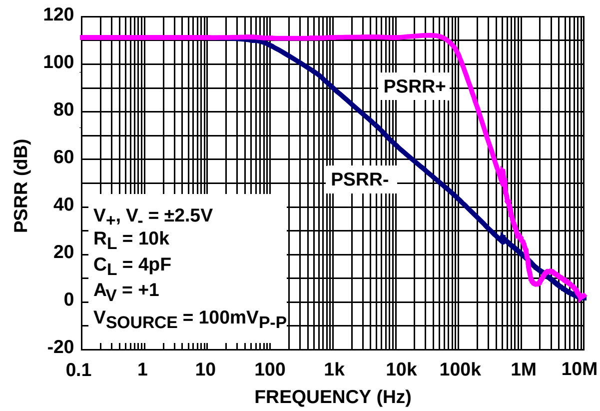


FIGURE 10. PSRR vs FREQUENCY, V_+, V_- = ±2.5V

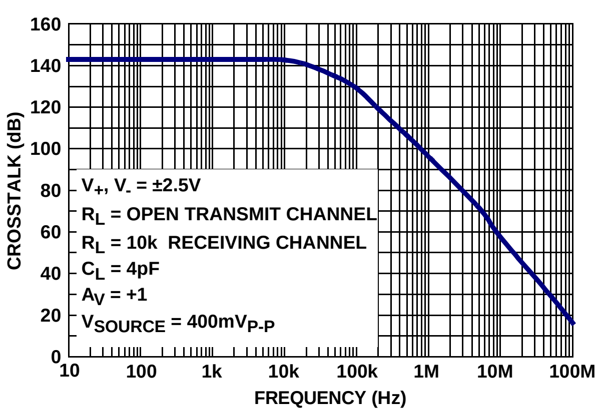


FIGURE 11. CROSSTALK vs FREQUENCY, V_+, V_- = ±2.5V

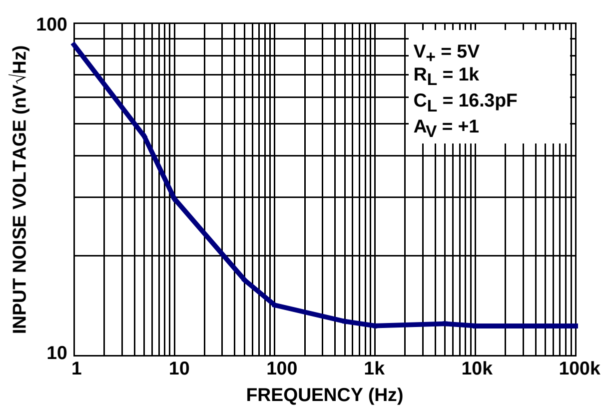


FIGURE 12. INPUT NOISE VOLTAGE DENSITY vs FREQUENCY

Typical Performance Curves $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, R_L = Open **(Continued)**

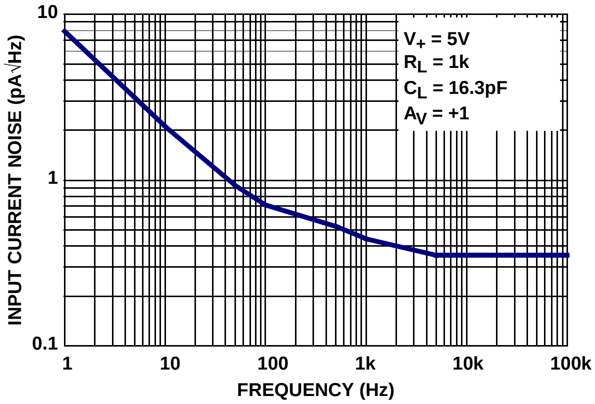


FIGURE 13. INPUT CURRENT NOISE DENSITY vs FREQUENCY

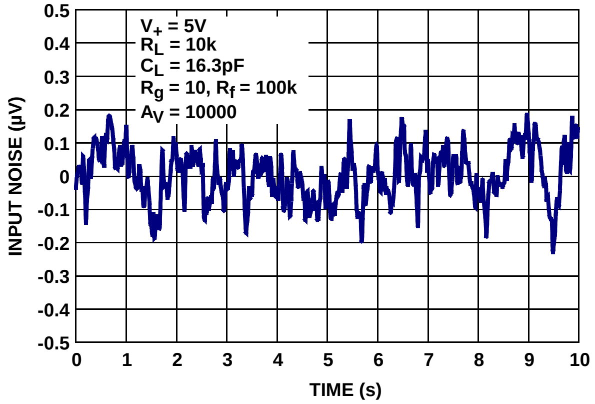


FIGURE 14. INPUT NOISE VOLTAGE 0.1Hz TO 10Hz

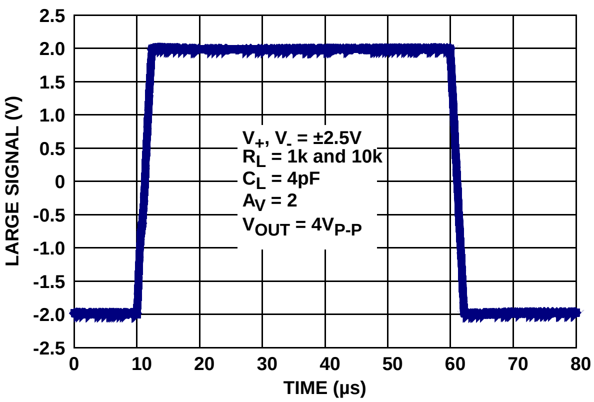


FIGURE 15. LARGE SIGNAL STEP RESPONSE

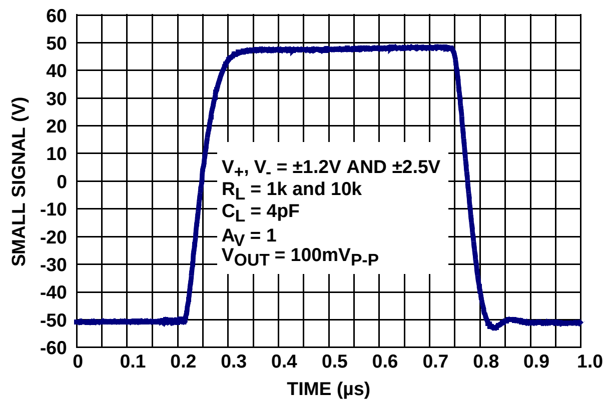


FIGURE 16. SMALL SIGNAL STEP RESPONSE

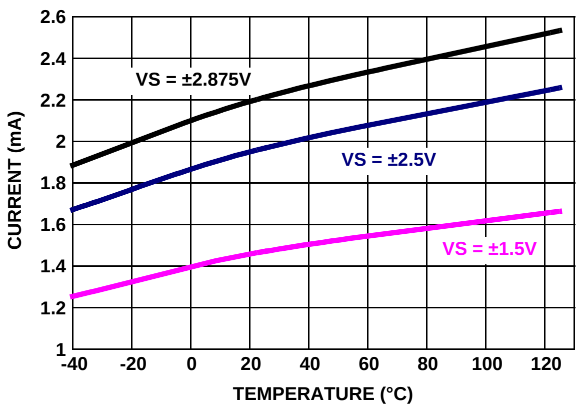


FIGURE 17. SUPPLY CURRENT vs TEMPERATURE vs SUPPLY VOLTAGE

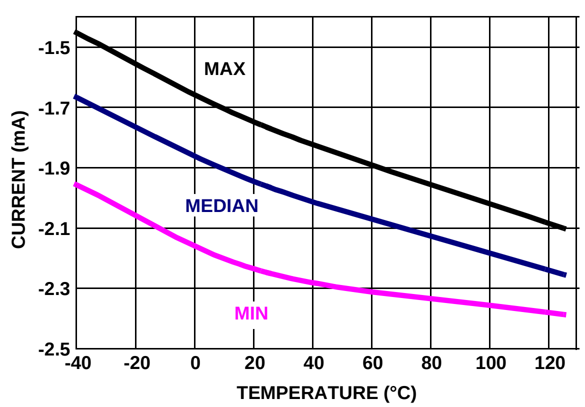


FIGURE 18. NEGATIVE SUPPLY CURRENT vs TEMPERATURE, V_+, $V_- = \pm2.5V$

Typical Performance Curves $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, R_L = Open **(Continued)**

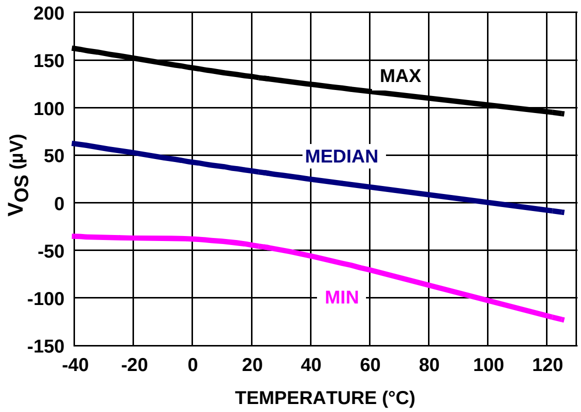


FIGURE 19. V_{OS} vs TEMPERATURE, V_+, $V_- = \pm1.2V$,

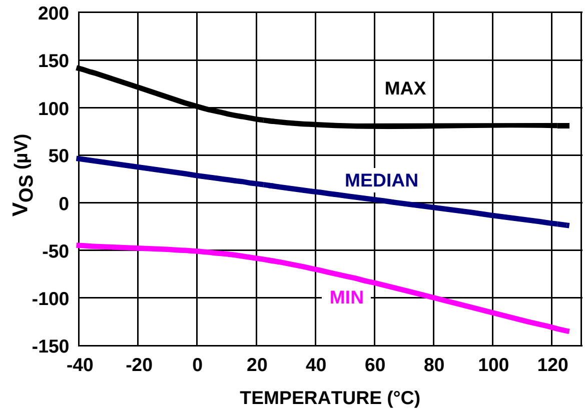


FIGURE 20. V_{OS} vs TEMPERATURE, V_+, $V_- = \pm2.5V$,

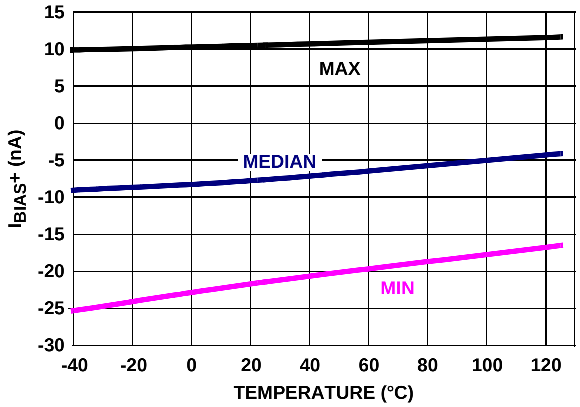


FIGURE 21. $I_{BIAS}+$ vs TEMPERATURE, V_+, $V_- = \pm2.5V$

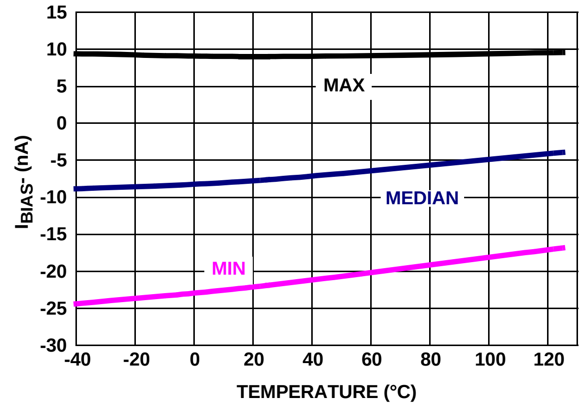


FIGURE 22. $I_{BIAS}-$ vs TEMPERATURE, V_+, $V_- = \pm2.5V$

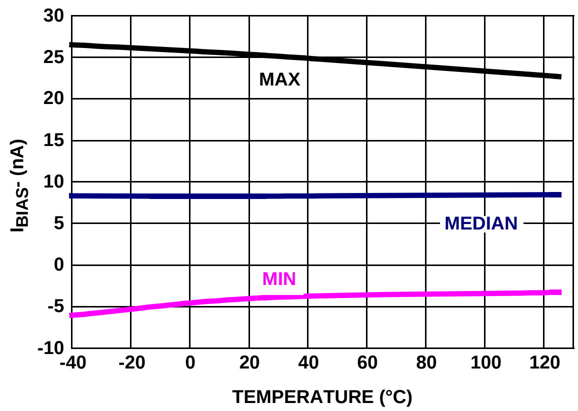


FIGURE 23. $I_{BIAS}+$ vs TEMPERATURE, V_+, $V_- = \pm1.2V$

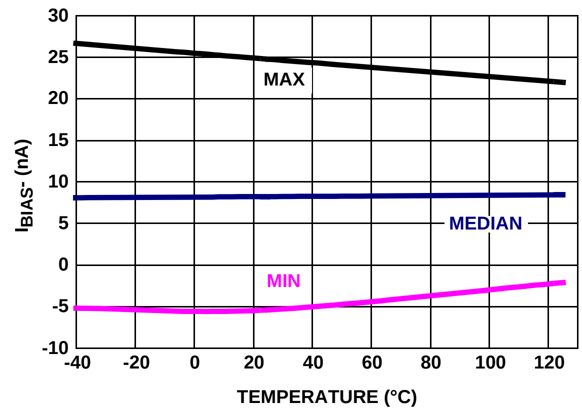


FIGURE 24. $I_{BIAS}-$ vs TEMPERATURE, V_+, $V_- = \pm1.2V$

Typical Performance Curves $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, R_L = Open **(Continued)**

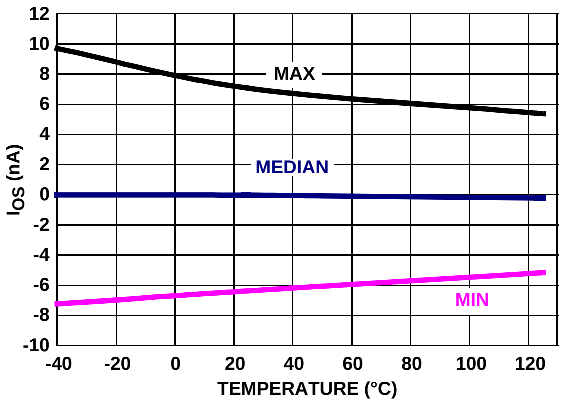


FIGURE 25. I_{OS} vs TEMPERATURE, V_+, $V_- = \pm2.5V$

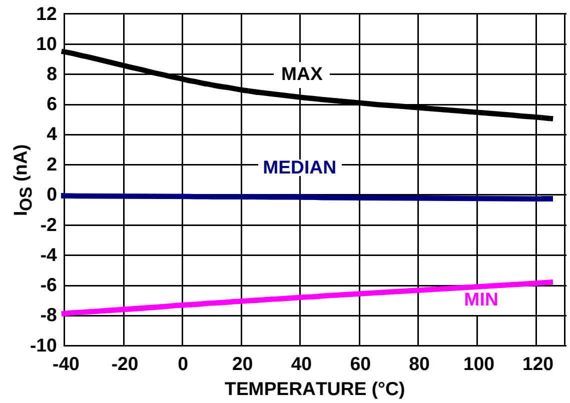


FIGURE 26. I_{OS} vs TEMPERATURE, V_+, $V_- = \pm1.2V$

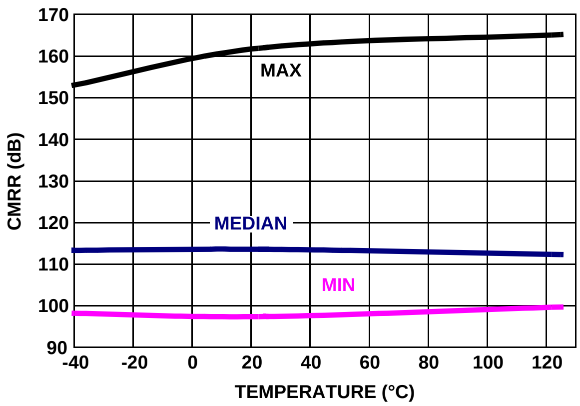


FIGURE 27. CMRR vs TEMPERATURE, V_+, $V_- = \pm2.5V$

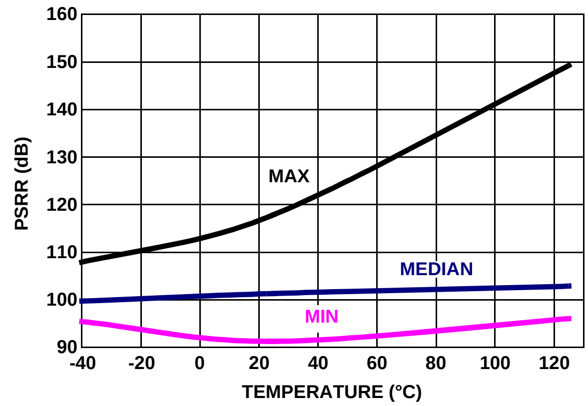


FIGURE 28. PSRR vs TEMPERATURE, V_+, $V_- = \pm1.2V$

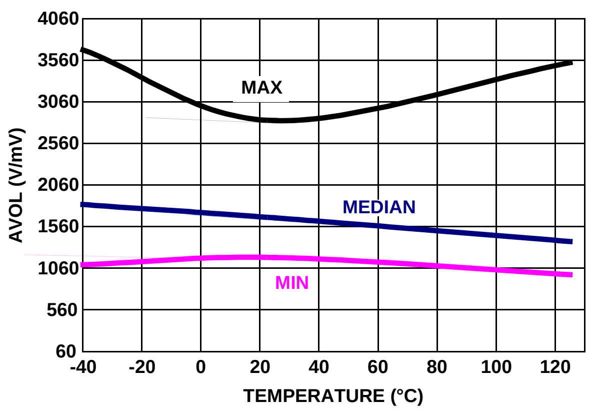


FIGURE 29. AVOL vs TEMPERATURE, V_+, $V_- = \pm2.5V$, $V_O = -2V$ TO $+2V$, $R_L = 100k$

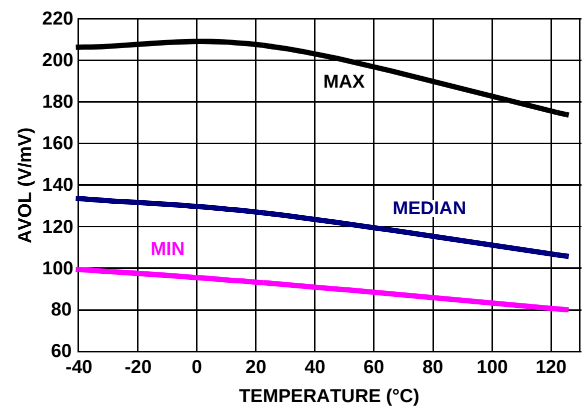


FIGURE 30. AVOL vs TEMPERATURE, V_+, $V_- = \pm2.5V$, $V_O = -2V$ TO $+2V$, $R_L = 1k$

Typical Performance Curves V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open **(Continued)**

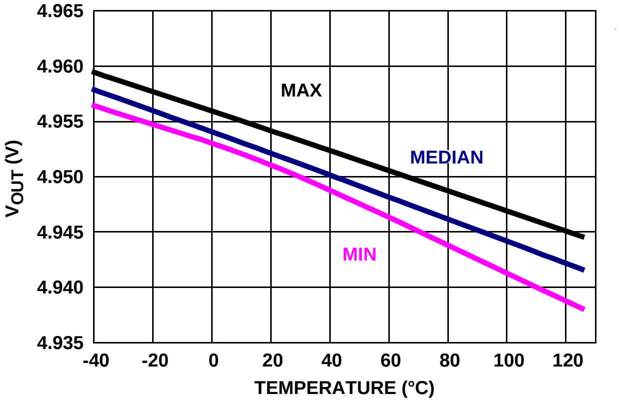


FIGURE 31. V_{OUT} HIGH vs TEMPERATURE, V_+, V_- = ±2.5V, R_L = 1k

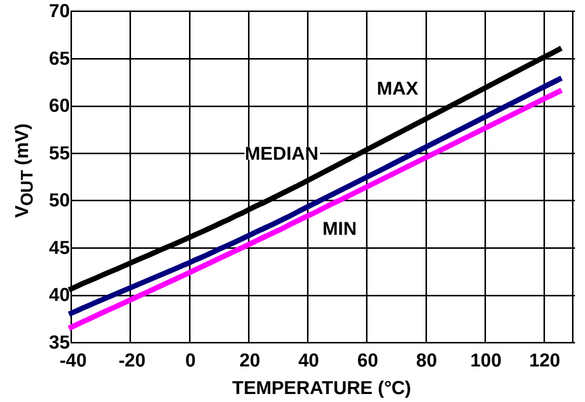


FIGURE 32. V_{OUT} LOW vs TEMPERATURE, V_+, V_- = ±2.5V, R_L = 1k

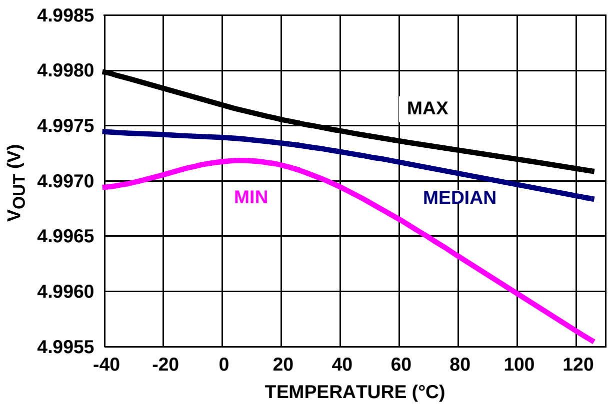


FIGURE 33. V_{OUT} HIGH vs TEMPERATURE, V_+, V_- = ±2.5V, R_L = 100k

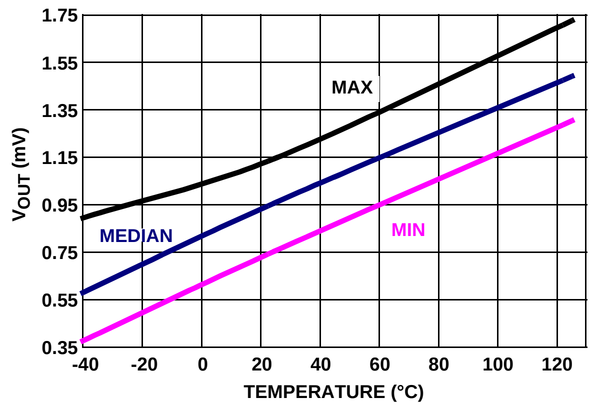


FIGURE 34. V_{OUT} LOW vs TEMPERATURE, V_+, V_- = ±2.5V, R_L = 100k

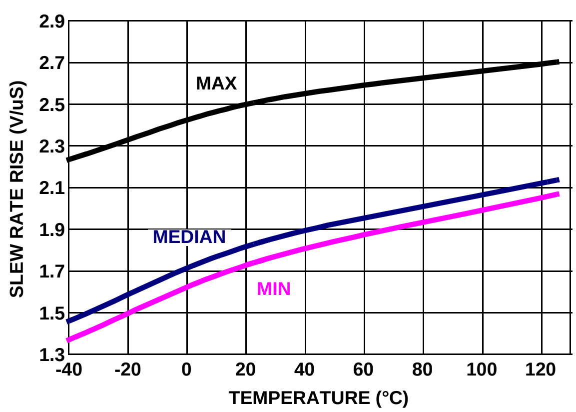
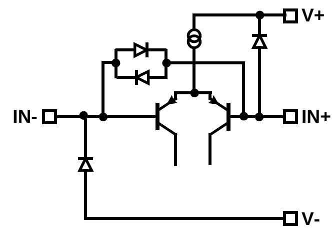
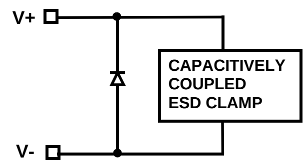
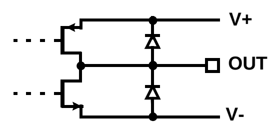


FIGURE 35. SLEW RATE RISE vs TEMPERATURE, V_{OUT} = ±1.5V, $V_{P-P}V_+$, V_- = ±2.5V, R_L = 100k

Pin Descriptions

ISL28236 (8 Ld SOIC) (8 Ld MSOP)	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
2 (A) 6 (B)	IN- IN-_A IN-_B	inverting input	 Circuit 1
3 (A) 5 (B)	IN+ IN+_A IN+_B	Non-inverting input	See Circuit 1
4	V-	Negative supply	 Circuit 2
1 (A) 7 (B)	OUT OUT_A OUT_B	Output	 Circuit 3
8	V+	Positive supply	See Circuit 2

Applications Information

Introduction

The ISL28236 is a dual channel Bi-CMOS rail-to-rail input, output (RRIO) micropower precision operational amplifier. The part is designed to operate from single supply (2.4V to 5.5V) or dual supply (±1.2V to ±2.75V). The ISL28236 has an input common mode range that extends 0.25V above the positive rail and down to the negative supply rail. The output operation can swing within about 3mV of the supply rails with a 100kΩ load.

Rail-to-Rail Input

Many rail-to-rail input stages use two differential input pairs, a long-tail PNP (or PFET) and an NPN (or NFET). Severe penalties have to be paid for this circuit topology. As the input signal moves from one supply rail to another, the operational amplifier switches from one input pair to the other. Thus causing drastic changes in input offset voltage and an undesired change in magnitude and polarity of input offset current.

The ISL28236 solves this problem using an internal charge-pump to provide a voltage boost to the V+ supply rail driving the input differential pair. This results in extending the input common voltage rails to 0.25V beyond the V+ positive rail. The input offset voltage exhibits a smooth behavior throughout the extended common-mode input range. The input bias current versus the common-mode voltage range gives an undistorted behavior from the negative rail to 0.25V higher than the positive rail.

Power Supply Decoupling

The internal charge pump operates at approximately 27MHz and oscillator ripple doesn't show up in the 5MHz bandwidth of the amplifier. Good power supply decoupling with 0.01µF capacitors at each device power supply pin, is the most effective way to reduce oscillator ripple at the amplifier output. Figure 36 shows the electrical connection of these capacitors using split power supplies. For single supply operation with V- tied to a ground plane, only a single 0.01µF capacitor from V+ is needed. When multiple ISL28236 op amps are used on a single PC board, each op amp will require a 0.01µF decoupling capacitor at each supply pin

Rail-to-Rail Output

The rail-rail output stage uses CMOS devices that typically swing to within 3mV of the supply rails with a 100kΩ load. The NMOS sinks current to swing the output in the negative direction. The PMOS sources current to swing the output in the positive direction.

Current Limiting

These devices have no internal current-limiting circuitry. If the output is shorted, it is possible to exceed the Absolute Maximum Rating for output current or power dissipation, potentially resulting in the destruction of the device.

Results of Overdriving the Output

Caution should be used when overdriving the output for long periods of time. Overdriving the output can occur in two ways.

1. The input voltage times the gain of the amplifier exceeds the supply voltage by a large value or,
2. The output current required is higher than the output stage can deliver.

These conditions can result in a shift in the Input Offset Voltage (V_{OS}) (as much as 1µV/hr. of exposure under these conditions).

IN+ and IN- Input Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. They also contain back-to-back diodes across the input terminals (see “Pin Descriptions” on page 10 - Circuit 1). For applications where the input differential voltage is expected to exceed 0.5V, an external series resistor must be used to ensure the input currents never exceed 5mA (Figure 36).

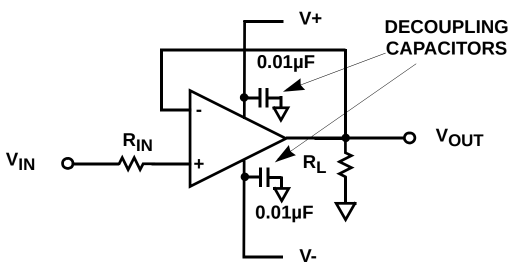


FIGURE 36. LOCAL POWER SUPPLY DECOUPLING AND INPUT CURRENT LIMITING

Limitations of the Differential Input Protection

If the input differential voltage is expected to exceed 0.5V, an external current limiting resistor must be used to ensure the input current never exceeds 5mA. For non-inverting unity gain applications, the current limiting can be via a series IN+ resistor, or via a feedback resistor of appropriate value. For other gain configurations, the series IN+ resistor is the best choice, unless the feedback (R_F) and gain setting (R_G) resistors are both sufficiently large to limit the input current to 5mA.

Large differential input voltages can arise from several sources:

1. During open loop (comparator) operation. Used this way, the IN+ and IN- voltages don’t track, so differentials arise.
2. When the amplifier is disabled but an input signal is still present. An R_L or R_G to GND keeps the IN- at GND, while the varying IN+ signal creates a differential voltage. Mux Amp applications are similar, except that the active channel V_{OUT} determines the voltage on the IN- terminal.
3. When the slew rate of the input pulse is considerably faster than the op amp’s slew rate. If the V_{OUT} can’t keep up with the IN+ signal, a differential voltage results, and visible distortion occurs on the input and output signals. To avoid this issue, keep the input slew rate below 1.9V/µs, or use appropriate current limiting resistors.

Large (>2V) differential input voltages can also cause an increase in disabled I_{CC}.

Using Only One Channel

If the application only requires one channel, the user must configure the unused channel to prevent it from oscillating. The unused channel will oscillate if the input and output pins are floating. This will result in higher than expected supply currents and possible noise injection into the channel being used. The proper way to prevent this oscillation is to short the output to the negative input and ground the positive input (as shown in Figure 37).

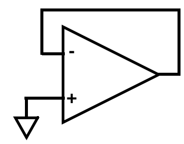


FIGURE 37. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

Power Dissipation

It is possible to exceed the +125°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related in Equation 1:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} x PD_{MAXTOTAL}) \qquad \text{(EQ. 1)}$$

where:

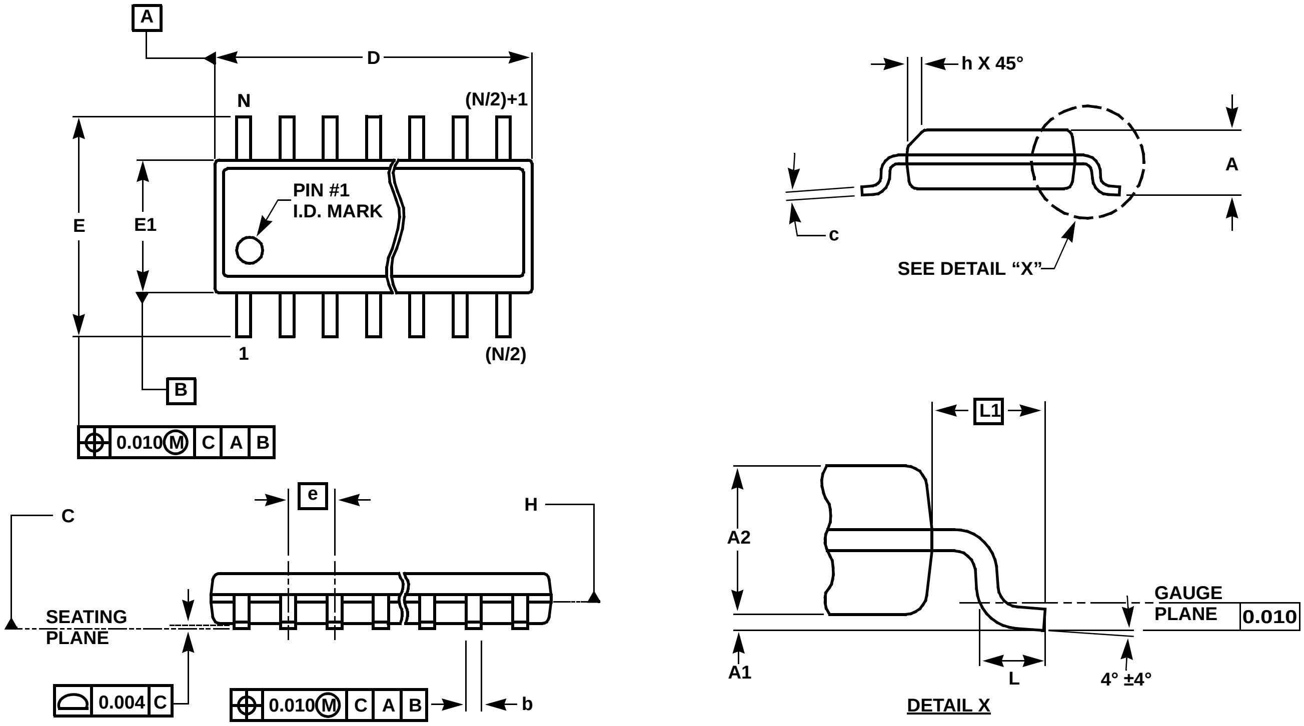
- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \qquad \text{(EQ. 2)}$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Total supply voltage
- I_{MAX} = Maximum supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

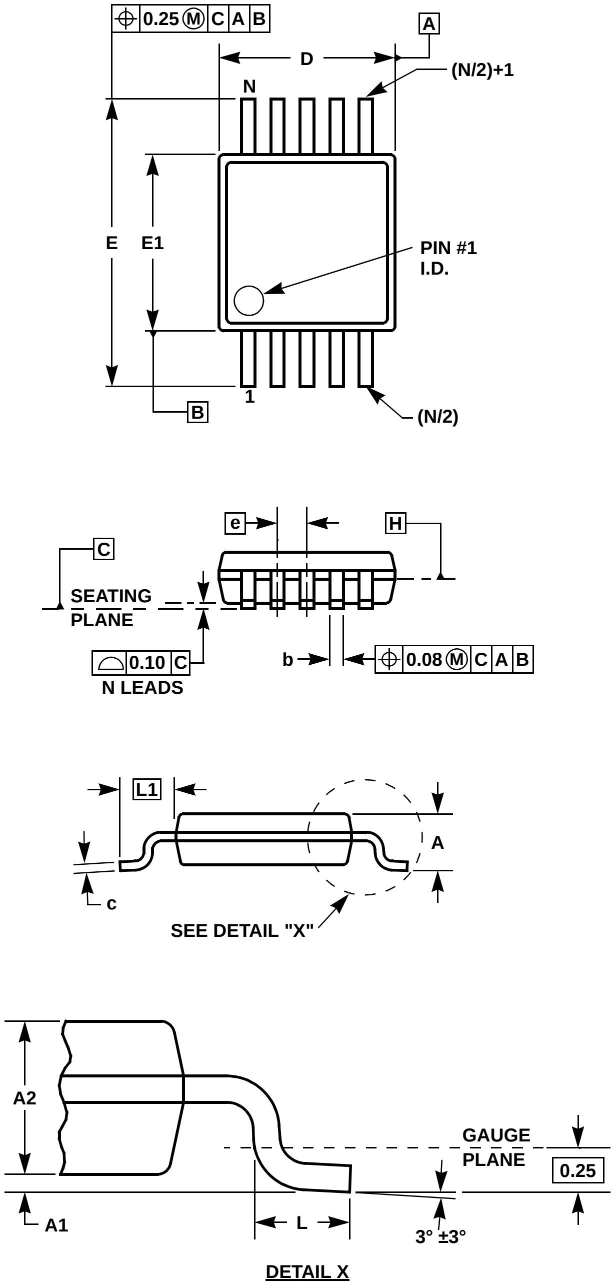
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

Mini SO Package Family (MSOP)



MDP0043

MINI SO PACKAGE FAMILY

SYMBOL	MILLIMETERS MSOP8	MILLIMETERS MSOP10	TOLERANCE	NOTES
A	1.10	1.10	Max.	-
A1	0.10	0.10	±0.05	-
A2	0.86	0.86	±0.09	-
b	0.33	0.23	+0.07/-0.08	-
c	0.18	0.18	±0.05	-
D	3.00	3.00	±0.10	1, 3
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

Rev. D 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.