74HC253; 74HCT253

Dual 4-input multiplexer; 3-state

Rev. 03 — 22 April 2010 Product data sheet

1. General description

The 74HC253; 74HCT253 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL).

The 74HC253; 74HCT253 provides a dual 4-input multiplexer with 3-state outputs which selects 2 bits of data from up to four sources selected by common data select inputs (S0, S1). The two 4-input multiplexer circuits have individual active LOW output enable inputs ($1\overline{OE}$, $2\overline{OE}$).

The 74HC253 and 74HCT253 are the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels applied to S0 and S1. The outputs are forced to a high-impedance OFF-state when $n\overline{OE}$ is HIGH.

The logic equations for the outputs are:

$$1Y = 1\overline{OE} \bullet (1I0 \bullet \overline{S1} \bullet \overline{S0} + 1I1 \bullet \overline{S1} \bullet S0 + 1I2 \bullet S1 \bullet \overline{S0} + 1I3 \bullet S1 \bullet S0)$$

$$2Y = 2\overline{OE} \bullet (2I0 \bullet \overline{S1} \bullet \overline{S0} + 2I1 \bullet \overline{S1} \bullet S0 + 2I2 \bullet S1 \bullet \overline{S0} + 2I3 \bullet S1 \bullet S0)$$

2. Features and benefits

- Non-inverting data path
- 3-state outputs interface directly with system bus
- Complies with JEDEC standard no. 7A
- Common select inputs
- Separate output enable inputs
- Input levels:
  - For 74HC253: CMOS level
  - For 74HCT253: TTL level
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Applications

- Data selectors
- Data multiplexers

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC253N	−40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HCT253N				
74HC253D	−40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT253D				
74HC253DB	−40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT253DB				

5. Functional diagram

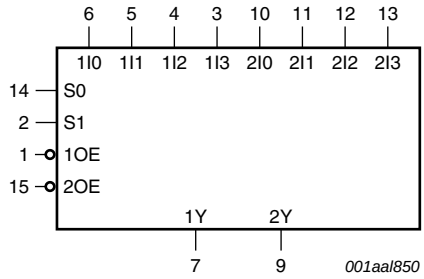

Fig 1. Logic symbol

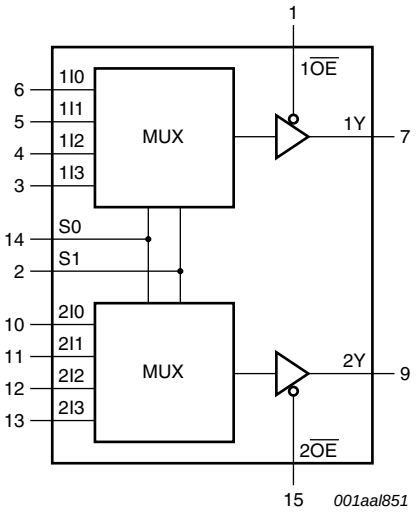

Fig 2. Functional diagram

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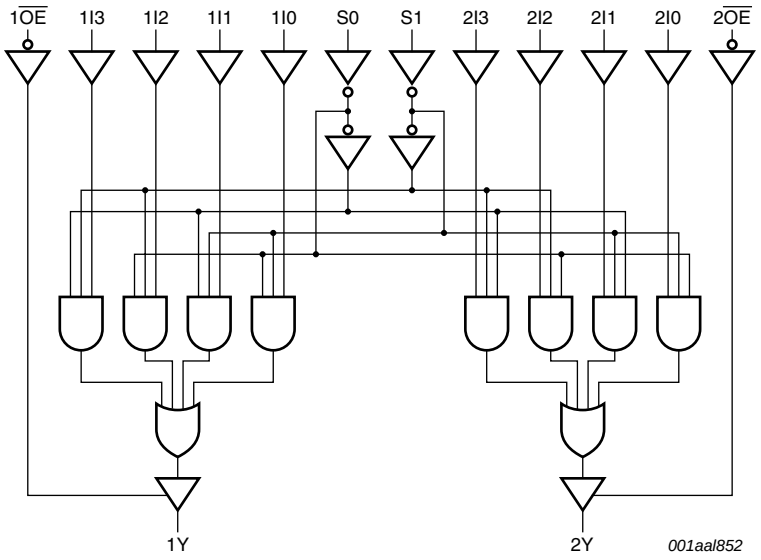

Fig 3. Logic diagram

6. Pinning information

6.1 Pinning

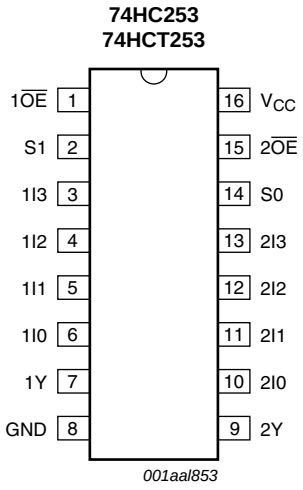

Fig 4. Pin configuration DIP16, SO16

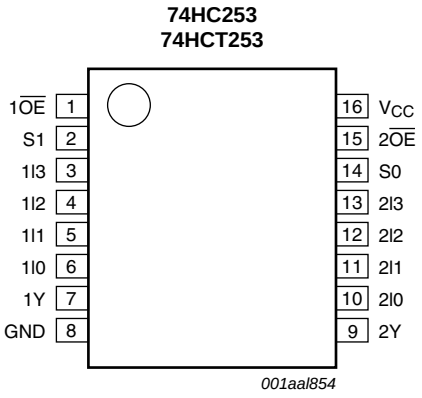

Fig 5. Pin configuration SSOP16

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6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{OE}$, $2\overline{OE}$	1, 15	output enable inputs (active LOW)
S0, S1	14, 2	data select inputs
1I0, 1I1, 1I2, 1I3	6, 5, 4, 3	data inputs source 1
1Y	7	multiplexer output source 1
GND	8	ground (0 V)
2Y	9	multiplexer output source 2
2I0, 2I1, 2I2, 2I3	10, 11, 12, 13	data inputs source 2
V_{CC}	16	supply voltage

7. Functional description

Table 3. Function table[1]

select Inputs		data inputs				output enable	output
S0	**S1**	**nI0**	**nI1**	**nI2**	**nI3**	**$n\overline{OE}$**	**nY**
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±50	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V		-	±35	mA
I_{CC}	supply current			-	70	mA
I_{GND}	ground current			–70	-	mA
T_{stg}	storage temperature			–65	+150	°C

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Table 4. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
P_{tot}	total power dissipation	T_{amb} = −40 °C to +125 °C				
	DIP16 package		[2]	-	750	mW
	SO16 package		[3]	-	500	mW
	SSOP16 package		[4]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P_{tot} derates linearly with 12 mW/K above 70 °C.

[3] P_{tot} derates linearly with 8 mW/K above 70 °C.

[4] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC253			74HCT253			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		−40	-	+125	−40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC253										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V

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Table 6. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = −20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = −20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = −20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = −6.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = −7.8 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 6.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 7.8 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±0.5	-	±5.0	-	±10.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA
C_I	input capacitance		-	3.5	-					pF
74HCT253										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = −20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = −6 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 6.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 5.5 V; $V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; I_O = 0 A	-	-	±0.5	-	±5.0	-	±10	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8.0	-	80	-	160	μA

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Table 6. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 2.1$ V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A								
		per input pin; 1In, 2In inputs	-	40	144	-	180	-	196	µA
		per input pin; n$\overline{OE}$ input	-	110	396	-	495	-	539	µA
		per input pin; Sn input	-	110	396	-	495	-	539	µA
C_I	input capacitance		-	3.5	-					pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); For test circuit see Figure 8.

Symbol	Parameter	Conditions		25 °C		−40 °C to +85 °C	−40 °C to +125 °C	Unit
				Typ	Max	Max	Max	
74HC253								
t_{pd}	propagation delay	1In to 1Y or 2In to 2Y; see Figure 6	[1]					
		V_{CC} = 2.0 V		55	175	220	265	ns
		V_{CC} = 4.5 V		20	35	44	53	ns
		V_{CC} = 5.0 V; C_L = 15 pF		17	-	-	-	ns
		V_{CC} = 6.0 V		16	30	37	45	ns
		Sn to nY; see Figure 6						
		V_{CC} = 2.0 V		58	175	220	265	ns
		V_{CC} = 4.5 V		21	35	44	53	ns
		V_{CC} = 5.0 V; C_L = 15 pF		18	-	-	-	ns
		V_{CC} = 6.0 V		17	30	37	45	ns
t_{en}	enable time	n$\overline{OE}$ to nY; see Figure 7	[2]					
		V_{CC} = 2.0 V		30	100	125	150	ns
		V_{CC} = 4.5 V		11	20	25	30	ns
		V_{CC} = 6.0 V		9	17	21	26	ns
t_{dis}	disable time	n$\overline{OE}$ to nY; see Figure 7	[3]					
		V_{CC} = 2.0 V		41	150	190	225	ns
		V_{CC} = 4.5 V		15	30	38	45	ns
		V_{CC} = 6.0 V		12	26	33	38	ns

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Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); For test circuit see Figure 8.

Symbol	Parameter	Conditions		25 °C		−40 °C to +85 °C	−40 °C to +125 °C	Unit
				Typ	Max	Max	Max	
t_t	transition time	see Figure 6	[4]					
		V_{CC} = 2.0 V		14	60	75	90	ns
		V_{CC} = 4.5 V		5	12	15	18	ns
		V_{CC} = 6.0 V		4	10	13	15	ns
C_{PD}	power dissipation capacitance	per multiplexer; V_I = GND to V_{CC}	[5]	55	-			pF
74HCT253								
t_{pd}	propagation delay	1In to 1Y or 2In to 2Y; see Figure 6	[1]					
		V_{CC} = 4.5 V		20	38	48	57	ns
		V_{CC} = 5.0 V; C_L = 15 pF		17	-	-		ns
		Sn to nY; see Figure 6						
		V_{CC} = 4.5 V		22	40	50	60	ns
		V_{CC} = 5.0 V; C_L = 15 pF		19	-			ns
t_{en}	enable time	$n\overline{OE}$ to nY; V_{CC} = 4.5 V; see Figure 7	[2]	14	30	38	45	ns
t_{dis}	disable time	$n\overline{OE}$ to nY; V_{CC} = 4.5 V; see Figure 7	[3]	13	30	38	45	ns
t_t	transition time	V_{CC} = 4.5 V; see Figure 6		5	12	15	18	ns
C_{PD}	power dissipation capacitance	per multiplexer; V_I = GND to V_{CC}	[5]	55	-			pF

[1] t_{pd} is the same as t_{PHL}, t_{PLH}.

[2] t_{en} is the same as t_{PZH}, t_{PZL}.

[3] t_{dis} is the same as t_{PHZ}, t_{PLZ}.

[4] t_t is the same as t_{THL}, t_{TLH}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

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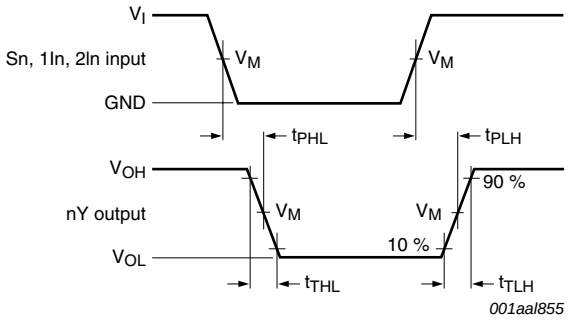
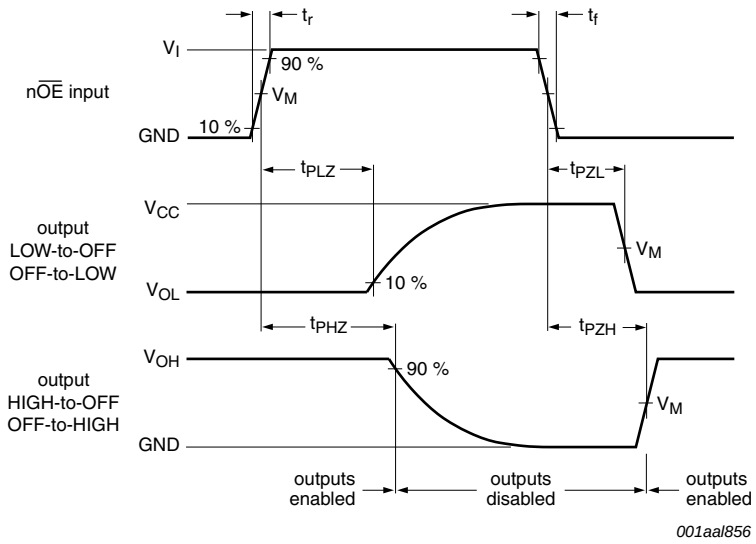
12. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Propagation delays input (Sn, 1In, 2In) to output (nY) and output (nY) transition times



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. 3-state output enable and disable times

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC253	$0.5V_{CC}$	$0.5V_{CC}$
74HCT253	1.3 V	1.3 V

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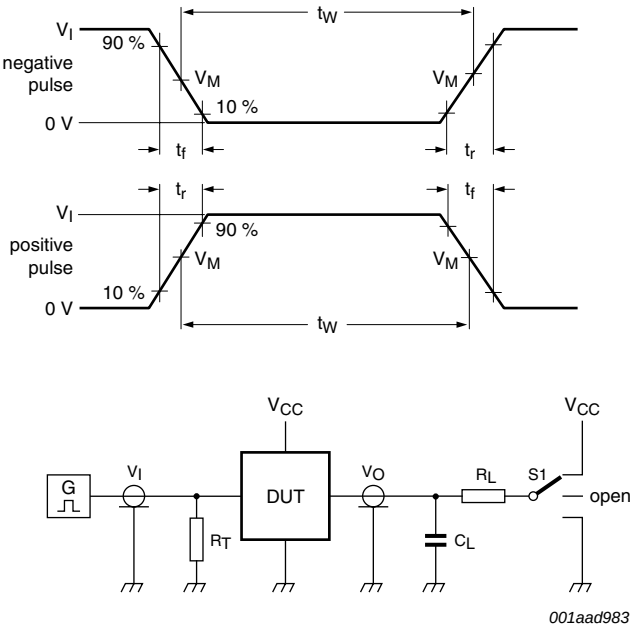

Measurement points are given in Table 8 and test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistor.

Fig 8. Test circuit for switching times

Table 9. Test data

Type	Input		Load		Switch position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC253	V_{CC}	6 ns	50 pF	1 kΩ	open	GND	V_{CC}
74HCT253	3 V	6 ns	50 pF	1 kΩ	open	GND	V_{CC}

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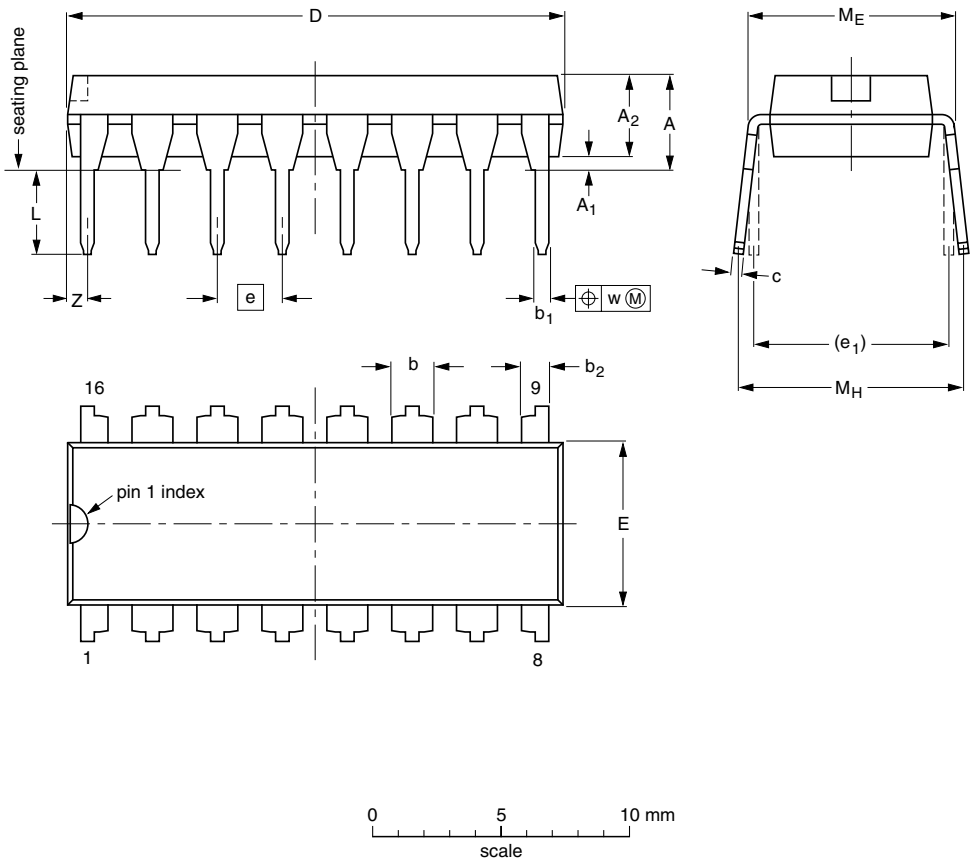
13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 9. Package outline SOT38-4 (DIP16)

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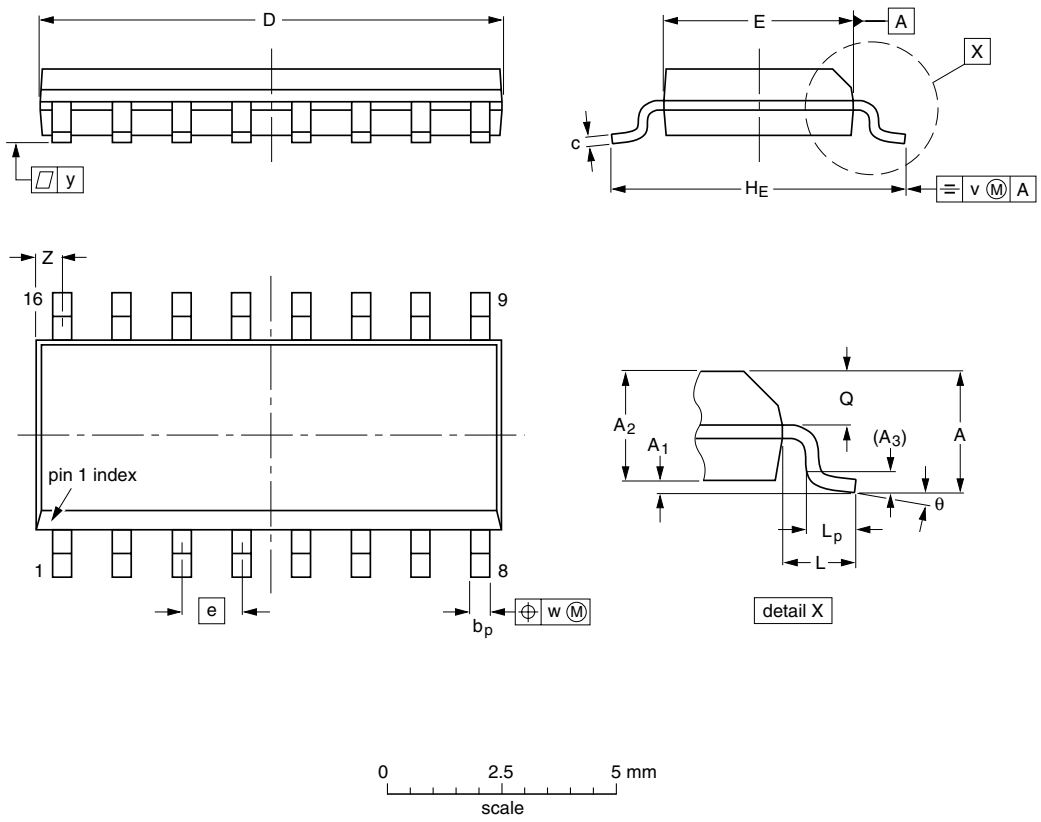
SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT109-1 (SO16)

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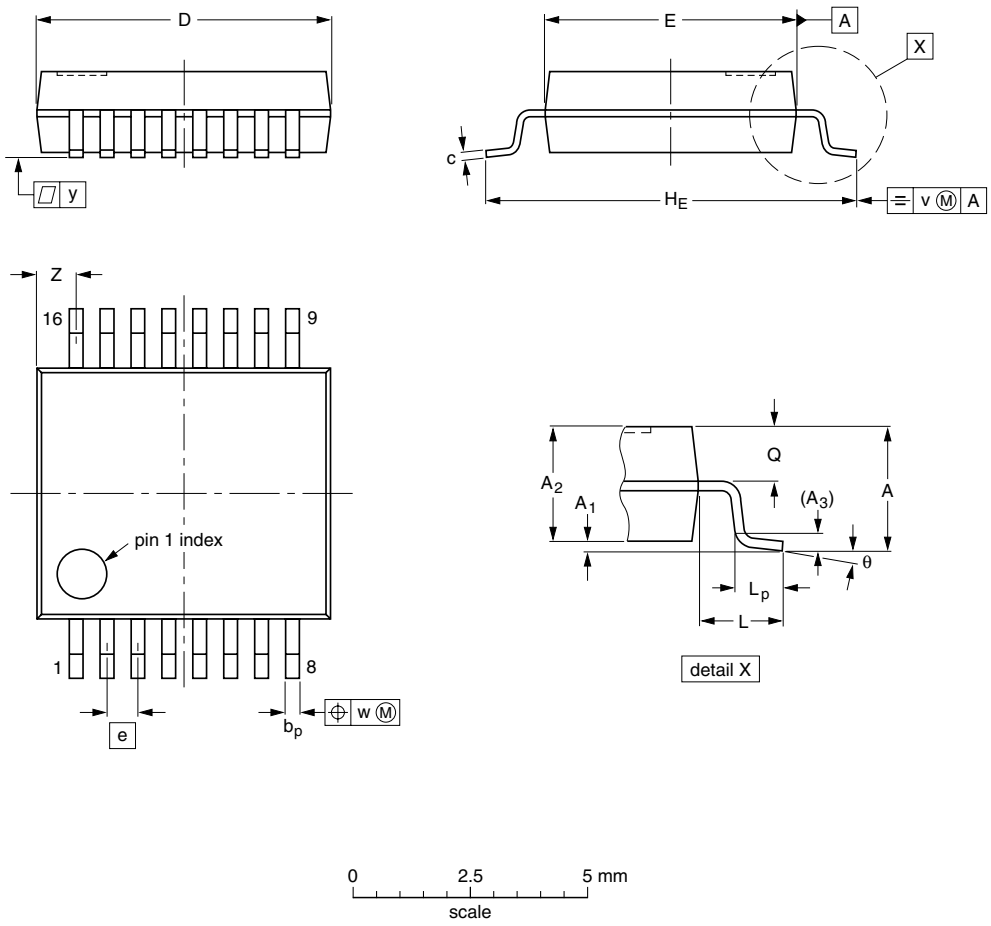
SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT338-1 (SSOP16)

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14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT253_3	20100422	Product data sheet	-	74HC_HCT253_CNV_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT253_CNV_2	970828	Product specification	-	-

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16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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