CY14B256Q1
CY14B256Q2
CY14B256Q3

256-Kbit (32 K × 8) Serial (SPI) nvSRAM

Features

- 256-Kbit nonvolatile static random access memory (nvSRAM)
  - Internally organized as 32 K × 8
  - STORE to QuantumTrap nonvolatile elements initiated automatically on power-down (AutoStore) or by user using HSB pin (Hardware STORE) or SPI instruction (Software STORE)
  - RECALL to SRAM initiated on power-up (Power-Up RECALL) or by SPI instruction (Software RECALL)
  - Automatic STORE on power-down with a small capacitor (except for CY14B256Q1)
- High reliability
  - Infinite read, write, and RECALL cycles
  - 1 million STORE cycles to QuantumTrap
  - Data retention: 20 years
- High-speed serial peripheral interface (SPI)
  - 40-MHz clock rate
  - Supports SPI mode 0 (0,0) and mode 3 (1,1)
- Write protection
  - Hardware protection using Write Protect ($\overline{WP}$) pin
  - Software protection using Write Disable instruction
  - Software block protection for 1/4,1/2, or entire array
- Low power consumption
  - Single 3 V +20%, –10% operation
  - Average active current of 10 mA at 40-MHz operation
- Industry standard configurations
  - Industrial temperature
  - CY14B256Q1 has identical pin configuration to industry standard 8-pin NV memory
  - 8-pin dual flat no-lead (DFN) package and 16-pin small outline integrated circuit (SOIC) package
  - Restriction of hazardous substances (RoHS) compliant

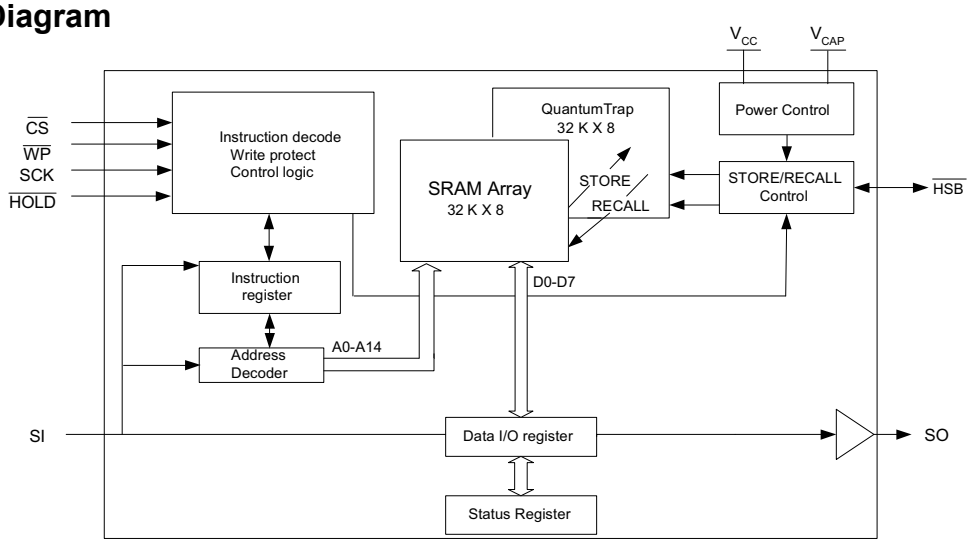
Functional Overview

The Cypress CY14B256Q1/CY14B256Q2/CY14B256Q3 combines a 256-Kbit nvSRAM[1] with a nonvolatile element in each memory cell with serial SPI interface. The memory is organized as 32 K words of 8 bits each. The embedded nonvolatile elements incorporate the QuantumTrap technology, creating the world's most reliable nonvolatile memory. The SRAM provides infinite read and write cycles, while the QuantumTrap cell provides highly reliable nonvolatile storage of data. Data transfers from SRAM to the nonvolatile elements (STORE operation) takes place automatically at power-down (except for CY14B256Q1). On power-up, data is restored to the SRAM from the nonvolatile memory (RECALL operation). The STORE and RECALL operations can also be initiated by the user through SPI instruction.

Configuration

Feature	CY14B256Q1	CY14B256Q2	CY14B256Q3
AutoStore	No	Yes	Yes
Software STORE	Yes	Yes	Yes
Hardware STORE	No	No	Yes

Logic Block Diagram



Note
1. This device will be referred to as nvSRAM throughout the document.

Contents

Device Operation

CY14B256Q1/CY14B256Q2/CY14B256Q3 is a 256-Kbit nvSRAM memory with a nonvolatile element in each memory cell. All the reads and writes to nvSRAM happen to the SRAM which gives nvSRAM the unique capability to handle infinite writes to the memory. The data in SRAM is secured by a STORE sequence that transfers the data in parallel to the nonvolatile QuantumTrap cells. A small capacitor (V_{CAP}) is used to AutoStore the SRAM data in nonvolatile cells when power goes down providing power-down data security. The QuantumTrap nonvolatile elements built in the reliable SONOS technology make nvSRAM the ideal choice for secure data storage.

The 256-Kbit memory array is organized as 32 K words × 8 bits. The memory is accessed through a standard SPI interface that enables very high clock speeds up to 40 MHz with zero cycle delay read and write cycles. This device supports SPI modes 0 and 3 (CPOL, CPHA = 0, 0 and 1, 1) and operates as SPI slave. The device is enabled using the chip select ($\overline{CS}$) pin and accessed through serial input (SI), serial output (SO), and serial clock (SCK) pins.

This device provides the feature for hardware and software write protection through the $\overline{WP}$ pin and WRDI instruction respectively along with mechanisms for block write protection (one quarter, one half, or full array) using BP0 and BP1 pins in the Status Register. Further, the HOLD pin is used to suspend any serial communication without resetting the serial sequence.

CY14B256Q1/CY14B256Q2/CY14B256Q3 uses the standard SPI opcodes for memory access. In addition to the general SPI instructions for read and write, it provides four special instructions which enable access to four nvSRAM specific functions: STORE, RECALL, AutoStore Disable (ASDISB), and AutoStore Enable (ASENB).

The major benefit of nvSRAM over serial EEPROMs is that all reads and writes to nvSRAM are performed at the speed of SPI bus with zero cycle delay. Therefore, no wait time is required after any of the memory accesses. The STORE and RECALL operations need finite time to complete and all memory accesses are inhibited during this time. While a STORE or RECALL operation is in progress, the busy status of the device is indicated by the Hardware STORE Busy ($\overline{HSB}$) pin and also reflected on the $\overline{RDY}$ bit of the Status Register.

The device is available in three different pin configurations that enable the user to choose a part which fits in best in their application. The feature summary is given in Table 1.

Table 1. Feature Summary

Feature	CY14B256Q1	CY14B256Q2	CY14B256Q3
$\overline{WP}$	Yes	No	Yes
V_{CAP}	No	Yes	Yes
$\overline{HSB}$	No	No	Yes
AutoStore	No	Yes	Yes
Power-Up RECALL	Yes	Yes	Yes
Hardware STORE	No	No	Yes
Software STORE	Yes	Yes	Yes
Software RECALL	Yes	Yes	Yes

SRAM Write

All writes to nvSRAM are carried out on the SRAM and do not use up any endurance cycles of the nonvolatile memory. This enables user to perform infinite write operations. A write cycle is performed through the WRITE instruction. The WRITE instruction is issued through the SI pin of the nvSRAM and consists of the WRITE opcode, two bytes of address, and one byte of data. Write to nvSRAM is done at SPI bus speed with zero cycle delay.

The device allows burst mode writes to be performed through SPI. This enables write operations on consecutive addresses without issuing a new WRITE instruction. When the last address in memory is reached in burst mode, the address rolls over to 0x0000 and the device continues to write.

The SPI write cycle sequence is defined in the Memory Access section of SPI Protocol Description.

SRAM Read

A read cycle is performed at the SPI bus speed and the data is read out with zero cycle delay after the READ instruction is executed. The READ instruction is issued through the SI pin of the nvSRAM and consists of the READ opcode and two bytes of address. The data is read out on the SO pin.

This device allows burst mode reads to be performed through SPI. This enables reads on consecutive addresses without issuing a new READ instruction. When the last address in memory is reached in burst mode read, the address rolls over to 0x0000 and the device continues to read.

The SPI read cycle sequence is defined explicitly in the Memory Access section of SPI Protocol Description.

STORE Operation

STORE operation transfers the data from the SRAM to the nonvolatile QuantumTrap cells. The device STOREs data to the nonvolatile cells using one of the three STORE operations: AutoStore, activated on device power-down; Software STORE, activated by a STORE instruction; and Hardware STORE, activated by the HSB. During the STORE cycle, an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. After a STORE cycle is initiated, read/write to CY14B256Q1/CY14B256Q2/CY14B256Q3 is inhibited until the cycle is completed.

The HSB signal or the RDY bit in the Status Register can be monitored by the system to detect if a STORE or Software RECALL cycle is in progress. The busy status of nvSRAM is indicated by HSB being pulled LOW or RDY bit being set to '1'. To avoid unnecessary nonvolatile STOREs, AutoStore and Hardware STORE operations are ignored unless at least one write operation has taken place since the most recent STORE or RECALL cycle. However, software initiated STORE cycles are performed regardless of whether a write operation has taken place.

AutoStore Operation

The AutoStore operation is a unique feature of nvSRAM which automatically stores the SRAM data to QuantumTrap cells during power-down. This STORE makes use of an external capacitor (V_{CAP}) and enables the device to safely STORE the data in the nonvolatile memory when power goes down.

During normal operation, the device draws current from V_{CC} to charge the capacitor connected to the V_{CAP} pin. When the voltage on the V_{CC} pin drops below V_{SWITCH} during power-down, the device inhibits all memory accesses to nvSRAM and automatically performs a conditional STORE operation using the charge from the V_{CAP} capacitor. The AutoStore operation is not initiated if no write cycle has been performed since the last RECALL.

Note If a capacitor is not connected to V_{CAP} pin, AutoStore must be disabled by issuing the AutoStore Disable instruction specified in AutoStore Enable (ASENB) instruction on page 13. If AutoStore is enabled without a capacitor on the V_{CAP} pin, the device attempts an AutoStore operation without sufficient charge to complete the STORE. This corrupts the data stored in the nvSRAM and Status Register. To resume normal functionality, the WRSR instruction must be issued to update the nonvolatile bits BP0, BP1 and WPEN in the Status Register.

Figure 1 shows the proper connection of the storage capacitor (V_{CAP}) for AutoStore operation. Refer to DC Electrical Characteristics on page 15 for the size of the V_{CAP}.

Note CY14B256Q1 does not support AutoStore operation. The user must perform Software STORE operation by using the SPI STORE instruction to secure the data.

Software STORE Operation

Software STORE enables the user to trigger a STORE operation through a special SPI instruction. STORE operation is initiated by executing STORE instruction irrespective of whether a write has been performed since the last NV operation.

A STORE cycle takes t_{STORE} time to complete, during which all the memory accesses to nvSRAM are inhibited. The RDY bit of the Status Register or the HSB pin may be polled to find the ready or busy status of the nvSRAM. After the t_{STORE} cycle time is completed, the SRAM is activated again for read and write operations.

Hardware STORE and HSB Pin Operation

The HSB pin in CY14B256Q3 is used to control and acknowledge STORE operations. If no STORE or RECALL is in progress, this pin can be used to request a Hardware STORE cycle. When the HSB pin is driven LOW, nvSRAM conditionally initiates a STORE operation after t_{DELAY} duration. An actual STORE cycle starts only if a write to the SRAM is performed since the last STORE or RECALL cycle. Reads and writes to the memory are inhibited for t_{STORE} duration or as long as HSB pin is LOW.

The HSB pin also acts as an open drain driver (internal 100 kΩ weak pull-up resistor) that is internally driven LOW to indicate a busy condition when the STORE (initiated by any means) is in progress.

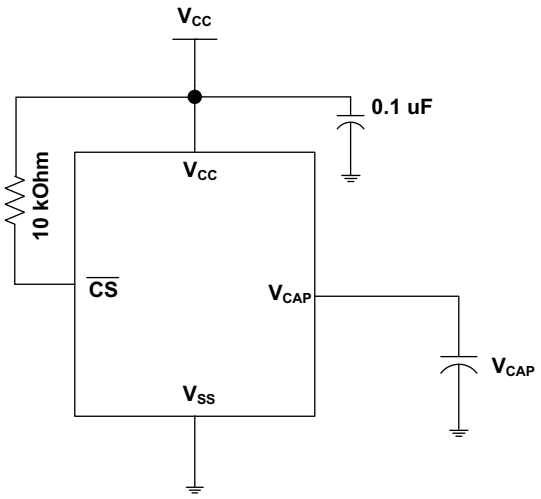
Note After each Hardware and Software STORE operation HSB is driven HIGH for a short time (t_{HHHD}) with standard output high current and then remains HIGH by an internal 100 kΩ pull-up resistor.

Note For successful last data byte STORE, a hardware store should be initiated at least one clock cycle after the last data bit D0 is received.

Upon completion of the STORE operation, the nvSRAM memory access is inhibited for t_{LZHSB} time after HSB pin returns HIGH. The HSB pin must be left unconnected if not used.

Note CY14B256Q1/CY14B256Q2 do not have HSB pin. RDY bit of the SPI Status Register may be probed to determine the ready or busy status of nvSRAM.

Figure 1. AutoStore Mode



RECALL Operation

A RECALL operation transfers the data stored in the nonvolatile QuantumTrap elements to the SRAM. A RECALL may be initiated in two ways: Hardware RECALL, initiated on power-up; and Software RECALL, initiated by a SPI RECALL instruction.

Internally, RECALL is a two step procedure. First, the SRAM data is cleared. Next, the nonvolatile information is transferred into the SRAM cells. All memory accesses are inhibited while a RECALL cycle is in progress. The RECALL operation does not alter the data in the nonvolatile elements.

Hardware RECALL (Power-Up)

During power-up, when V_{CC} crosses V_{SWITCH}, an automatic RECALL sequence is initiated, which transfers the content of nonvolatile memory on to the SRAM. The data would previously have been stored on the nonvolatile memory through a STORE sequence.

A Power-Up RECALL cycle takes t_{FA} time to complete and the memory access is disabled during this time. HSB pin is used to detect the ready status of the device.

Software RECALL

Software RECALL enables the user to initiate a RECALL operation to restore the content of nonvolatile memory on to the SRAM. A Software RECALL is issued by using the SPI instruction for RECALL.

A Software RECALL takes t_{RECALL} time to complete during which all memory accesses to nvSRAM are inhibited. The controller must provide sufficient delay for the RECALL operation to complete before issuing any memory access instructions.

Disabling and Enabling AutoStore

If the application does not require the AutoStore feature, it can be disabled by using the ASDISB instruction. If this is done, the nvSRAM does not perform a STORE operation at power-down.

AutoStore can be re-enabled by using the ASENB instruction. However, these operations are not nonvolatile and if the user needs this setting to survive the power cycle, a STORE operation must be performed following AutoStore Disable or Enable operation.

Note CY14B256Q2/CY14B256Q3 has AutoStore enabled from the factory. In CY14B256Q1, V_{CAP} pin is not present and AutoStore option is not available. The AutoStore Enable and Disable instructions to CY14B256Q1 are ignored.

Note If AutoStore is disabled and V_{CAP} is not required, then the V_{CAP} pin must be left open. The V_{CAP} pin must never be connected to ground. The Power-Up RECALL operation cannot be disabled in any case.

Noise Considerations

Refer to CY application note AN1064.

Serial Peripheral Interface

SPI Overview

The SPI is a four-pin interface with chip select ($\overline{CS}$), serial input (SI), serial output (SO), and serial clock (SCK) pins. CY14B256Q1/CY14B256Q2/CY14B256Q3 provides serial access to nvSRAM through SPI interface. The SPI bus on this device can run at speeds up to 40 MHz.

The SPI is a synchronous serial interface which uses clock and data pins for memory access and supports multiple devices on the data bus. A device on SPI bus is activated using the $\overline{CS}$ pin.

The relationship between chip select, clock, and data is dictated by the SPI mode. This device supports SPI modes 0 and 3. In both these modes, data is clocked into the nvSRAM on the rising edge of SCK starting from the first rising edge after $\overline{CS}$ goes active.

The SPI protocol is controlled by opcodes. These opcodes specify the commands from the bus master to the slave device. After $\overline{CS}$ is activated the first byte transferred from the bus master is the opcode. Following the opcode, any addresses and data are then transferred. The $\overline{CS}$ must go inactive after an operation is complete and before a new opcode can be issued. The commonly used terms used in SPI protocol are as follows:

SPI Master

The SPI master device controls the operations on a SPI bus. A SPI bus may have only one master with one or more slave devices. All the slaves share the same SPI bus lines and the master may select any of the slave devices using the $\overline{CS}$ pin. All the operations must be initiated by the master activating a slave device by pulling the $\overline{CS}$ pin of the slave LOW. The master also generates the SCK and all the data transmission on SI and SO lines are synchronized with this clock.

SPI Slave

The SPI slave device is activated by the master through the chip select line. A slave device gets the SCK as an input from the SPI master and all the communication is synchronized with this clock. SPI slave never initiates a communication on the SPI bus and acts on the instruction from the master.

CY14B256Q1/CY14B256Q2/CY14B256Q3 operates as a SPI slave and may share the SPI bus with other SPI slave devices.

Chip Select ($\overline{CS}$)

For selecting any slave device, the master needs to pull-down the corresponding $\overline{CS}$ pin. Any instruction can be issued to a slave device only while the $\overline{CS}$ pin is LOW. When the device is not selected, data through the SI pin is ignored and the serial output pin (SO) remains in a high-impedance state.

Note A new instruction must begin with the falling edge of $\overline{CS}$. Therefore, only one opcode can be issued for each active chip select cycle.

Serial Clock (SCK)

Serial clock is generated by the SPI master and the communication is synchronized with this clock after $\overline{CS}$ goes LOW.

CY14B256Q1/CY14B256Q2/CY14B256Q3 enables SPI modes 0 and 3 for data communication. In both these modes, the inputs are latched by the slave device on the rising edge of SCK and outputs are issued on the falling edge. Therefore, the first rising edge of SCK signifies the arrival of the first bit (MSB) of SPI instruction on the SI pin. Further, all data inputs and outputs are synchronized with SCK.

Data Transmission - SI and SO

SPI data bus consists of two lines, SI and SO, for serial data communication. The SI is also referred to as Master Out Slave In (MOSI) and SO is referred to as Master In Slave Out (MISO). The master issues instructions to the slave through the SI pin, while the slave responds through the SO pin. Multiple slave devices may share the SI and SO lines as described earlier.

CY14B256Q1/CY14B256Q2/CY14B256Q3 has two separate pins for SI and SO, which can be connected with the master as shown in Figure 2 on page 6.

Most Significant Bit (MSB)

The SPI protocol requires that the first bit to be transmitted is the most significant bit (MSB). This is valid for both address and data transmission.

The 256-Kbit serial nvSRAM requires a 2-byte address for any read or write operation. However, since the address is only 15-bits, it implies that the first MSB that is fed in is ignored by the device. Although this bit is 'don't care', Cypress recommends that this bit is treated as 0 to enable seamless transition to higher memory densities.

Serial Opcode

After the slave device is selected with $\overline{CS}$ going LOW, the first byte received is treated as the opcode for the intended operation. CY14B256Q1/CY14B256Q2/CY14B256Q3 uses the standard opcodes for memory accesses. In addition to the memory accesses, it provides additional opcodes for the nvSRAM specific functions: STORE, RECALL, AutoStore Enable, and AutoStore Disable. Refer to Table 2 on page 8 for details.

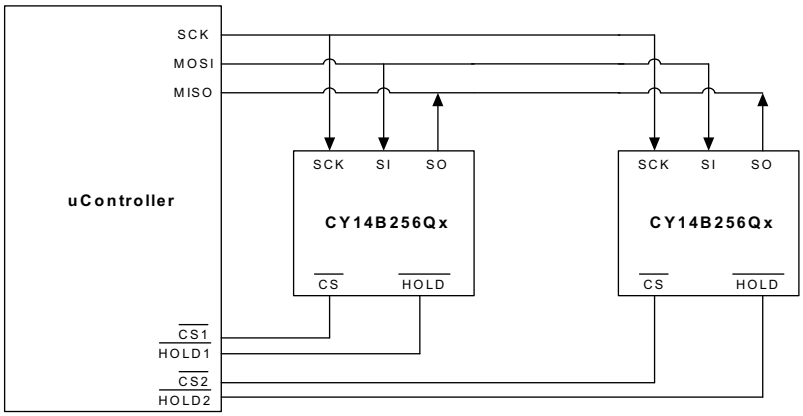
Invalid Opcode

If an invalid opcode is received, the opcode is ignored and the device ignores any additional serial data on the SI pin till the next falling edge of $\overline{CS}$ and the SO pin remains tristated.

Status Register

CY14B256Q1/CY14B256Q2/CY14B256Q3 has an 8-bit Status Register. The bits in the Status Register are used to configure the SPI bus. These bits are described in the Table 4 on page 9.

Figure 2. System Configuration Using SPI nvSRAM



SPI Modes

CY14B256Q1/CY14B256Q2/CY14B256Q3 may be driven by a microcontroller with its SPI peripheral running in either of the following two modes:

- SPI Mode 0 (CPOL=0, CPHA=0)
- SPI Mode 3 (CPOL=1, CPHA=1)

For both these modes, the input data is latched in on the rising edge of SCK starting from the first rising edge after CS goes active. If the clock starts from a HIGH state (in mode 3), the first rising edge after the clock toggles, is considered. The output data is available on the falling edge of SCK.

The two SPI modes are shown in Figure 3 and Figure 4. The status of clock when the bus master is in standby mode and not transferring data is:

- SCK remains at 0 for Mode 0
- SCK remains at 1 for Mode 3

CPOL and CPHA bits must be set in the SPI controller for the either Mode 0 or Mode 3. The device detects the SPI mode from the status of SCK pin when the device is selected by bringing the $\overline{CS}$ pin LOW. If SCK pin is LOW when the device is selected, SPI Mode 0 is assumed and if SCK pin is HIGH, it works in SPI Mode 3.

Figure 3. SPI Mode 0

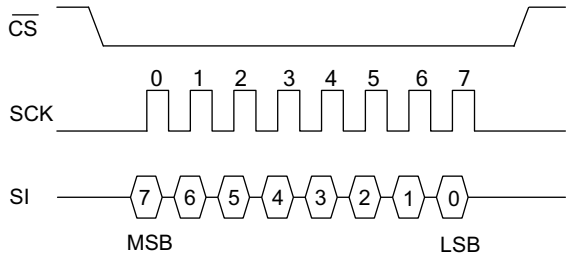
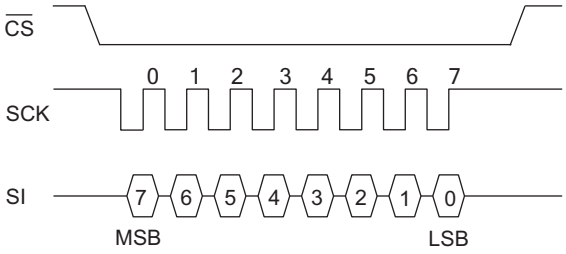


Figure 4. SPI Mode 3



SPI Operating Features

Power-Up

Power-up is defined as the condition when the power supply is turned on and V_{CC} crosses Vswitch voltage. During this time, the $\overline{CS}$ must be allowed to follow the V_{CC} voltage. Therefore, $\overline{CS}$ must be connected to V_{CC} through a suitable pull-up resistor. As a built in safety feature, $\overline{CS}$ is both edge sensitive and level sensitive. After power-up, the device is not selected until a falling edge is detected on $\overline{CS}$. This ensures that $\overline{CS}$ must have been HIGH, before going LOW to start the first operation.

As described earlier, nvSRAM performs a Power-Up RECALL operation after power-up and therefore, all memory accesses are disabled for t_{FA} duration after power-up. The $\overline{HSB}$ pin can be probed to check the Ready or Busy status of nvSRAM after power-up.

Power On Reset

A power on reset (POR) circuit is included to prevent inadvertent writes. At power-up, the device does not respond to any instruction until the V_{CC} reaches the POR threshold voltage (V_{SWITCH}). After V_{CC} transitions the POR threshold, the device is internally reset and performs an Power-Up RECALL operation. During Power-Up RECALL all device accesses are inhibited. The device is in the following state after POR:

- Deselected (after power-up, a falling edge is required on $\overline{CS}$ before any instructions are started).
- Standby power mode
- Not in the HOLD condition
- Status Register state:
  - Write Enable (WEN) bit is reset to '0'.
  - WPEN, BP1, BP0 unchanged from previous STORE operation
  - Don't care bits 4-6 are reset to '0'.

The WPEN, BP1, and BP0 bits of the Status Register are nonvolatile bits and remain unchanged from the previous STORE operation.

Before selecting and issuing instructions to the memory, a valid and stable V_{CC} voltage must be applied. This voltage must remain valid until the end of the instruction transmission.

Power-Down

At power-down (continuous decay of V_{CC}), when V_{CC} drops from the normal operating voltage and below the V_{SWITCH} threshold voltage, the device stops responding to any instruction sent to it. If a write cycle is in progress and the last data bit D0 has been received when the power goes down, it is allowed t_{DELAY} time to complete the write. After this, all memory accesses are inhibited and a conditional AutoStore operation is performed (AutoStore is not performed if no writes have happened since the last RECALL cycle). This feature prevents inadvertent writes to nvSRAM from happening during power-down.

However, to completely avoid the possibility of inadvertent writes during power-down, ensure that the device is deselected and is in standby power mode, and the $\overline{CS}$ follows the voltage applied on V_{CC}.

Active Power and Standby Power Modes

When $\overline{CS}$ is LOW, the device is selected and is in the active power mode. The device consumes I_{CC} current, as specified in DC Electrical Characteristics on page 15. When $\overline{CS}$ is HIGH, the device is deselected and the device goes into the standby power mode if a STORE or RECALL cycle is not in progress. If a STORE or RECALL cycle is in progress, the device goes into the standby power mode after the STORE or RECALL cycle is completed. In the standby power mode, the current drawn by the device drops to I_{SB}.

SPI Functional Description

The CY14B256Q1/CY14B256Q2/CY14B256Q3 uses an 8-bit instruction register. Instructions and their operation codes are listed in Table 2. All instructions, addresses, and data are transferred with the MSB first and start with a HIGH to LOW $\overline{CS}$ transition. There are, in all, 10 SPI instructions that provide access to most of the functions in nvSRAM. Further, the $\overline{WP}$, $\overline{HOLD}$ and $\overline{HSB}$ pins provide additional functionality driven through hardware.

Table 2. Instruction Set

Instruction Category	Instruction Name	Opcode	Operation
Status Register control instructions	WREN	0000 0110	Set write enable latch
	WRDI	0000 0100	Reset write enable latch
	RDSR	0000 0101	Read Status Register
	WRSR	0000 0001	Write Status Register
SRAM Read/Write instructions	READ	0000 0011	Read data from memory array
	WRITE	0000 0010	Write data to memory array
Special NV instructions	STORE	0011 1100	Software STORE
	RECALL	0110 0000	Software RECALL
	ASENB	0101 1001	AutoStore Enable
	ASDISB	0001 1001	AutoStore Disable
Reserved	- Reserved -	0001 1110	

The SPI instructions are divided based on their functionality in the following types:

- Status Register access: RDSR and WRSR instructions
- Write protection functions: WREN and WRDI instructions along with $\overline{WP}$ pin and WEN, BP0, and BP1 bits
- SRAM memory access: READ and WRITE instructions
- nvSRAM special instructions: STORE, RECALL, ASENB, and ASDISB

Status Register

The Status Register bits are listed in Table 3. The Status Register consists of a Ready bit ($\overline{RDY}$) and data protection bits BP1, BP0, WEN, and WPEN. The $\overline{RDY}$ bit can be polled to check the Ready or Busy status while a nvSRAM STORE or Software RECALL cycle is in progress. The Status Register can be modified by WRSR instruction and read by RDSR instruction. However, only the WPEN, BP1, and BP0 bits of the Status Register can be modified by using the WRSR instruction. The WRSR instruction has no effect on WEN and $\overline{RDY}$ bits. The default value shipped from the factory for WEN, BP0, BP1, bits 4-6 and WPEN bits is '0'.

Table 3. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN (0)	X (0)	X (0)	X (0)	BP1 (0)	BP0 (0)	WEN (0)	$\overline{RDY}$

Table 4. Status Register Bit Definition

Bit	Definition	Description
Bit 0 ($\overline{RDY}$)	Ready	Read only bit indicates the ready status of device to perform a memory access. This bit is set to '1' by the device while a STORE or Software RECALL cycle is in progress.
Bit 1 (WEN)	Write Enable	WEN indicates if the device is write enabled. This bit defaults to '0' (disabled) on power-up. WEN = '1' --> Write enabled WEN = '0' --> Write disabled
Bit 2 (BP0)	Block Protect bit '0'	Used for block protection. For details see Table 5 on page 10.
Bit 3 (BP1)	Block Protect bit '1'	Used for block protection. For details see Table 5 on page 10.
Bit 4-6	Don't care	Bits are writable and volatile. On power-up, bits are written with '0'.
Bit 7 (WPEN)	Write Protect Enable bit	Used for enabling the function of Write Protect Pin ($\overline{WP}$). For details see Table 6 on page 11.

Read Status Register (RDSR) Instruction

The Read Status Register (RDSR) instruction provides access to the status register. This instruction is used to probe the write enable status of the device or the Ready status of the device. $\overline{RDY}$ bit is set by the device to '1' whenever a STORE or Software RECALL cycle is in progress. The block protection and WPEN bits indicate the extent of protection employed.

This instruction is issued after the falling edge of $\overline{CS}$ using the opcode for RDSR.

Write Status Register (WRSR) Instruction

The WRSR instruction enables the user to write to the Status Register. However, this instruction cannot be used to modify bit 0 and bit 1 ($\overline{RDY}$ and WEN). The BP0 and BP1 bits can be used to select one of four levels of block protection. Further, WPEN bit must be set to '1' to enable the use of Write Protect ($\overline{WP}$) pin.

WRSR instruction is a write instruction and needs writes to be enabled (WEN bit set to '1') using the WREN instruction before it is issued. The instruction is issued after the falling edge of $\overline{CS}$ using the opcode for WRSR followed by 8 bits of data to be stored in the Status Register. Since only bits 2, 3, and 7 can be modified by WRSR instruction, it is recommended to leave the bits 4-6 as '0' while writing to the Status Register.

Note In CY14B256Q1/CY14B256Q2/CY14B256Q3, the values written to Status Register are saved to nonvolatile memory only after a STORE operation. If AutoStore is disabled (or while using CY14B256Q1), any modifications to the Status Register must be secured by performing a Software STORE operation.

Note CY14B256Q2 does not have $\overline{WP}$ pin. Any modification to bit 7 of the Status Register has no effect on the functionality of CY14B256Q2.

Figure 5. Read Status Register (RDSR) Instruction Timing

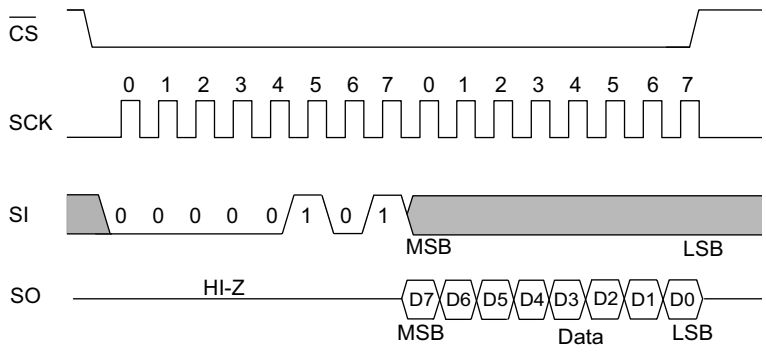
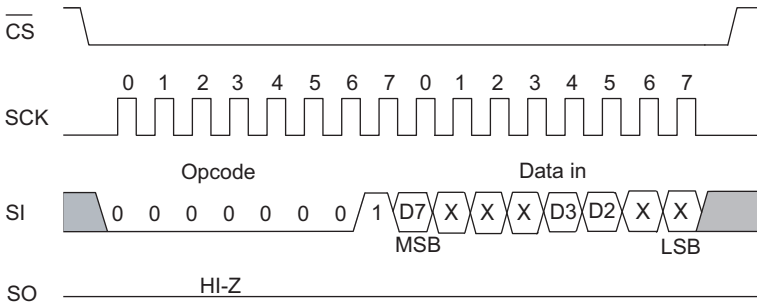


Figure 6. Write Status Register (WRSR) Instruction Timing



Write Protection and Block Protection

CY14B256Q1/CY14B256Q2/CY14B256Q3 provides features for both software and hardware write protection using WRDI instruction and WP. Additionally, this device also provides block protection mechanism through BP0 and BP1 pins of the Status Register.

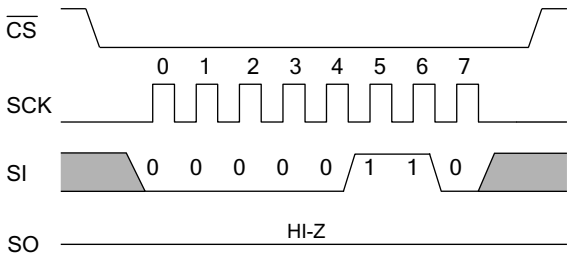
The write enable and disable status of the device is indicated by WEN bit of the Status Register. The write instructions (WRSR and WRITE) and nvSRAM special instruction (STORE, RECALL, ASENB, and ASDISB) need the write to be enabled (WEN bit = 1) before they can be issued.

Write Enable (WREN) Instruction

On power-up, the device is always in the write disable state. The following WRITE, WRSR, or nvSRAM special instruction must therefore be preceded by a Write Enable instruction. If the device is not write enabled (WEN = '0'), it ignores the write instructions and returns to the standby state when CS is brought HIGH. A new CS falling edge is required to re-initiate serial communication. The instruction is issued following the falling edge of CS. When this instruction is used, the WEN bit of Status Register is set to '1'. WEN bit defaults to '0' on power-up.

Note After completion of a write instruction (WRSR or WRITE) or nvSRAM special instruction (STORE, RECALL, ASENB, and ASDISB) instruction, WEN bit is cleared to '0'. This is done to provide protection from any inadvertent writes. Therefore, WREN instruction must be used before a new write instruction is issued.

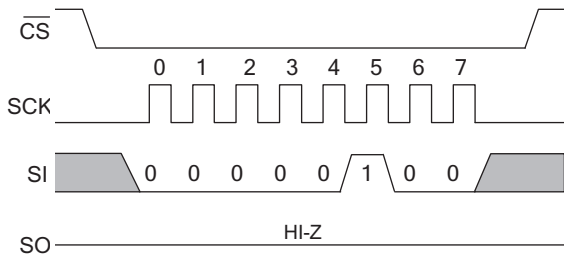
Figure 7. WREN Instruction



Write Disable (WRDI) Instruction

Write Disable instruction disables the write by clearing the WEN bit to '0' in order to protect the device against inadvertent writes. This instruction is issued following the falling edge of CS followed by opcode for WRDI instruction. The WEN bit is cleared on the rising edge of CS following a WRDI instruction.

Figure 8. WRDI Instruction



Block Protection

Block protection is provided using the BP0 and BP1 pins of the Status Register. These bits can be set using WRSR instruction and probed using the RDSR instruction. The nvSRAM is divided into four array segments. One-quarter, one-half, or all of the memory segments can be protected. Any data within the protected segment is read only. Table 5 shows the function of Block Protect bits.

Table 5. Block Write Protect Bits

Level	Status Register Bits		Array Addresses Protected
	BP1	BP0	
0	0	0	None
1 (1/4)	0	1	0x6000-0x7FFF
2 (1/2)	1	0	0x4000-0x7FFF
3 (All)	1	1	0x0000-0x7FFF

Write Protect ($\overline{WP}$) Pin

The write protect pin ($\overline{WP}$) is used to provide hardware write protection. $\overline{WP}$ pin enables all normal read and write operations when held HIGH. When the $\overline{WP}$ pin is brought LOW and WPEN bit is '1', all write operations to the Status Register are inhibited. The hardware write protection function is blocked when the WPEN bit is '0'. This enables the user to install the device in a system with the $\overline{WP}$ pin tied to ground, and still write to the Status Register.

$\overline{WP}$ pin can be used along with WPEN and Block Protect bits (BP1 and BP0) of the Status Register to inhibit writes to memory. When $\overline{WP}$ pin is LOW and WPEN is set to '1', any modifications to the Status Register are disabled. Therefore, the memory is protected by setting the BP0 and BP1 bits and the $\overline{WP}$ pin inhibits any modification of the Status Register bits, providing hardware write protection.

Note $\overline{WP}$ going LOW when $\overline{CS}$ is still LOW has no effect on any of the ongoing write operations to the Status Register. CY14B256Q2 does not have $\overline{WP}$ pin and therefore does not provide hardware write protection.

Table 6 summarizes all the protection features of this device.

Table 6. Write Protection Operation

WPEN	$\overline{WP}$	WEN	Protected Blocks	Unprotected Blocks	Status Register
X	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	LOW	1	Protected	Writable	Protected
1	HIGH	1	Protected	Writable	Writable

Memory Access

All memory accesses are done using the READ and WRITE instructions. These instructions cannot be used while a STORE or RECALL cycle is in progress. A STORE cycle in progress is indicated by the $\overline{RDY}$ bit of the Status Register and the $\overline{HSB}$ pin.

Read Sequence (READ) instruction

The read operations on this device are performed by giving the instruction on the SI pin and reading the output on SO pin. The following sequence needs to be followed for a read operation:

After the $\overline{CS}$ line is pulled LOW to select a device, the read opcode is transmitted through the SI line followed by two bytes of address. The MSB bit (A15) of the address is a "don't care". After the last address bit is transmitted on the SI pin, the data (D7-D0) at the specific address is shifted out on the SO line on the falling edge of SCK starting with D7. Any other data on SI line after the last address bit is ignored.

CY14B256Q1/CY14B256Q2/CY14B256Q3 allows reads to be performed in bursts through SPI which can be used to read consecutive addresses without issuing a new READ instruction. If only one byte is to be read, the $\overline{CS}$ line must be driven HIGH after one byte of data comes out. However, the read sequence may be continued by holding the $\overline{CS}$ line LOW and the address is automatically incremented and data continues to shift out on SO pin. When the last data memory address (0x7FFF) is reached, the address rolls over to 0x0000 and the device continues to read.

Write Sequence (WRITE) instruction

The write operations on this device are performed through the SI pin. To perform a write operation, if the device is write disabled, then the device must first be write enabled through the WREN instruction. When the writes are enabled (WEN = '1'), WRITE instruction is issued after the falling edge of $\overline{CS}$. A WRITE instruction constitutes transmitting the WRITE opcode on SI line followed by 2 bytes of address and the data (D7-D0) which is to be written. The MSB bit (A15) of the address is a "don't care".

CY14B256Q1/CY14B256Q2/CY14B256Q3 enables writes to be performed in bursts through SPI which can be used to write consecutive addresses without issuing a new WRITE instruction. If only one byte is to be written, the $\overline{CS}$ line must be driven HIGH after the D0 (LSB of data) is transmitted. However, if more bytes are to be written, $\overline{CS}$ line must be held LOW and address is incremented automatically. The following bytes on the SI line are treated as data bytes and written in the successive addresses. When the last data memory address (0x7FFF) is reached, the address rolls over to 0x0000 and the device continues to write. The WEN bit is reset to '0' on completion of a WRITE sequence.

Note When a burst write reaches a protected block address, it continues the address increment into the protected space but does not write any data to the protected memory. If the address roll over takes the burst write to unprotected space, it resumes writes. The same operation is true if a burst write is initiated within a write protected block.

Figure 9. Read Instruction Timing

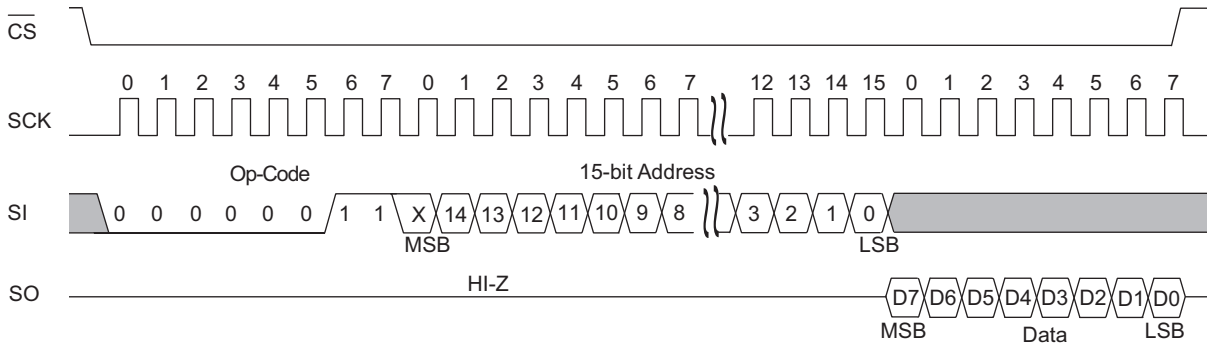


Figure 10. Burst Mode Read Instruction Timing

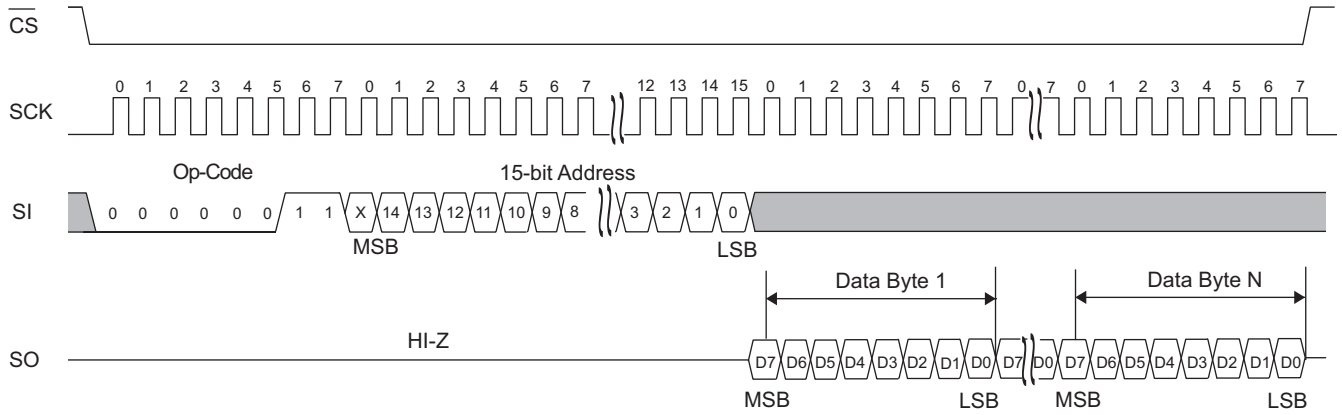


Figure 11. Write Instruction Timing

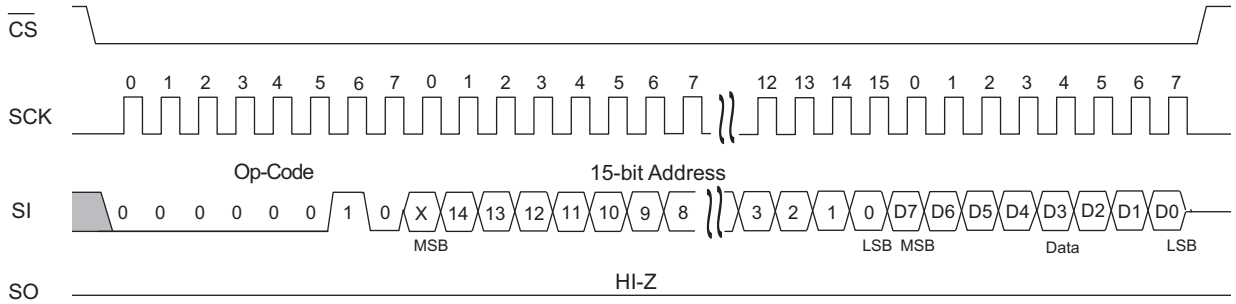
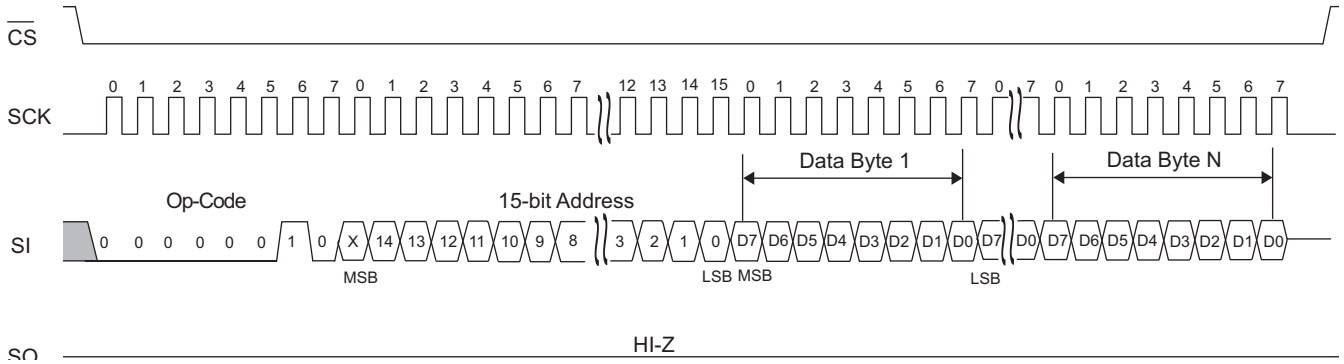


Figure 12. Burst Mode Write Instruction Timing



nvSRAM Special Instructions

CY14B256Q1/CY14B256Q2/CY14B256Q3 provides four special instructions which enables access to the nvSRAM specific functions: STORE, RECALL, ASDISB, and ASENB. Table 7 lists these instructions.

Software STORE (STORE) instruction

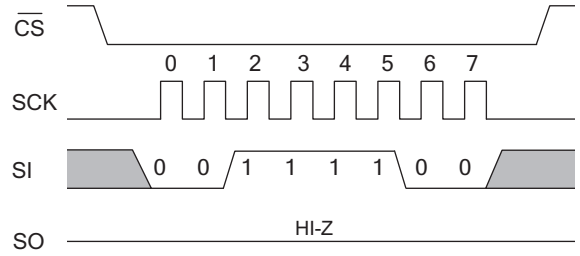
When a STORE instruction is executed, nvSRAM performs a Software STORE operation. The STORE operation is performed irrespective of whether a write has taken place since the last STORE or RECALL operation.

Table 7. nvSRAM Special Instructions

Function Name	Opcode	Operation
STORE	0011 1100	Software STORE
RECALL	0110 0000	Software RECALL
ASENB	0101 1001	AutoStore Enable
ASDISB	0001 1001	AutoStore Disable

To issue this instruction, the device must be write enabled (WEN bit = '1'). The instruction is performed by transmitting the STORE opcode on the SI pin following the falling edge of $\overline{CS}$. The WEN bit is cleared on the positive edge of $\overline{CS}$ following the STORE instruction.

Figure 13. Software STORE Operation

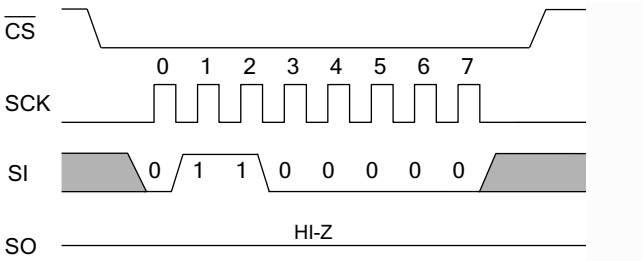


Software RECALL (RECALL) instruction

When a RECALL instruction is executed, nvSRAM performs a Software RECALL operation. To issue this instruction, the device must be write enabled (WEN = '1').

The instruction is performed by transmitting the RECALL opcode on the SI pin following the falling edge of CS. The WEN bit is cleared on the positive edge of CS following the RECALL instruction.

Figure 14. Software RECALL Operation



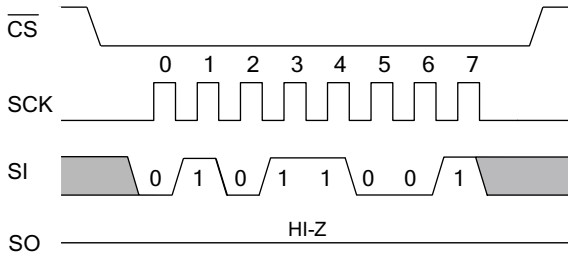
AutoStore Enable (ASENB) instruction

The AutoStore Enable instruction enables the AutoStore on CY14B256Q1. This setting is not nonvolatile and needs to be followed by a STORE sequence if this is desired to survive the power cycle.

To issue this instruction, the device must be write enabled (WEN = '1'). The instruction is performed by transmitting the ASENB opcode on the SI pin following the falling edge of CS. The WEN bit is cleared on the positive edge of CS following the ASENB instruction.

Note If ASDISB and ASENB instructions are executed in CY14B256Q1, the device is busy for the duration of software sequence processing time (t_{SS}). However, ASDISB and ASENB instructions have no effect on CY14B256Q1 as AutoStore is internally disabled.

Figure 15. AutoStore Enable Operation

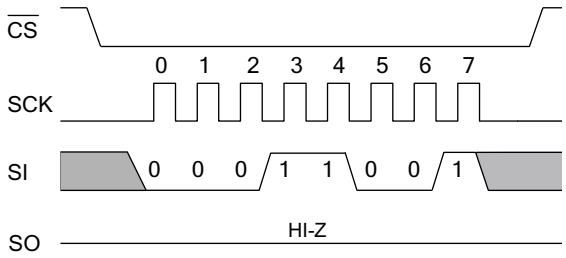


AutoStore Disable (ASDISB) instruction

AutoStore is enabled by default in CY14B256Q2/CY14B256Q3. The ASDISB instruction disables the AutoStore. This setting is not nonvolatile and needs to be followed by a STORE sequence if this is desired to survive the power cycle.

To issue this instruction, the device must be write enabled (WEN = '1'). The instruction is performed by transmitting the ASDISB opcode on the SI pin following the falling edge of CS. The WEN bit is cleared on the positive edge of CS following the ASDISB instruction.

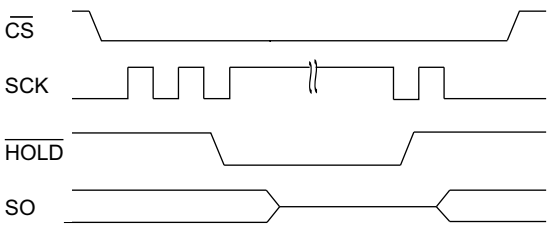
Figure 16. AutoStore Disable Operation



HOLD Pin Operation

The HOLD pin is used to pause the serial communication. When the device is selected and a serial sequence is underway, HOLD is used to pause the serial communication with the master device without resetting the ongoing serial sequence. To pause, the HOLD pin must be brought LOW when the SCK pin is LOW. CS pin must remain LOW along with HOLD pin to pause serial communication. While the device serial communication is paused, inputs to the SI pin are ignored and the SO pin is in the high impedance state. To resume serial communication, the HOLD pin must be brought HIGH when the SCK pin is LOW (SCK may toggle during HOLD).

Figure 17. HOLD Operation



Best Practices

nvSRAM products have been used effectively for over 27 years. While ease-of-use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

- The nonvolatile cells in this nvSRAM product are delivered from Cypress with 0x00 written in all cells. Incoming inspection routines at customer or contract manufacturer's sites sometimes reprogram these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. End product's firmware should not assume an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration, cold or warm boot status, and so on should always program a unique NV pattern (that is, complex 4 byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.
- Power-up boot firmware routines should rewrite the nvSRAM into the desired state (for example, AutoStore enabled). While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently such as program bugs and incoming inspection routines.
- The V_{CAP} value specified in this data sheet includes a minimum and a maximum value size. Best practice is to meet this requirement and not exceed the maximum V_{CAP} value because the nvSRAM internal algorithm calculates V_{CAP} charge and discharge time based on this maximum V_{CAP} value. Customers that want to use a larger V_{CAP} value to make sure there is extra STORE charge and STORE time should discuss their V_{CAP} size selection with Cypress to understand any impact on the V_{CAP} voltage level at the end of a t_{RECALL} period.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Maximum accumulated storage time

At 150 °C ambient temperature..... .... 1000 h

At 85 °C ambient temperature..... ... 20 Years

Ambient temperature with power applied ..... –55 °C to +150 °C

Supply voltage on V_{CC} relative to V_{SS}.....–0.5 V to +4.1 V

DC voltage applied to outputs in high Z state ..... –0.5 V to V_{CC} + 0.5 V

Input voltage ..... –0.5 V to V_{CC} + 0.5 V

Transient voltage (< 20 ns) on any pin to ground potential ..... –2.0 V to V_{CC} + 2.0 V

Package power dissipation capability (T_A = 25 °C) ..... 1.0 W

Surface mount lead soldering temperature (3 seconds) ..... +260 °C

DC output current (1 output at a time, 1 s duration)..... 15 mA

Static discharge voltage..... > 2001 V (per MIL-STD-883, method 3015)

Latch up current..... > 200 mA

Table 8. Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	2.7 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range (V_{CC} = 2.7 V to 3.6 V)

Parameter	Description	Test Conditions	Min	Typ[2]	Max	Unit
V_{CC}	Power supply voltage		2.7	3.0	3.6	V
I_{CC1}	Average V_{cc} current	At f_{SCK} = 40 MHz. Values obtained without output loads (I_{OUT} = 0 mA)	–	–	10	mA
I_{CC2}	Average V_{CC} current during STORE	All inputs don't care, V_{CC} = Max. Average current for duration t_{STORE}	–	–	10	mA
I_{CC4}	Average V_{CAP} current during AutoStore cycle	All inputs don't care. Average current for duration t_{STORE}	–	–	5	mA
I_{SB}	V_{CC} standby current	$\overline{CS} \geq (V_{CC} - 0.2\,V)$. $V_{IN} \leq 0.2\,V$ or $\geq (V_{CC} - 0.2\,V)$. Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz	–	–	5	mA
I_{IX}[3]	Input leakage current (except HSB)	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$	–1	–	+1	µA
	Input leakage current (for $\overline{HSB}$)	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$	–100	–	+1	µA
I_{OZ}	Off state output leakage current	V_{CC} = Max, $V_{SS} \leq V_{OUT} \leq V_{CC}$	–1	–	+1	µA
V_{IH}	Input HIGH voltage		2.0	–	V_{CC} + 0.5	V
V_{IL}	Input LOW voltage		V_{SS} – 0.5	–	0.8	V
V_{OH}	Output HIGH voltage	I_{OUT} = –2 mA	2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OUT} = 4 mA	–	–	0.4	V
V_{CAP}	Storage capacitor	Between V_{CAP} pin and V_{SS}, 5 V rated	61	68	180	µF

Notes
2. Typical values are at 25 °C, V_{CC}= V_{CC} (Typ). Not 100% tested.
3. The $\overline{HSB}$ pin has I_{OUT} = –2 µA for V_{OH} of 2.4 V when both active high and LOW drivers are disabled. When they are enabled standard V_{OH} and V_{OL} are valid. This parameter is characterized but not tested.

Data Retention and Endurance

Parameter	Description	Min	Unit
$DATA_R$	Data retention	20	Years
NV_C	Nonvolatile STORE operations	1,000	K

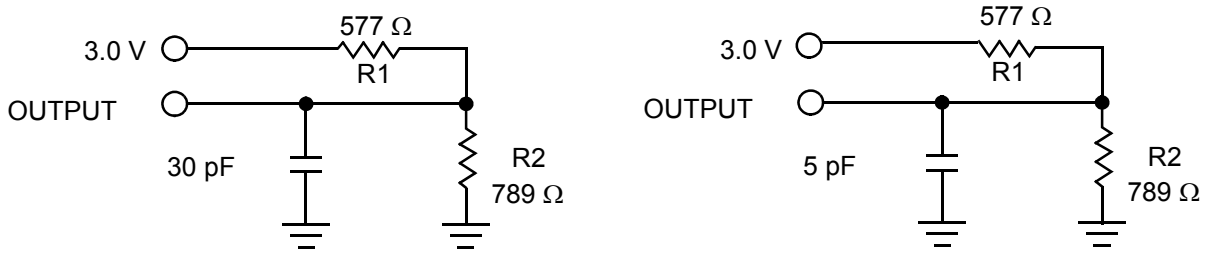
Capacitance

Parameter[4]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = V_{CC} (Typ)	6	pF
C_{OUT}	Output pin capacitance		8	pF

Thermal Resistance

Parameter [4]	Description	Test Conditions	16-SOIC	8-DFN	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	55.17	17.7	°C/W
Θ_{JC}	Thermal resistance (junction to case)		2.64	18.8	°C/W

Figure 18. AC Test Loads and Waveforms



AC Test Conditions

Input pulse levels..... 0 V to 3 V
Input rise and fall times (10% to 90%)..... ≤ 3 ns
Input and output timing reference levels..... 1.5 V

Note
4. These parameters are guaranteed by design and are not tested.

AC Switching Characteristics

Cypress Parameter	Alt. Parameter	Description	40 MHz		Unit
			Min	Max	
f_{SCK}	f_{SCK}	Clock frequency, SCK	–	40	MHz
t_{CL}	t_{WL}	Clock pulse width LOW	11	–	ns
t_{CH}	t_{WH}	Clock pulse width HIGH	11	–	ns
t_{CS}	t_{CE}	CS high time	20	–	ns
t_{CSS}	t_{CES}	CS setup time	10	–	ns
t_{CSH}	t_{CEH}	CS hold time	10	–	ns
t_{SD}	t_{SU}	Data in setup time	5	–	ns
t_{HD}	t_{H}	Data in hold time	5	–	ns
t_{HH}	t_{HD}	HOLD hold time	5	–	ns
t_{SH}	t_{CD}	HOLD setup time	5	–	ns
t_{CO}	t_{V}	Output valid	–	9	ns
t_{HHZ}[5]	t_{HZ}	HOLD to output HIGH-Z	–	15	ns
t_{HLZ}[5]	t_{LZ}	HOLD to output LOW-Z	–	15	ns
t_{OH}	t_{HO}	Output hold time	0	–	ns
t_{HZCS}	t_{DIS}	Output disable time	–	25	ns

Figure 19. Synchronous Data Timing (Mode 0)

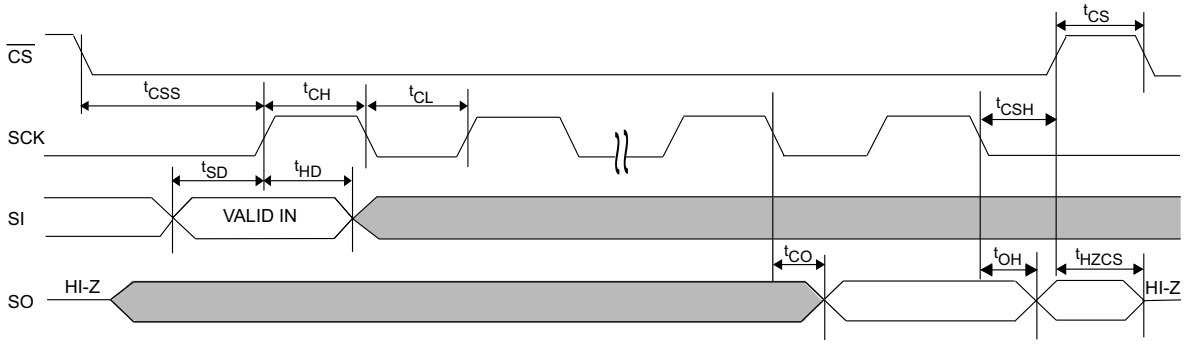
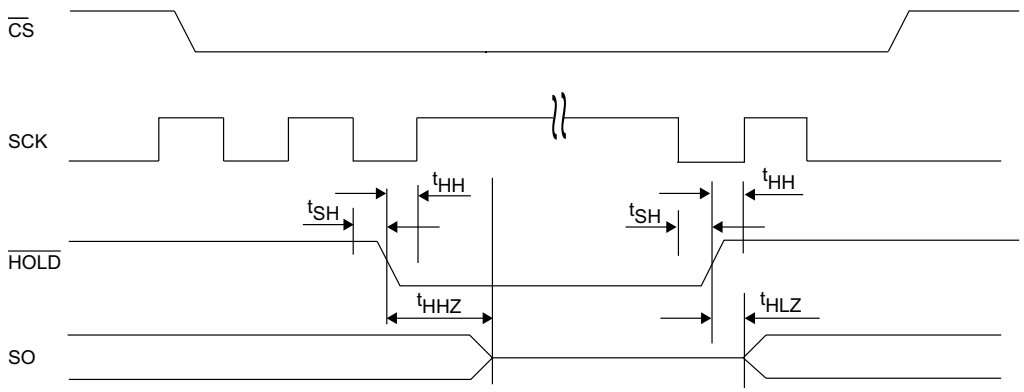


Figure 20. HOLD Timing



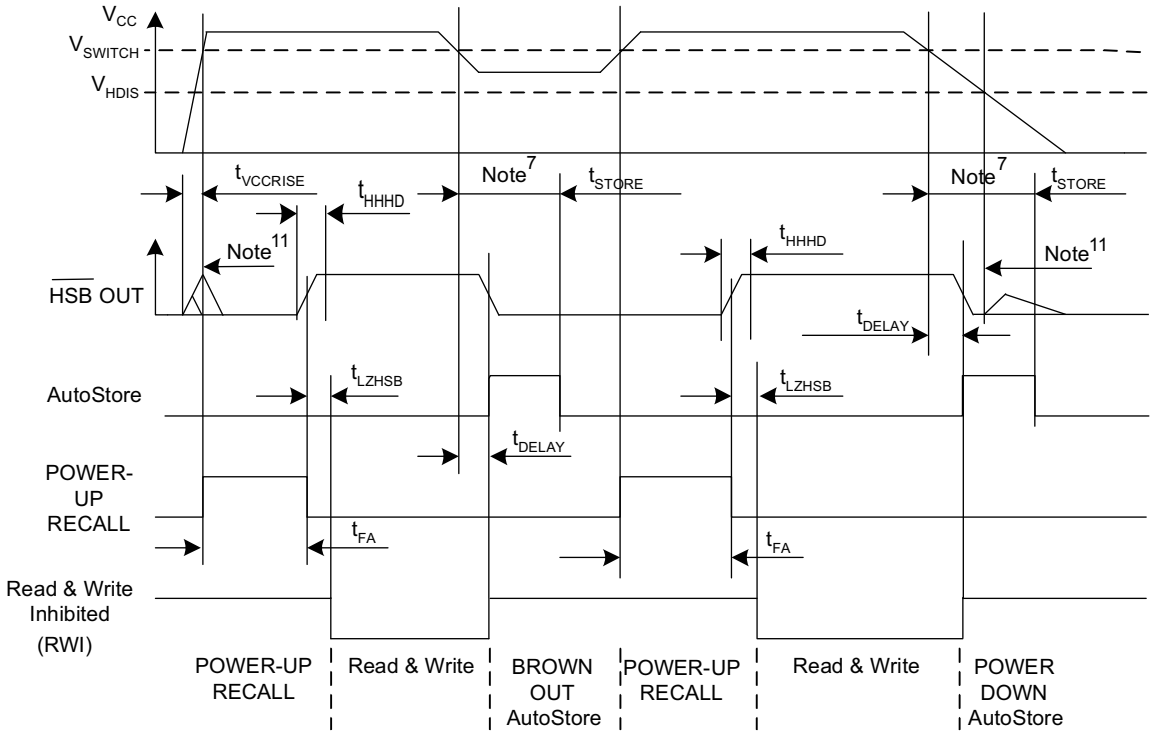
Note
5. These parameters are guaranteed by design and are not tested.

AutoStore or Power-Up RECALL

Parameter	Description	CY14B256Q1/CY14B256Q2/CY14B256Q3		Unit
		Min	Max	
t_{FA} [6]	Power-Up RECALL duration	–	20	ms
t_{STORE} [7]	STORE cycle duration	–	8	ms
t_{DELAY} [8]	Time allowed to complete SRAM write cycle	–	25	ns
V_{SWITCH}	Low voltage trigger level	–	2.65	V
$t_{VCCRISE}$ [9]	V_{CC} rise time	150	–	µs
V_{HDIS} [9]	HSB output disable voltage	–	1.9	V
t_{LZHSB} [9]	HSB high to nvSRAM active time	–	5	µs
t_{HHHD} [9]	HSB high active time	–	500	ns

Switching Waveforms

Figure 21. AutoStore or Power-Up RECALL[10]



Notes
6. t_{FA} starts from the time V_{CC} rises above V_{SWITCH}.
7. If an SRAM write has not taken place since the last nonvolatile cycle, AutoStore or Hardware STORE is not initiated
8. On a Hardware STORE and AutoStore initiation, SRAM write operation continues to be enabled for time t_{DELAY}.
9. These parameters are guaranteed by design and are not tested.
10. Read and write cycles are ignored during STORE, RECALL, and while V_{CC} is below V_{SWITCH}.
11. During power-up and power-down, HSB glitches when HSB pin is pulled up through an external resistor.

Software Controlled STORE and RECALL Cycles

Parameter	Description	CY14B256Q1/CY14B256Q2/CY14B256Q3		Unit
		Min	Max	
t_{RECALL}	RECALL duration	–	200	µs
t_{SS} [12, 13]	Soft sequence processing time	–	100	µs

Figure 22. Software STORE Cycle[13]

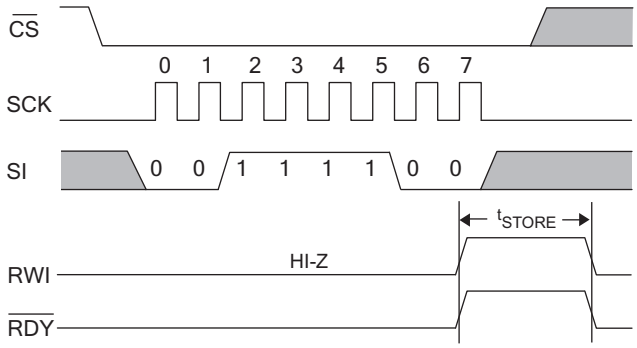


Figure 23. Software RECALL Cycle[13]

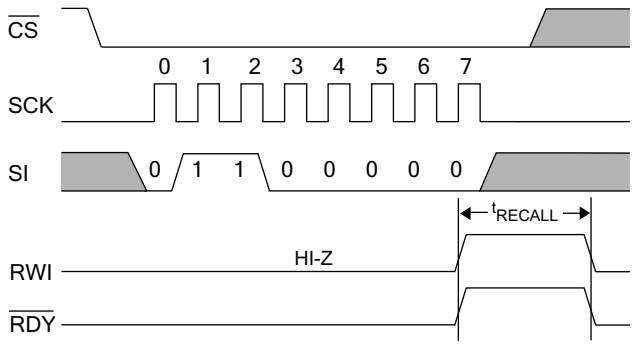


Figure 24. AutoStore Enable Cycle

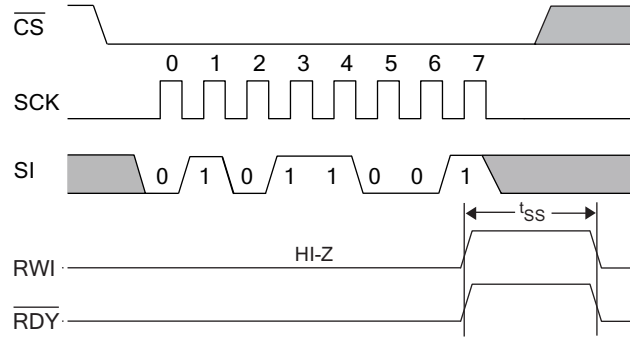
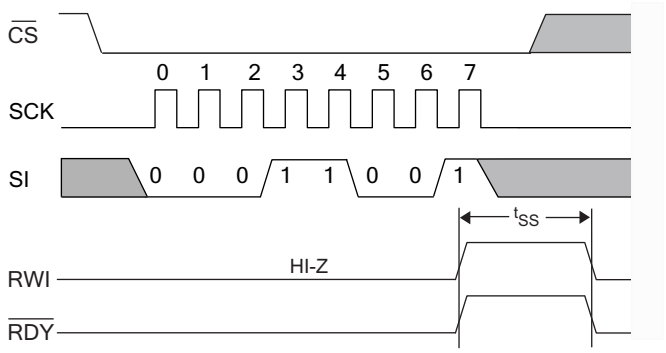


Figure 25. AutoStore Disable Cycle



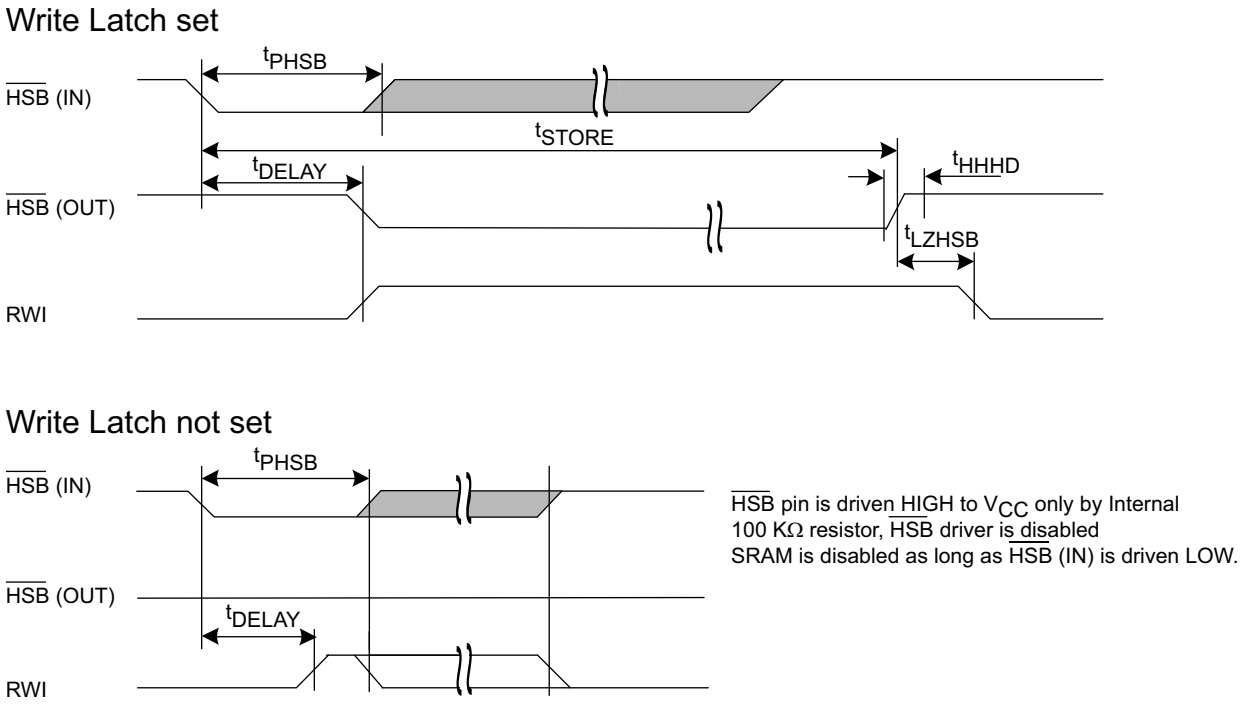
Notes
12. This is the amount of time it takes to take action on a soft sequence command. Vcc power must remain HIGH to effectively register command.
13. Commands such as STORE and RECALL lock out IO until operation is complete which further increases this time. See the specific command.

Hardware STORE Cycle

Parameter	Description	CY14B256Q3		Unit
		Min	Max	
t_{PHSB}	Hardware STORE pulse width	15	–	ns

Switching Waveforms

Figure 26. Hardware STORE Cycle[14]



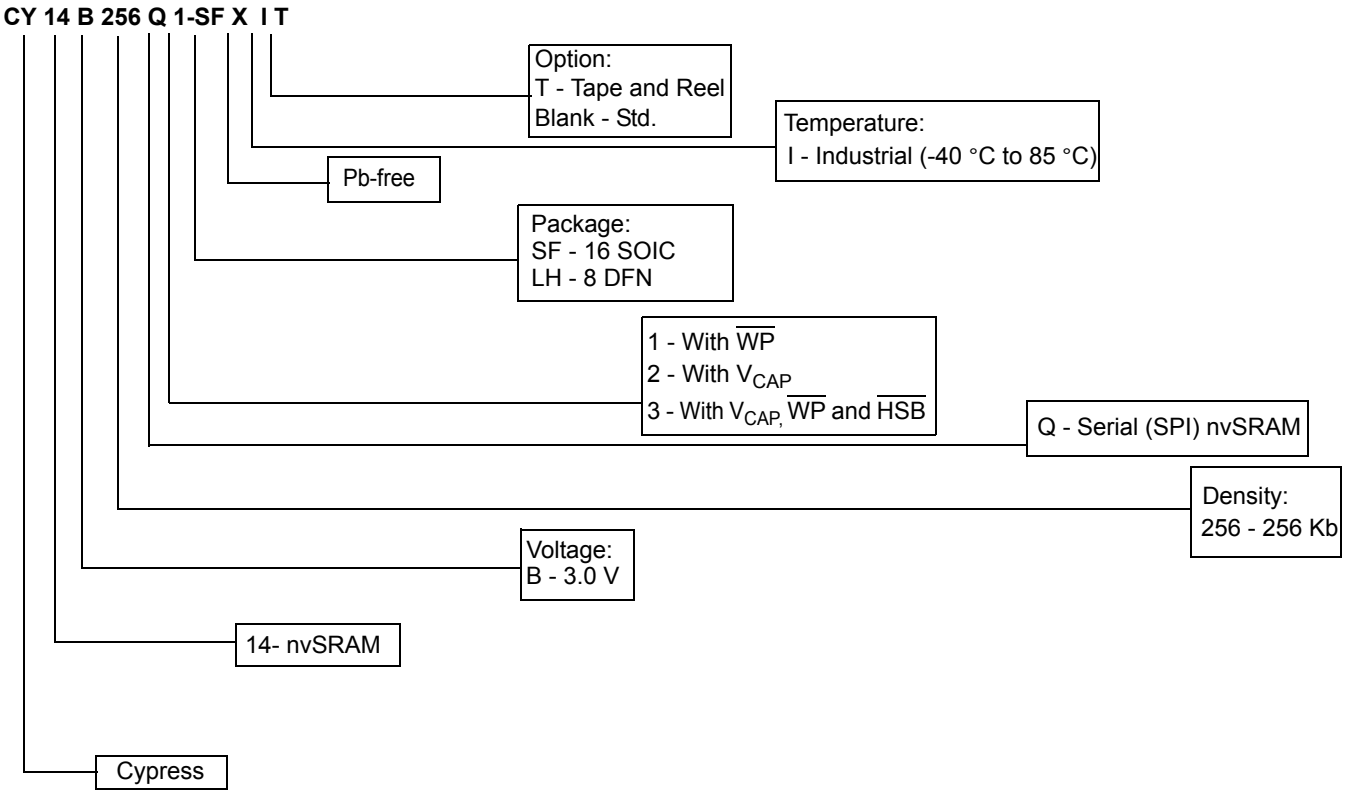
Note
14. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.

Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Range
CY14B256Q1-LHXIT	001-50671	8-pin DFN (with $\overline{WP}$)	Industrial
CY14B256Q1-LHXI	001-50671	8-pin DFN (with $\overline{WP}$)	
CY14B256Q2-LHXIT	001-50671	8-pin DFN (with V_{CAP})	
CY14B256Q2-LHXI	001-50671	8-pin DFN (with V_{CAP})	
CY14B256Q3-SFXIT	51-85022	16-pin SOIC (with V_{CAP}, $\overline{WP}$ and $\overline{HSB}$)	
CY14B256Q3-SFXI	51-85022	16-pin SOIC (with V_{CAP}, $\overline{WP}$ and $\overline{HSB}$)	

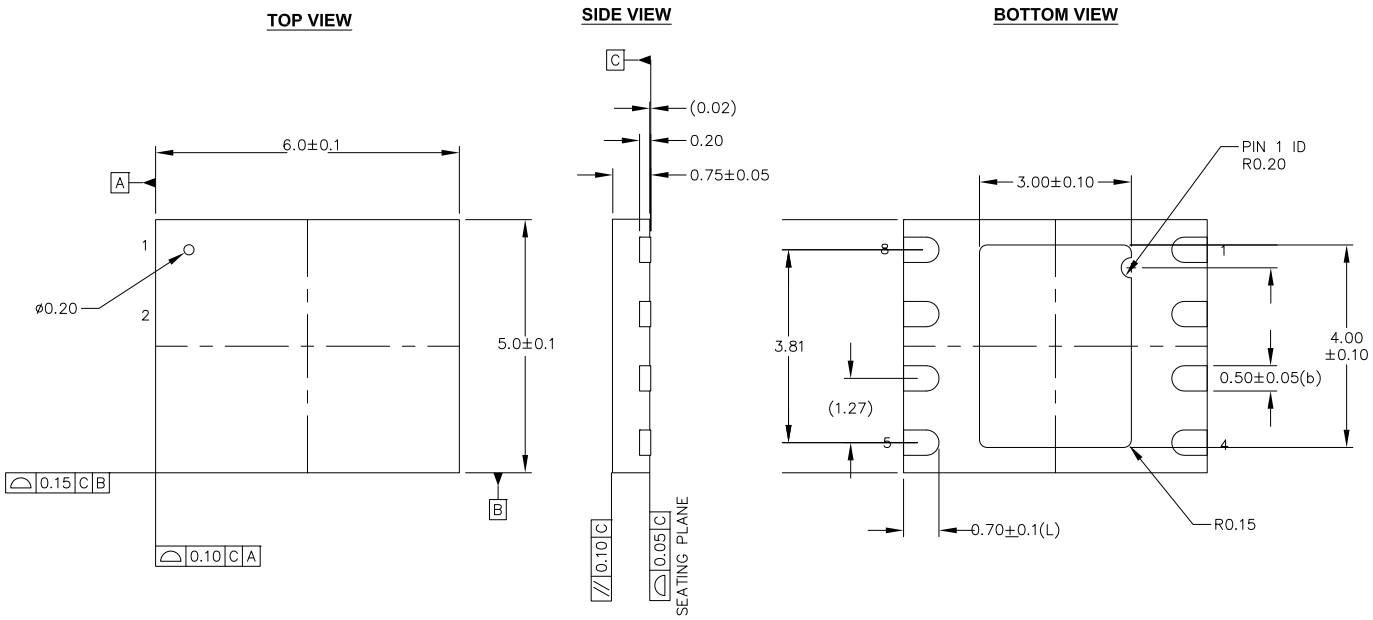
All the above parts are Pb-free.

Ordering Code Definition



Package Diagrams

Figure 27. 8-pin (300 mil) DFN Package



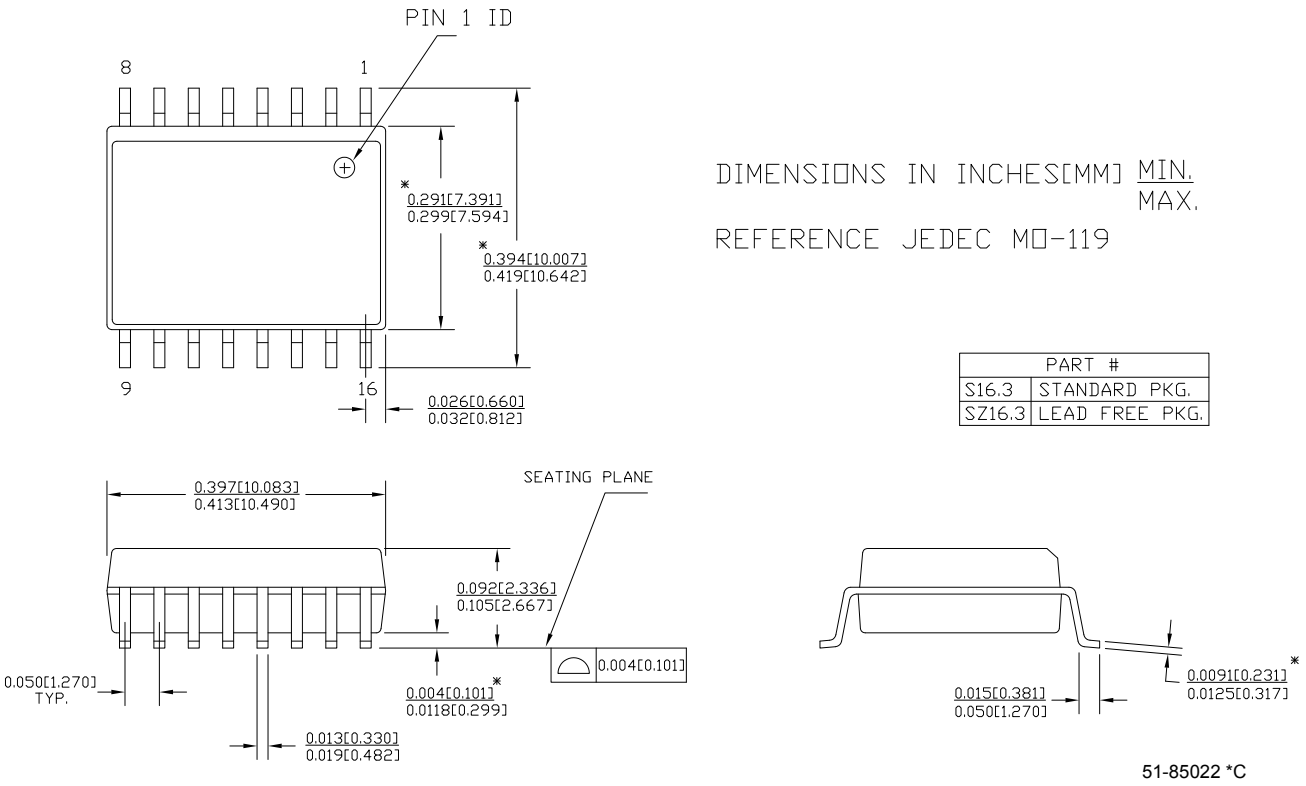
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS
2. PACKAGE WEIGHT: TBD
3. BASED ON REF JEDEC # MO-240 EXCEPT DIMENSIONS (L) and (b)

001-50671 *B

Package Diagrams *(continued)*

Figure 28. 16-pin (300 mil) SOIC Package



Acronyms

Acronym	Description
CMOS	Complementary metal oxide semiconductor
CPHA	Clock phase
CPOL	Clock polarity
DFN	Dual flat no-lead
EEPROM	Electrically erasable programmable read-only memory
EIA	Electronic Industries Alliance
I/O	Input/output
JEDEC	Joint Electron Devices Engineering Council
nvSRAM	nonvolatile static random access memory
RoHS	Restriction of hazardous substances
RWI	Read and write inhibited
SOIC	Small outline integrated circuit
SONOS	Silicon-oxide-nitride-oxide-silicon
SPI	Serial peripheral interface

Document Conventions

Symbol	Unit of Measure
°C	degree Celsius
Hz	Hertz
KΩ	kilo ohm
µA	micro Amperes
µF	micro Farad
µs	micro second
mA	milli Amperes
MHz	Mega Hertz
ns	nano seconds
Ω	ohm
pF	pico Farad
V	Volts
W	Watts

Document History Page

Document Title: CY14B256Q1/CY14B256Q2/CY14B256Q3 256-Kbit (32 K × 8) Serial (SPI) nvSRAM Document Number: 001-53882				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2733272	GVCH/AESA	07/08/09	New data sheet
*A	2758444	GVCH	09/01/09	Moved data sheet status from Preliminary to Final Removed commercial temperature related specs Added thermal resistance values for 16-SOIC and DFN package Added note to Write Sequence (WRITE) description
*B	2839453	GVCH/PYRS	01/06/10	Changed STORE cycles to QuantumTrap from 200 K to 1 Million Added Contents Updated Figure 3
*C	3009761	GVCH	08/17/2010	Changed ground naming convention from GND to V_{SS} Table 1: Added more clarity on HSB pin operation Hardware STORE and HSB Pin Operation: Added more clarity on $\overline{HSB}$ pin operation Updated Power-Down description Power On Reset: Added status of bits 4-6 Table 4: Added definition of bits 4-6 Updated Figure 6 Updated Figure 19, Figure 20, and Figure 21 Updated footnote 14 Added Figure 24 and Figure 25 Removed t_{DHSB} parameter Updated Figure 26 Updated Package Diagrams Added Acronyms and Document Conventions.
*D	3054787	GVCH	10/11/2010	Added watermark as “For Evaluation Samples only. Production will be supported with the next revision silicon in SOIC package.” Updated HOLD Pin Operation, Figure 17 and Figure 20 to indicate that $\overline{CS}$ pin must remain LOW along with HOLD pin to pause serial communication
*E	3143330	GVCH	01/17/2011	Hardware STORE and HSB Pin Operation: Added more clarity on $\overline{HSB}$ pin operation Updated t_{LZHSB} parameter description Fixed typo in Figure 21.

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