

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for W-CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

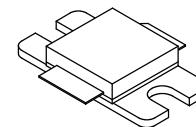
- Typical 2-carrier W-CDMA Performance for $V_{DD} = 28$ Volts, $I_{DQ} = 500$ mA, $f = 2157.5$ MHz, Channel Bandwidth = 3.84 MHz, Adjacent Channels measured over 3.84 MHz Bandwidth at f1 -5 MHz and f2 +5 MHz, Distortion Products measured over a 3.84 MHz Bandwidth at f1 -10 MHz and f2 +10 MHz, Peak/Avg. = 8.3 dB @ 0.01% Probability on CCDF.
- Output Power — 10 Watts Avg.
- Efficiency — 23.5%
- Gain — 15 dB
- IM3 — -37.5 dBc
- ACPR — -41 dBc
- Capable of Handling 5:1 VSWR, @ 28 Vdc, 2140 MHz, 45 Watts CW Output Power

Features

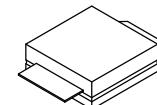
- Internally Matched for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Low Gold Plating Thickness on Leads, 40 μ " Nominal.
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 Inch Reel.

MRF21045LR3
MRF21045LSR3

2110-2170 MHz, 45 W, 28 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465E-04, STYLE 1
NI-400
MRF21045LR3



CASE 465F-04, STYLE 1
NI-400S
MRF21045LSR3

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	105 0.60	W W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Case Operating Temperature	T_C	150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (1)	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.65	$^\circ\text{C}/\text{W}$

Table 3. ESD Protection Characteristics

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M2 (Minimum)

- Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

Table 4. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

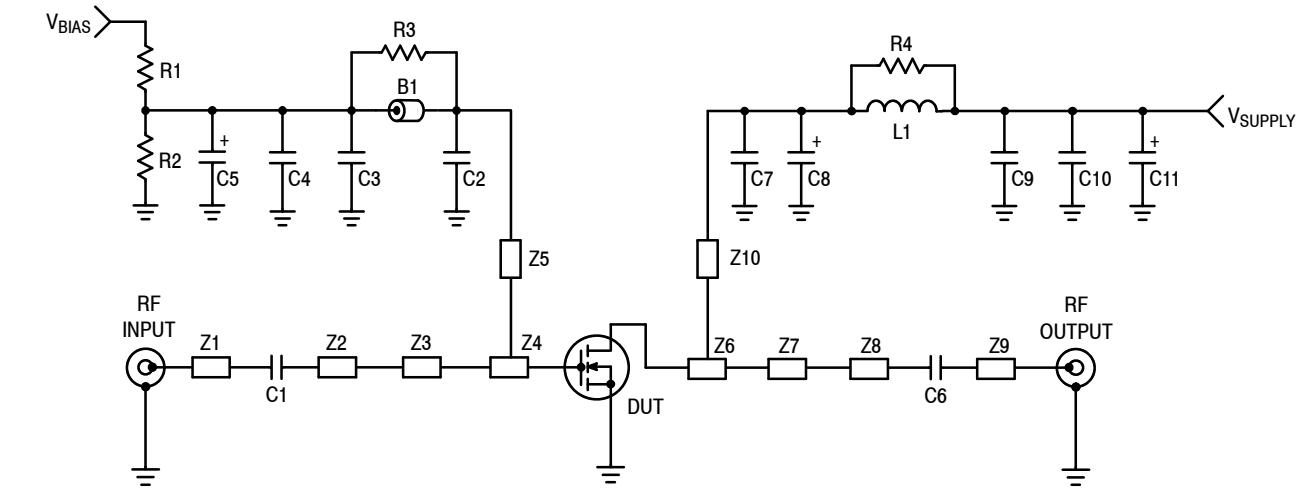
Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-Source Breakdown Voltage ($V_{GS} = 0 \text{ Vdc}$, $I_D = 100 \mu\text{A}$)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 28 \text{ Vdc}$, $V_{GS} = 0 \text{ Vdc}$)	I_{DSS}	—	—	10	μA
Gate-Source Leakage Current ($V_{GS} = 5 \text{ Vdc}$, $V_{DS} = 0 \text{ Vdc}$)	I_{GSS}	—	—	1	μA
On Characteristics (DC)					
Gate Threshold Voltage ($V_{DS} = 10 \text{ Vdc}$, $I_D = 100 \mu\text{A}$)	$V_{GS(\text{th})}$	2	—	4	Vdc
Gate Quiescent Voltage ($V_{DS} = 28 \text{ Vdc}$, $I_D = 500 \text{ mA}$)	$V_{GS(Q)}$	3	3.9	5	Vdc
Drain-Source On-Voltage ($V_{GS} = 10 \text{ Vdc}$, $I_D = 1 \text{ A}$)	$V_{DS(\text{on})}$	—	0.19	0.21	Vdc
Forward Transconductance ($V_{DS} = 10 \text{ Vdc}$, $I_D = 1 \text{ A}$)	g_{fs}	—	3	—	S
Dynamic Characteristics (1)					
Reverse Transfer Capacitance ($V_{DS} = 28 \text{ Vdc}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$)	C_{rss}	—	1.8	—	pF
Functional Tests (In Freescale Test Fixture, 50 ohm system) 2-carrier W-CDMA. Peak/Avg. = 8.3 dB @ 0.01% Probability on CCDF.					
Common-Source Amplifier Power Gain ($V_{DD} = 28 \text{ Vdc}$, $P_{out} = 10 \text{ W Avg.}$, $I_{DQ} = 500 \text{ mA}$, $f_1 = 2157.5 \text{ MHz}$, $f_2 = 2167.5 \text{ MHz}$)	G_{ps}	13.5	15	—	dB
Drain Efficiency ($V_{DD} = 28 \text{ Vdc}$, $P_{out} = 10 \text{ W Avg.}$, $I_{DQ} = 500 \text{ mA}$, $f_1 = 2157.5 \text{ MHz}$, $f_2 = 2167.5 \text{ MHz}$)	η	21	23.5	—	%
Third Order Intermodulation Distortion ($V_{DD} = 28 \text{ Vdc}$, $P_{out} = 10 \text{ W Avg.}$, $I_{DQ} = 500 \text{ mA}$, $f_1 = 2157.5 \text{ MHz}$, $f_2 = 2167.5 \text{ MHz}$; IM3 measured over 3.84 MHz Bandwidth at $f_1 - 10 \text{ MHz}$ and $f_2 + 10 \text{ MHz}$)	IM3	—	-37.5	-35	dBc
Adjacent Channel Power Ratio ($V_{DD} = 28 \text{ Vdc}$, $P_{out} = 10 \text{ W Avg.}$, $I_{DQ} = 500 \text{ mA}$, $f_1 = 2157.5 \text{ MHz}$, $f_2 = 2167.5 \text{ MHz}$; ACPR measured over 3.84 MHz Bandwidth at $f_1 - 5 \text{ MHz}$ and $f_2 + 5 \text{ MHz}$)	ACPR	—	-41	-38	dBc
Input Return Loss ($V_{DD} = 28 \text{ Vdc}$, $P_{out} = 10 \text{ W Avg.}$, $I_{DQ} = 500 \text{ mA}$, $f_1 = 2157.5 \text{ MHz}$, $f_2 = 2167.5 \text{ MHz}$)	IRL	—	-12	-9	dB

1. Part is internally matched both on input and output.

(continued)

Table 4. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (In Freescale Test Fixture, 50 ohm system) — continued					
Two-Tone Common-Source Amplifier Power Gain ($V_{DD} = 28 \text{ Vdc}$, $P_{out} = 45 \text{ W PEP}$, $I_{DQ} = 500 \text{ mA}$, $f_1 = 2110 \text{ MHz}$, $f_2 = 2120 \text{ MHz}$ and $f_1 = 2160 \text{ MHz}$, $f_2 = 2170 \text{ MHz}$)	G_{ps}	—	14.9	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 28 \text{ Vdc}$, $P_{out} = 45 \text{ W PEP}$, $I_{DQ} = 500 \text{ mA}$, $f_1 = 2110 \text{ MHz}$, $f_2 = 2120 \text{ MHz}$ and $f_1 = 2160 \text{ MHz}$, $f_2 = 2170 \text{ MHz}$)	η	—	36	—	%
Intermodulation Distortion ($V_{DD} = 28 \text{ Vdc}$, $P_{out} = 45 \text{ W PEP}$, $I_{DQ} = 500 \text{ mA}$, $f_1 = 2110 \text{ MHz}$, $f_2 = 2120 \text{ MHz}$ and $f_1 = 2160 \text{ MHz}$, $f_2 = 2170 \text{ MHz}$)	IMD	—	-30	—	dBc
Two-Tone Input Return Loss ($V_{DD} = 28 \text{ Vdc}$, $P_{out} = 45 \text{ W PEP}$, $I_{DQ} = 500 \text{ mA}$, $f_1 = 2110 \text{ MHz}$, $f_2 = 2120 \text{ MHz}$ and $f_1 = 2160 \text{ MHz}$, $f_2 = 2170 \text{ MHz}$)	IRL	—	-12	—	dB
P_{out} , 1 dB Compression Point ($V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 500 \text{ mA}$, $f = 2170 \text{ MHz}$)	P_{1dB}	—	50	—	W



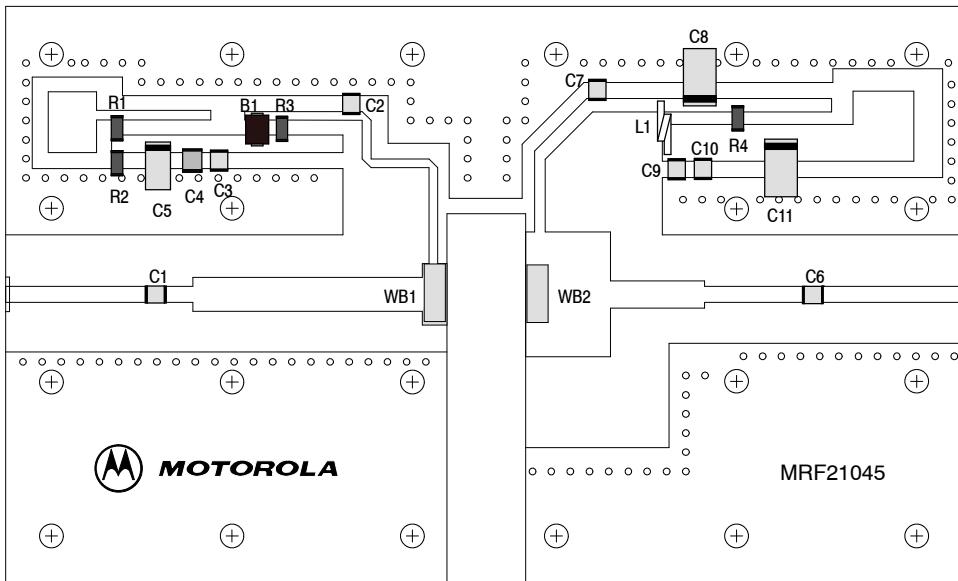
Z1, Z9 0.750" x 0.084" Transmission Line
 Z2 0.160" x 0.084" Transmission Line
 Z3 1.195" x 0.176" Transmission Line
 Z4 0.125" x 0.320" Transmission Line
 Z5 1.100" x 0.045" Transmission Line
 Z6 0.442" x 0.650" Transmission Line
 Z7 0.490" x 0.140" Transmission Line
 Z8 0.540" x 0.084" Transmission Line
 Z10 0.825" x 0.055" Transmission Line

Board 0.030" Glass Teflon®,
 Keene GX-0300-55-22, $\epsilon_r = 2.55$
 PCB Etched Circuit Boards
 MRF21045 Rev. 3, CMR

Figure 1. MRF21045LR3(SR3) Test Circuit Schematic

Table 5. MRF21045LR3(SR3) Component Designations and Values

Designators	Description
B1	Short Ferrite Bead, Fair Rite, #2743019447
C1, C2, C6	43 pF Chip Capacitors, ATC #100B430JCA500X
C7	5.6 pF Chip Capacitor, ATC #100B5R6JCA500X
C3, C9	1000 pF Chip Capacitors, ATC #100B102JCA500X
C4, C10	0.1 μ F Chip Capacitors, Kemet #CDR33BX104AKWS
C5	1.0 μ F Tantalum Chip Capacitor, Kemet #T491C105M050
C8	10 μ F Tantalum Chip Capacitor, Kemet #T495X106K035AS4394
C11	22 μ F Tantalum Chip Capacitor, Kemet #T491X226K035AS4394
L1	1 Turn, #20 AWG, 0.100" ID
N1, N2	Type N Flange Mounts, Omni Spectra #3052-1648-10
R1	1.0 k Ω , 1/8 W Chip Resistor
R2	180 k Ω , 1/8 W Chip Resistor
R3, R4	10 Ω , 1/8 W Chip Resistors



Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 2. MRF21045LR3(SR3) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

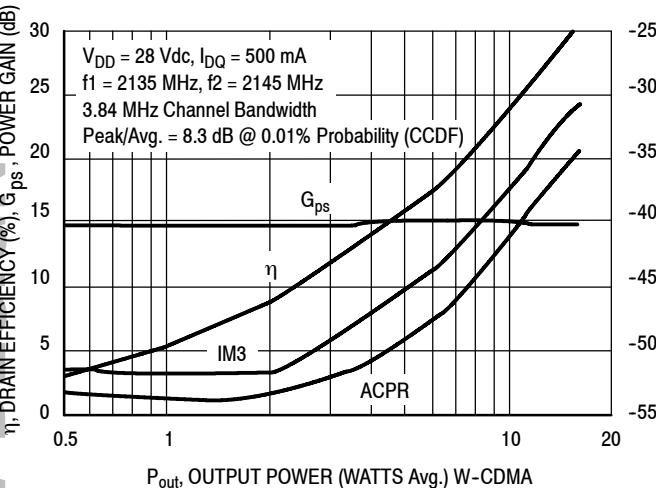


Figure 3. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

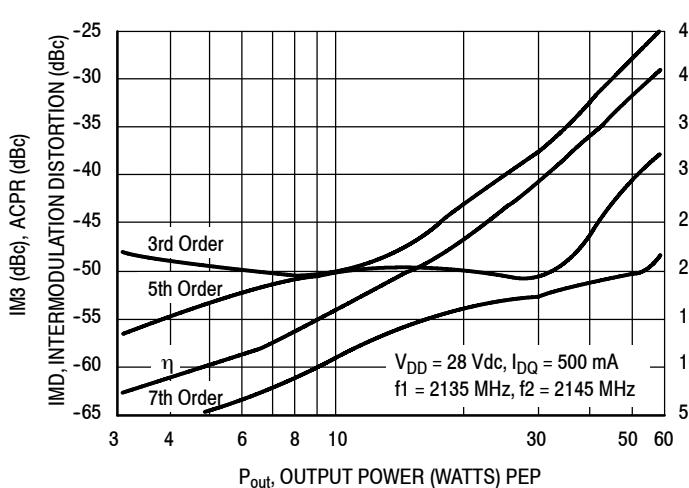


Figure 4. Intermodulation Distortion Products versus Output Power

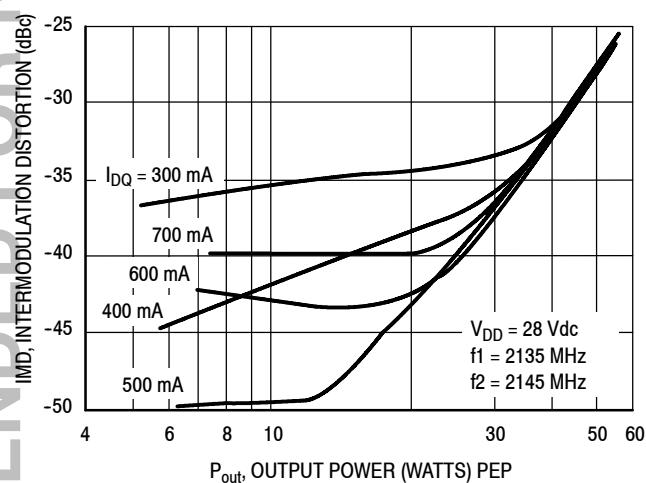


Figure 5. Intermodulation Distortion versus Output Power

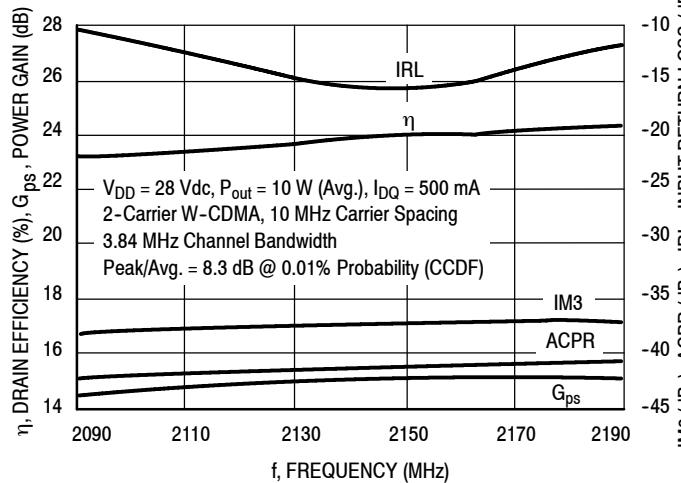


Figure 6. 2-Carrier W-CDMA Broadband Performance

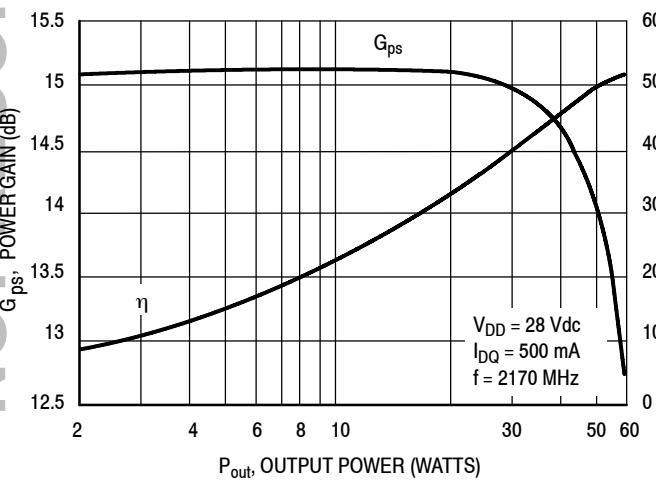


Figure 7. CW Performance

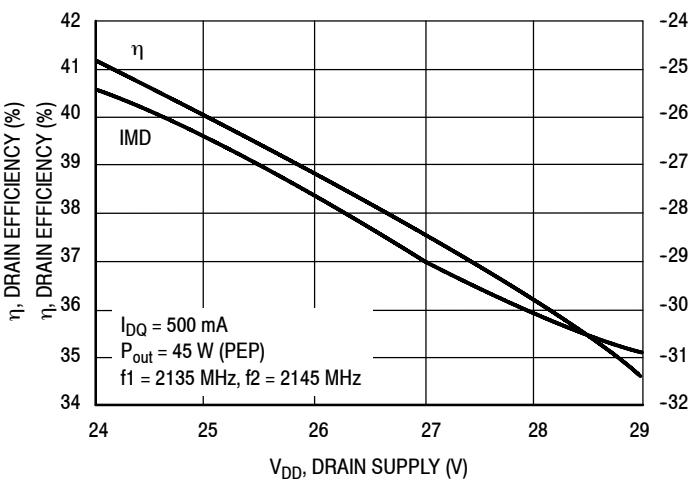
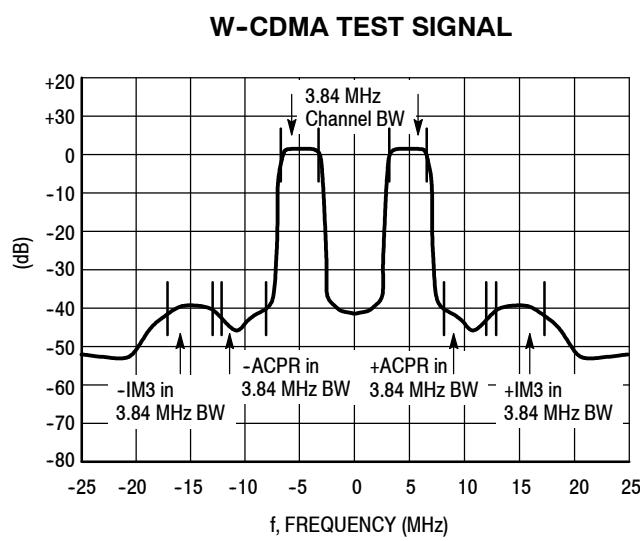
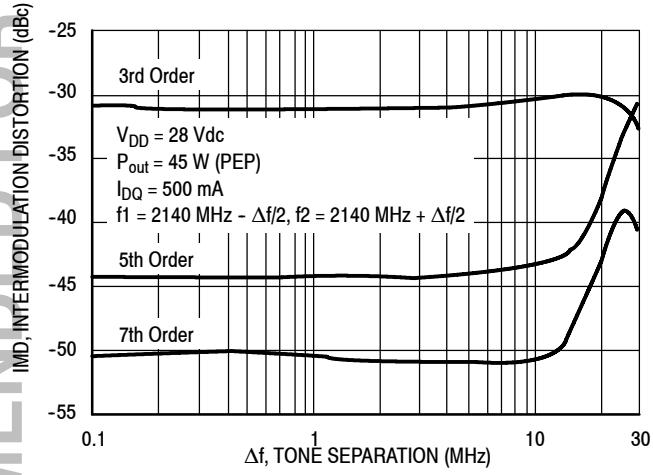
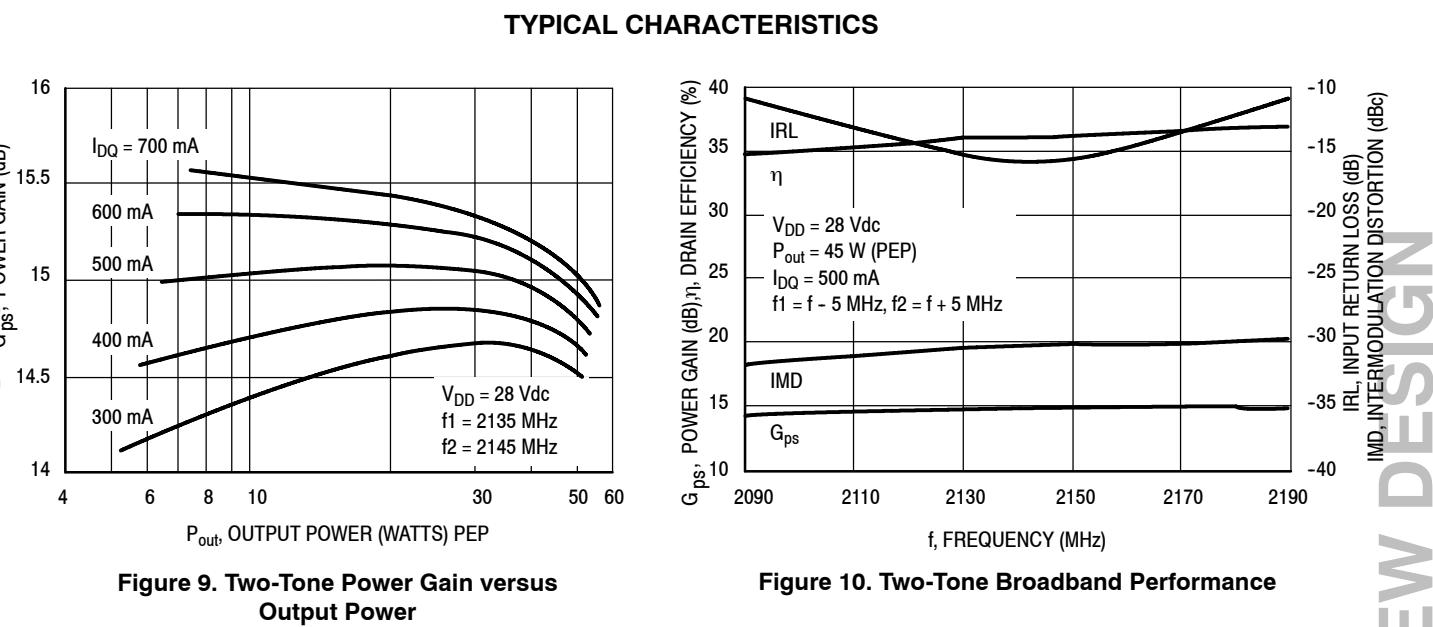
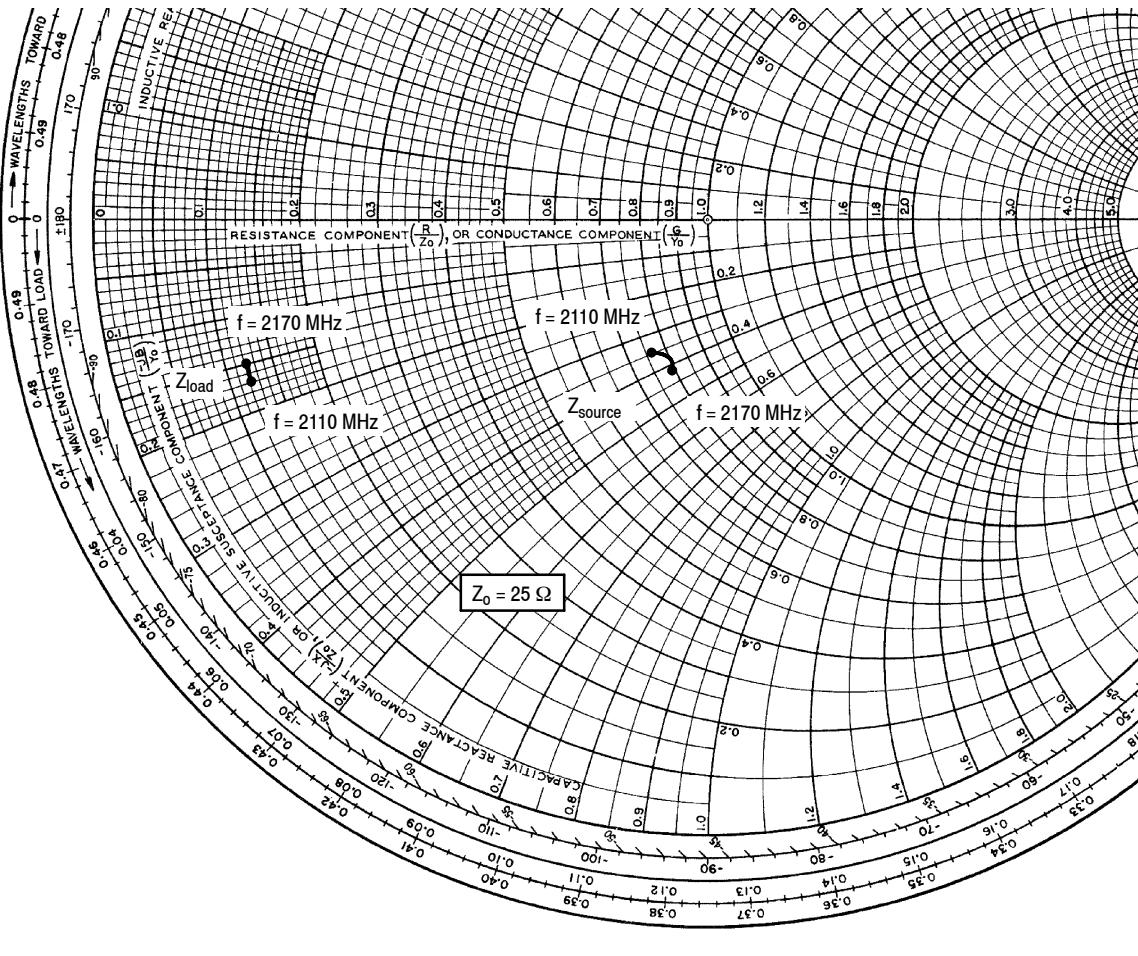


Figure 8. Two-Tone Intermodulation Distortion and Drain Efficiency versus Drain Supply



NOT RECOMMENDED FOR NEW DESIGN

NOT RECOMMENDED FOR NEW DESIGN



$V_{DD} = 28$ Vdc, $I_{DQ} = 500$ mA, $P_{out} = 10$ W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
2110	18.88 - j8.86	3.11 - j4.18
2140	19.80 - j9.93	3.09 - j3.87
2170	19.68 - j10.44	3.12 - j3.72

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

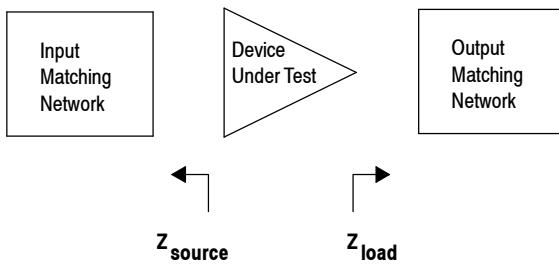
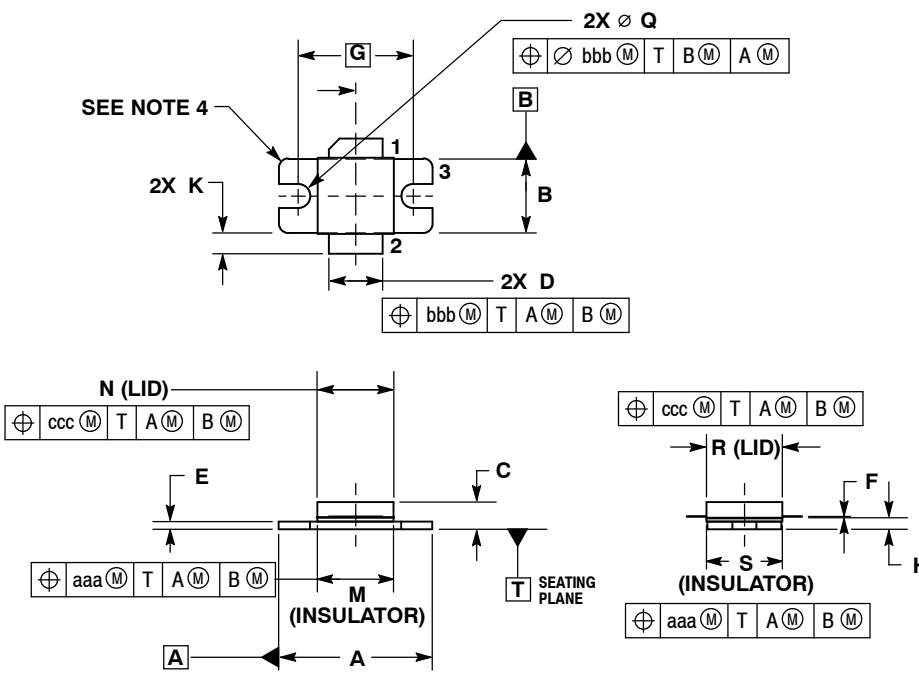


Figure 13. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS



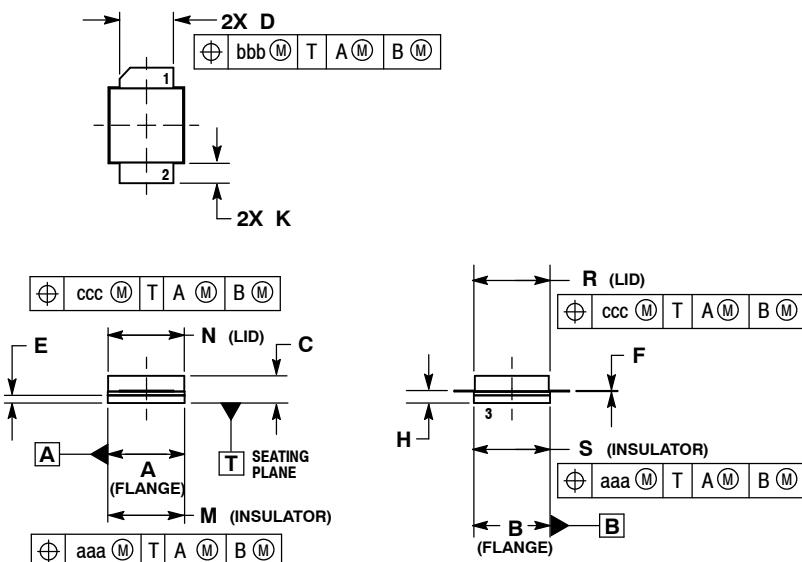
NOTES:

- CONTROLLING DIMENSION: INCH.
- INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
- DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
- INFORMATION ONLY: CORNER BREAK (4X) TO BE .060-.005 (1.52±0.13) RADIUS OR .06±.005 (1.52±0.13) x 45° CHAMFER.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.795	.805	20.19	20.44
B	.380	.390	9.65	9.9
C	.125	.163	3.17	4.14
D	.275	.285	6.98	7.24
E	.035	.045	0.89	1.14
F	.004	.006	0.10	0.15
G	.600	BSC	15.24	BSC
H	.057	.067	1.45	1.7
K	.092	.122	2.33	3.1
M	.395	.405	10	10.3
N	.395	.405	10	10.3
Q	Ø .120	Ø .130	Ø 3.05	Ø 3.3
R	.395	.405	10	10.3
S	.395	.405	10	10.3
aaa	.005	BSC	0.127	BSC
bbb	.010	BSC	0.254	BSC
ccc	.015	BSC	0.381	BSC

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465E-04
ISSUE F
NI-400
MRF21045LR3



NOTES:

- CONTROLLING DIMENSION: INCH.
- INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
- DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.395	.405	10.03	10.29
B	.395	.405	10.03	10.29
C	.125	.163	3.18	4.14
D	.275	.285	6.98	7.24
E	.035	.045	0.89	1.14
F	.004	.006	0.10	0.15
H	.057	.067	1.45	1.70
K	.092	.122	2.34	3.10
M	.395	.405	10.03	10.29
N	.395	.405	10.03	10.29
R	.395	.405	10.03	10.29
S	.395	.405	10.03	10.29
aaa	.005	REF	0.127	REF
bbb	.010	REF	0.254	REF
ccc	.015	REF	0.38	REF

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465F-04
ISSUE E
NI-400S
MRF21045LSR3

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
12	Oct. 2008	<ul style="list-style-type: none">• Data sheet revised to reflect part status change, p. 1, including use of applicable overlay.• Modified data sheet to reflect RF Test Reduction described in Product and Process Change Notification number, PCN12779, p. 1, 2• Added Product Documentation and Revision History, p. 10

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