EN29SL800
8 Megabit (1024K x 8-bit / 512K x 16-bit) Flash Memory Boot Sector Flash Memory, CMOS 1.8 Volt-only

FEATURES

- Single power supply operation
- Full voltage range:1.65-2.2 volt for read and write operations.
- Ideal for battery-powered applications.

- High performance
- Access times as fast as 70 ns

- Low power consumption (typical values at 5 MHz)
- 15 mA typical active read current
- 15 mA typical program/erase current
- 0.2 μA typical standby current

- Flexible Sector Architecture:
- One 16-Kbyte, two 8-Kbyte, one 32-Kbyte, and fifteen 64-Kbyte sectors (byte mode)
- One 8-Kword, two 4-Kword, one 16-Kword and fifteen 32-Kword sectors (word mode)

- Sector protection:
- Hardware locking of sectors to prevent program or erase operations within individual sectors
- Additionally, temporary Sector Unprotect allows code changes in previously locked sectors.

- High performance program/erase speed
- Byte/Word program time: 5μs/7μs typical
- Sector erase time: 500ms typical

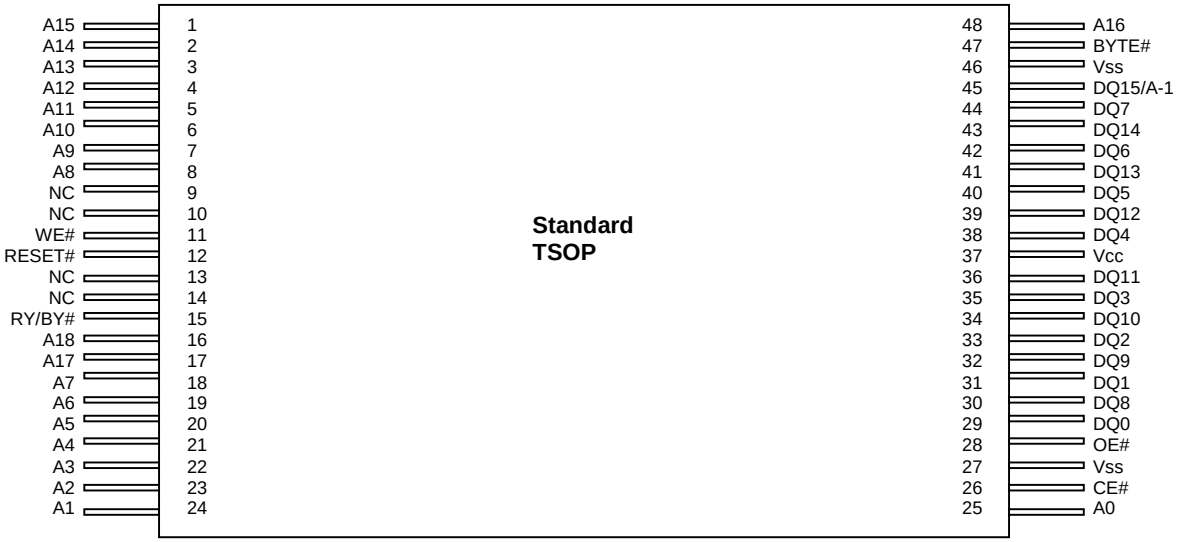
- JEDEC Standard Embedded Erase and Program Algorithms
- JEDEC standard DATA# polling and toggle bits feature
- Single Sector and Chip Erase
- Sector Unprotect Mode
- Erase Suspend / Resume modes: Read or program another Sector during Erase Suspend Mode
- Low Vcc write inhibit ≤ 1.2V
- Minimum 100K endurance cycle
- Package Options
- 48-pin TSOP (Type 1)
- 48-ball 6mm x 8mm FBGA
- 48-ball 5mm x 6mm WFBGA
- 48-ball 5mm x 6mm WLGA
- Commercial and industrial temperature Range

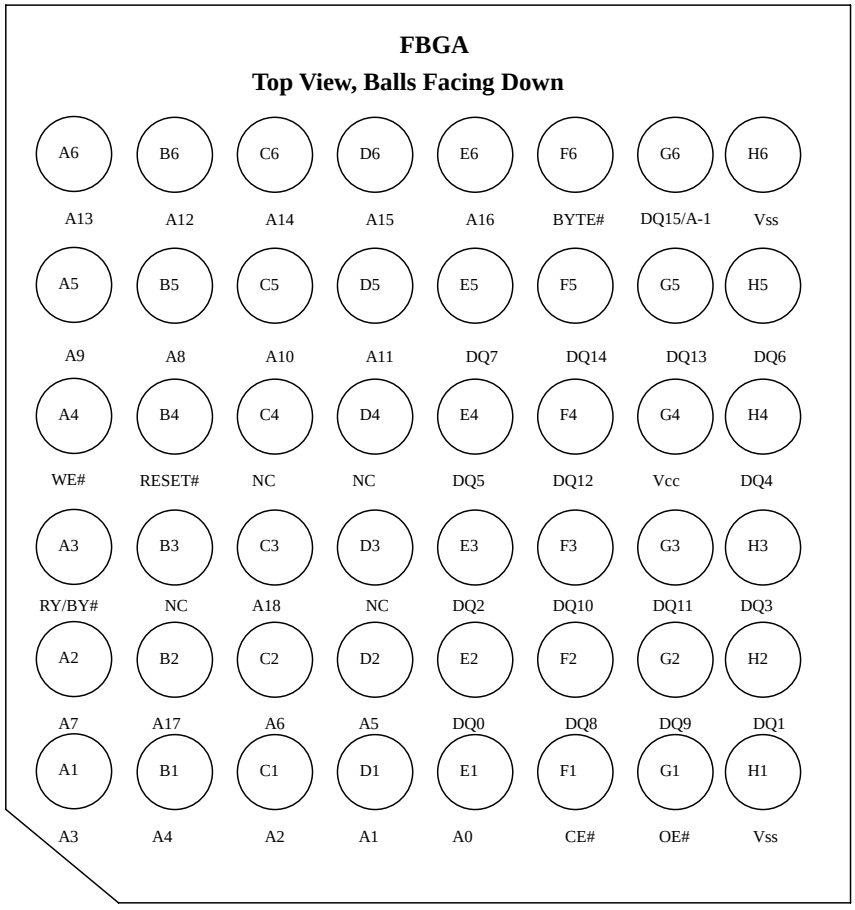
GENERAL DESCRIPTION

The EN29SL800 is an 8-Megabit, electrically erasable, read/write non-volatile flash memory, organized as 1,048,576 bytes or 524,288 words. Any byte can be programmed typically in 5μs. The EN29SL800 features 1.8V voltage read and write operation, with access time as fast as 70ns to eliminate the need for WAIT statements in high-performance microprocessor systems.

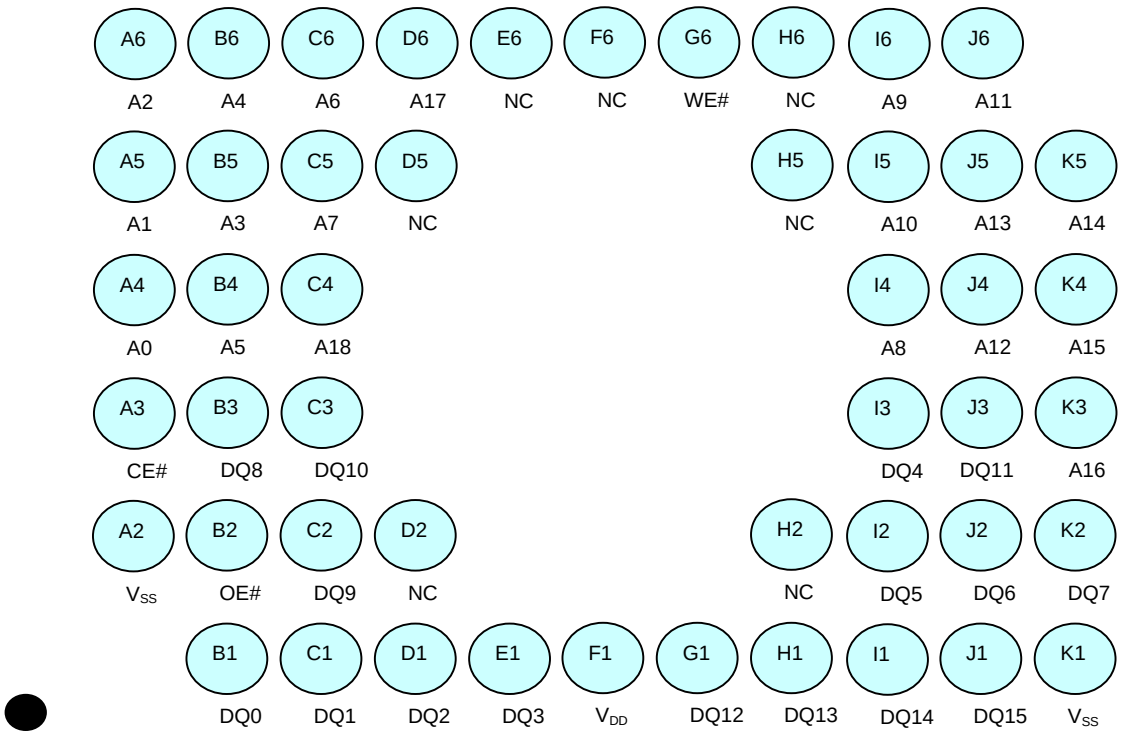
The EN29SL800 has separate Output Enable (OE#), Chip Enable (CE#), and Write Enable (WE#) controls, which eliminate bus contention issues. This device is designed to allow either single Sector or full chip erase operation, where each sector can be individually protected against program/erase operations or temporarily unprotected to erase or program. The device can sustain a minimum of 100K program/erase cycles on each sector.

CONNECTION DIAGRAMS





WFBGA and WLGA
Top View, Balls Facing Down



Notes:

1. Reset#, RY/BY#, Byte# are not available for WFBGA package.
2. It is organized as 512K x 16 (8Mbit)

TABLE 1. PIN DESCRIPTION

Pin Name	Function
A0-A18	Addresses
DQ0-DQ14	15 Data Inputs/Outputs
DQ15 / A-1	DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)
CE#	Chip Enable
OE#	Output Enable
RESET#	Hardware Reset Pin
RY/BY#	Ready/Busy Output
WE#	Write Enable
Vcc	Supply Voltage (1.65-2.2V)
Vss	Ground
NC	Not Connected to anything
BYTE#	Byte/Word Mode

FIGURE 1. LOGIC DIAGRAM

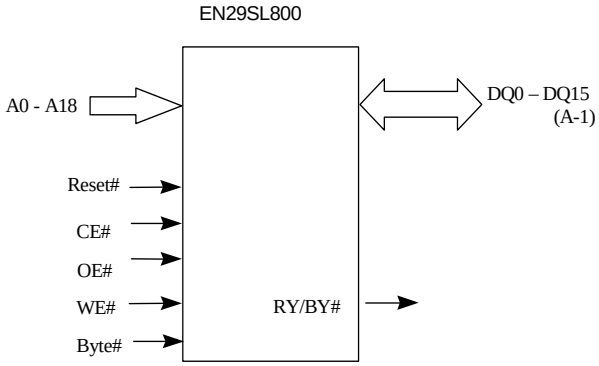


TABLE 2A. TOP BOOT BLOCK SECTOR ARCHITECTURE

Sector	ADDRESS RANGE		SECTOR SIZE (Kbytes / Kwords)	A18	A17	A16	A15	A14	A13	A12
	(X16)	(X8)								
18	7E000h-7FFFFh	FC000h-FFFFFh	16/8	1	1	1	1	1	1	X
17	7D000h-7DFFFh	FA000h-FBFFFh	8/4	1	1	1	1	1	0	1
16	7C000h-7CFFFh	F8000h-F9FFFh	8/4	1	1	1	1	1	0	0
15	78000h-7BFFFh	F0000h – F7FFFh	32/16	1	1	1	1	0	X	X
14	70000h-77FFFh	E0000h - EFFFFh	64/32	1	1	1	0	X	X	X
13	68000h-6FFFFh	D0000h - DFFFFh	64/32	1	1	0	1	X	X	X
12	60000h-67FFFh	C0000h - CFFFFh	64/32	1	1	0	0	X	X	X
11	58000h-5FFFFh	B0000h - BFFFFh	64/32	1	0	1	1	X	X	X
10	50000h-57FFFh	A0000h - AFFFFh	64/32	1	0	1	0	X	X	X
9	48000h-4FFFFh	90000h - 9FFFFh	64/32	1	0	0	1	X	X	X
8	40000h-47FFFh	80000h - 8FFFFh	64/32	1	0	0	0	X	X	X
7	38000h-3FFFFh	70000h - 7FFFFh	64/32	0	1	1	1	X	X	X
6	30000h-37FFFh	60000h - 6FFFFh	64/32	0	1	1	0	X	X	X
5	28000h-2FFFFh	50000h – 5FFFFh	64/32	0	1	0	1	X	X	X
4	20000h-27FFFh	40000h – 4FFFFh	64/32	0	1	0	0	X	X	X
3	18000h-1FFFFh	30000h – 3FFFFh	64/32	0	0	1	1	X	X	X
2	10000h-17FFFh	20000h - 2FFFFh	64/32	0	0	1	0	X	X	X
1	08000h-0FFFFh	10000h - 1FFFFh	64/32	0	0	0	1	X	X	X
0	00000h-07FFFh	00000h - 0FFFFh	64/32	0	0	0	0	X	X	X

TABLE 2B. BOTTOM BOOT BLOCK SECTOR ARCHITECTURE

Sector	ADDRESS RANGE		SECTOR SIZE (Kbytes/ Kwords)	A18	A17	A16	A15	A14	A13	A12
	(X16)	(X8)								
18	78000h-7FFFFh	F0000h – FFFFFh	64/32	1	1	1	1	X	X	X
17	70000h-77FFFh	E0000h – EFFFFh	64/32	1	1	1	0	X	X	X
16	68000h-6FFFFh	D0000h – DFFFFh	64/32	1	1	0	1	X	X	X
15	60000h-67FFFh	C0000h – CFFFFh	64/32	1	1	0	0	X	X	X
14	58000h-5FFFFh	B0000h - BFFFFh	64/32	1	0	1	1	X	X	X
13	50000h-57FFFh	A0000h - AFFFFh	64/32	1	0	1	0	X	X	X
12	48000h-4FFFFh	90000h – 9FFFFh	64/32	1	0	0	1	X	X	X
11	40000h-47FFFh	80000h – 8FFFFh	64/32	1	0	0	0	X	X	X
10	38000h-3FFFFh	70000h –7FFFFh	64/32	0	1	1	1	X	X	X
9	30000h-37FFFh	60000h – 6FFFFh	64/32	0	1	1	0	X	X	X
8	28000h-2FFFFh	50000h – 5FFFFh	64/32	0	1	0	1	X	X	X
7	20000h-27FFFh	40000h – 4FFFFh	64/32	0	1	0	0	X	X	X
6	18000h-1FFFFh	30000h – 3FFFFh	64/32	0	0	1	1	X	X	X
5	10000h-17FFFh	20000h – 2FFFFh	64/32	0	0	1	0	X	X	X
4	08000h-0FFFFh	10000h – 1FFFFh	64/32	0	0	0	1	X	X	X
3	04000h-07FFFh	08000h – 0FFFFh	32/16	0	0	0	0	1	X	X
2	03000h-03FFFh	06000h – 07FFFh	8/4	0	0	0	0	0	1	1
1	02000h-02FFFh	04000h – 05FFFh	8/4	0	0	0	0	0	1	0
0	00000h-01FFFh	00000h – 03FFFh	16/8	0	0	0	0	0	0	X

PRODUCT SELECTOR GUIDE

Product Number		EN29SL800	
Speed Option	Regulated Voltage Range: Vcc=1.8 –2.2V	**-70**	
	Full Voltage Range: Vcc=1.65 – 2.2 V		**-90**
Max Access Time, ns (t_{acc})		70	90
Max CE# Access, ns (t_{ce})		70	90
Max OE# Access, ns (t_{oe})		30	35

BLOCK DIAGRAM

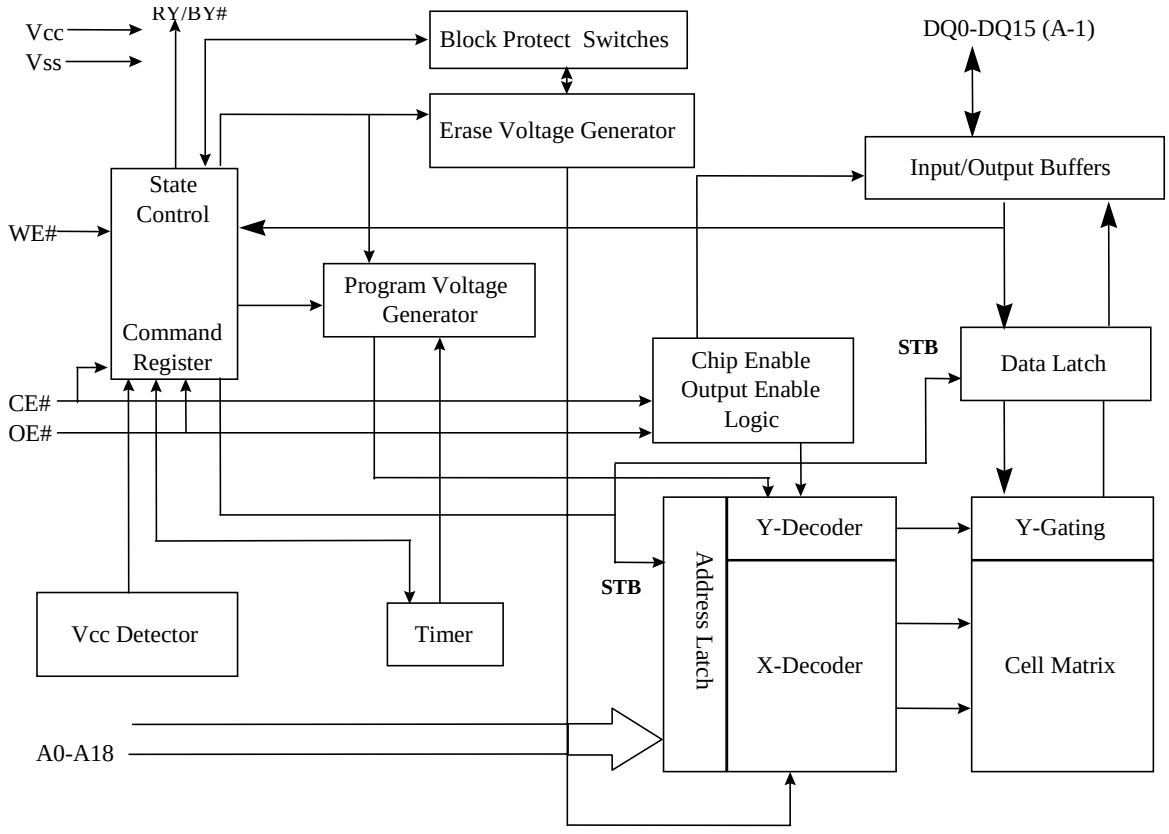


TABLE 3. OPERATING MODES

8M FLASH USER MODE TABLE

Operation	CE#	OE#	WE#	Reset#	A0-A18	DQ0-DQ7	DQ8-DQ15	
							Byte# = V_{IH}	Byte# = V_{IL}
Read	L	L	H	H	A_{IN}	D_{OUT}	D_{OUT}	High-Z
Write	L	H	L	H	A_{IN}	D_{IN}	D_{IN}	High-Z
CMOS Standby	$V_{cc} \pm 0.2V$	X	X	$V_{cc} \pm 0.2V$	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	X	High-Z	High-Z	High-Z
Hardware Reset	X	X	X	L	X	High-Z	High-Z	High-Z
Temporary Sector Unprotect	X	X	X	V_{ID}	A_{IN}	D_{IN}	D_{IN}	X
Sector Protect	L	H	L	V_{ID}	Sector Address, A6 = L, A1 = H, A0 = L	D_{IN}	X	X
Sector Unprotect	L	H	L	V_{ID}	Sector Address, A6 = L, A1 = H, A0 = L	D_{IN}	X	X

Notes:
L=logic low= V_{IL}, H=Logic High= V_{IH}, V_{ID} =10.0 ± 1.0V, X=Don't Care (either L or H, but not floating!),
D_{IN}=Data In, D_{OUT}=Data Out, A_{IN}=Address In

TABLE 4. DEVICE IDENTIFICTION (Autoselect Codes)

8M FLASH MANUFACTURER/DEVICE ID TABLE

Description	Mode	CE#	OE#	WE#	A18 to A12	A11 to A10	A9[2]	A8	A7	A6	A5 to A2	A1	A0	DQ8 to DQ15	DQ7 to DQ0
Manufacturer ID: Eon		L	L	H	X	X	V_{ID}	H[1]	X	L	X	L	L	X	1Ch
Device ID (top boot block)	Word	L	L	H	X	X	V_{ID}	X	X	L	X	L	H	22h	EAh
	Byte	L	L	H										X	EAh
Device ID (bottom boot block)	Word	L	L	H	X	X	V_{ID}	X	X	L	X	L	H	22h	6Bh
	Byte	L	L	H										X	6Bh
Sector Protection Verification		L	L	H	SA	X	V_{ID}	X	X	L	X	H	L	X	01h (Protected)
														X	00h (Unprotected)

Note:
1. If a manufacturing ID is read with A8=L, the chip will output a configuration code 7Fh. A further Manufacturing ID must be read with A8=H.
2. A9 = VID is for HV A9 Autoselect mode only. A9 must be ≤ Vcc (CMOS logic level) for Command Autoselect Mode.

USER MODE DEFINITIONS

Word / Byte Configuration

The signal set on the BYTE# Pin controls whether the device data I/O pins DQ15-DQ0 operate in the byte or word configuration. When the Byte# Pin is set at logic '1', then the device is in word configuration, DQ15-DQ0 are active and are controlled by CE# and OE#.

On the other hand, if the Byte# Pin is set at logic '0', then the device is in byte configuration, and only data I/O pins DQ0-DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8-DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

Standby Mode

The EN29SL800 has a CMOS-compatible standby mode, which reduces the current to $< 0.2\mu A$ (typical). It is placed in CMOS-compatible standby when the CE# pin is at $V_{CC} \pm 0.2$. RESET# and BYTE# pin must also be at CMOS input levels. If CE# and RESET# are held at V_{IH}, but not within $V_{CC} \pm 0.2V$, the device will be in the standby modes,but the standby current will be greater.The outputs are in a high-impedance state independent of the OE# input.

Read Mode

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See "Erase Suspend/Erase Resume Commands" for more additional information.

The system must issue the reset command to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See the "Reset Command" additional details.

Output Disable Mode

When the OE# pin is at a logic high level (V_{IH}), the output from the EN29SL800 is disabled. The output pins are placed in a high impedance state.

Auto Select Identification Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ15–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (9.0 V to 11.0 V) on address pin A9. Address pins A8, A6, A1, and A0 must be as shown in Autoselect Codes table. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits. Refer to the corresponding Sector Address Tables. The Command Definitions table shows the remaining address bits that are don't-care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ15–DQ0.

To access the autoselect codes in-system; the host system can issue the autoselect command via the command register, as shown in the Command Definitions table. This method does not require V_{ID}. See “Command Definitions” for details on using the autoselect mode.

Write Mode

Write operations, including programming data and erasing sectors of memory, require the host system to write a command or command sequence to the device. Write cycles are initiated by placing the byte or word address on the device’s address inputs while the data to be written is input on DQ[7:0] in Byte Mode (BYTE# = L) or on DQ[15:0] in Word Mode (BYTE# = H). The host system must drive the CE# and WE# pins Low and the OE# pin High for a valid write operation to take place. All addresses are latched on the falling edge of WE# and CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. The system is not required to provide further controls or timings. The device automatically provides internally generated program / erase pulses and verifies the programmed /erased cells’ margin. The host system can detect completion of a program or erase operation by observing the RY/BY# pin, or by reading the DQ[7] (Data# Polling) and DQ[6] (Toggle) status bits.

The ‘Command Definitions’ section of this document provides details on the specific device commands implemented in the EN29SL800.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at Vss±0.3 V, the device draws CMOS standby current (Icc2). If RESET# is held at VIL but not within Vss±0.3 V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firm- ware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin will immediately go to a “1” but the actual internal operations may be active until t_{READY} (During Embedded Algorithms: 20uS) amount of time has passed. The system thus must wait at least t_{READY} amount of time after the RESET# is asserted. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is "1"), the reset operation is completed within a time of t_{READY} (Not during Embedded Algorithms: 500nS). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to the DC Characteristics tables Icc3 for RESET# parameters and to the figures at page 26 on datasheet for the timing diagram.

Sector Protection/Unprotection

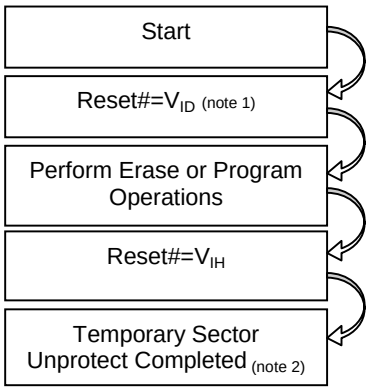
The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors.

There are two methods to enabling this hardware protection circuitry. The first one requires only that the RESET# pin be at V_{ID} and then standard microprocessor timings can be used to enable or disable this feature. See Flowchart 7a and 7b for the algorithm and Figure 12 for the timings. When doing Sector Unprotect, all the other sectors should be protected first.

The second method is meant for programming equipment. This method requires V_{ID} be applied to both OE# and A9 pin and non-standard microprocessor timings are used. This method is described in a separate document called EN29SL800 Supplement, which can be obtained by contacting a representative of Eon Silicon Solution, Inc.

Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sector groups to change data while in-system. The Sector Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sectors can be programmed or erased by simply selecting the sector addresses. Once is removed from the RESET# pin, all the previously protected sectors are protected again. See accompanying figure and timing diagrams for more details.



Notes:
1. All protected sectors unprotected.
2. Previously protected sectors protected again.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{acc} + 30ns. The automatic sleep mode is independent of the CE#, WE# and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output is latched and always available to the system. Icc_5 in the DC Characteristics table represents the automatic sleep mode current specification.

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes as seen in the Command Definitions table. Additionally, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by false system level signals during Vcc power up and power down transitions, or from system noise.

Low V_{CC} Write Inhibit

When Vcc is less than V_{LKO}, the device does not accept any write cycles. This protects data during Vcc power up and power down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until Vcc is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when Vcc is greater than V_{LKO}.

Write Pulse “Glitch” protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH}, or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one. If CE#, WE#, and OE# are all logical zero (not recommended usage), it will be considered a read.

Power-up Write Inhibit

During power-up, the device automatically resets to READ mode and locks out write cycles. Even with CE# = V_{IL}, WE# = V_{IL} and OE# = V_{IH}, the device will not accept commands on the rising edge of WE#.

COMMAND DEFINITIONS

The operations of EN29SL800 are selected by one or more commands written into the command register to perform Read/Reset Memory, Read ID, Read Sector Protection, Program, Sector Erase, Chip Erase, Erase Suspend and Erase Resume. Commands are made up of data sequences written at specific addresses via the command register. The sequences for the specified operation are defined in the Command Definitions table (Table 5). Incorrect addresses, incorrect data values or improper sequences will reset the device to Read Mode.

Table 5. EN29SL800 Command Definitions

Command Sequence			Cycles	Bus Cycles											
				1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read			1	RA	RD										
Reset			1	xxx	F0										
Autoselect	Manufacturer ID	Word	4	555	AA	2AA	55	555	90	000	7F				
										100	1C				
		Byte		AAA		555		AAA		000	7F				
										200	1C				
	Device ID Top Boot	Word	4	555	AA	2AA	55	555	90	X01	22EA				
		Byte		AAA		555		AAA		X02	EA				
	Device ID Bottom Boot	Word	4	555	AA	2AA	55	555	90	X01	226B				
		Byte		AAA		555		AAA		X02	6B				
	Sector Protect Verify	Word	4	555	AA	2AA	55	555	90	(SA) X02	XX00				
											XX01				
		Byte		AAA		555		AAA		(SA) X04	00				
											01				
Program		Word	4	555	AA	2AA	55	555	A0	PA	PD				
		Byte		AAA		555		AAA							
Chip Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
		Byte		AAA		555		AAA		AAA		555		AAA	
Sector Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
		Byte		AAA		555		AAA		AAA		555			
Erase Suspend			1	xxx	B0										
Erase Resume			1	xxx	30										

Address and Data values indicated in hex
RA = Read Address: address of the memory location to be read. This is a read cycle.
RD = Read Data: data read from location RA during Read operation. This is a read cycle.
PA = Program Address: address of the memory location to be programmed. X = Don't-Care
PD = Program Data: data to be programmed at location PA
SA = Sector Address: address of the Sector to be erased or verified. Address bits A18-A12 uniquely select any Sector.

Reading Array Data

The device is automatically set to reading array data after power up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

Following an Erase Suspend command, Erase Suspend mode is entered. The system can read array data using the standard read timings, with the only difference in that if it reads at an address within erase suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception.

The Reset command must be issued to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See next section for details on Reset.

Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don't-care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete. The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to reading array data (also applies to autoselect during Erase Suspend).

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. The Command Definitions table shows the address and data requirements. This is an alternative to the method that requires V_{ID} on address bit A9 and is intended for PROM programmers.

Two unlock cycles followed by the autoselect command initiate the autoselect command sequence. Autoselect mode is then entered and the system may read at addresses shown in Table 4 any number of times, without needing another command sequence.

The system must write the reset command to exit the autoselect mode and return to reading array data.

Word / Byte Programming Command

The device may be programmed by byte or by word, depending on the state of the Byte# Pin. Programming the EN29SL800 is performed by using a four bus-cycle operation (two unlock write cycles followed by the Program Setup command and Program Data Write cycle). When the program command is executed, no additional CPU controls or timings are necessary. An internal timer terminates the program operation automatically. Address is latched on the falling edge of CE# or WE#, whichever is last; data is latched on the rising edge of CE# or WE#, whichever is first.

Programming status may be checked by sampling data on DQ7 (DATA# polling) or on DQ6 (toggle bit). When the program operation is successfully completed, the device returns to read mode and the user can read the data programmed to the device at that address. Note that data can not be programmed from a 0 to a 1. Only an erase operation can change a data from 0 to 1. When programming time limit is exceeded, DQ5 will produce a logical "1" and a Reset command can return the device to Read mode.

Chip Erase Command

Chip erase is a six-bus-cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. The Command Definitions table shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Chip Erase algorithm are ignored.

The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. See “Write Operation Status” for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Flowchart 4 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in “AC Characteristics” for parameters, and to the Chip/Sector Erase Operation Timings for timing waveforms.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two un-lock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. The Command Definitions table shows the address and data requirements for the sector erase command sequence.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. Refer to “Write Operation Status” for information on these status bits. Flowchart 4 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations tables in the “AC Characteristics” section for parameters, and to the Sector Erase Operations Timing diagram for timing waveforms.

Erase Suspend / Resume Command

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Addresses are don’t-cares when writing the Erase Suspend command.

When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20 μs to suspend the erase operation.

After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See “Write Operation Status” for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See “Write Operation Status” for more information. The Autoselect command is not supported during Erase Suspend Mode.

The system must write the Erase Resume command (address bits are don’t-care) to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.

WRITE OPERATION STATUS

DQ7: DATA# Polling

The EN29SL800 provides DATA# polling on DQ7 to indicate the status of the embedded operations. The DATA# Polling feature is active during the embedded Programming, Sector Erase, Chip Erase, and Erase Suspend. (See Table 6)

When the embedded Programming is in progress, an attempt to read the device will produce the complement of the data last written to DQ7. Upon the completion of the embedded Programming, an attempt to read the device will produce the true data written to DQ7. For the embedded Programming, DATA# polling is valid after the rising edge of the fourth WE# or CE# pulse in the four-cycle sequence.

When the embedded Erase is in progress, an attempt to read the device will produce a “0” at the DQ7 output. Upon the completion of the embedded Erase, the device will produce the “1” at the DQ7 output during the read cycles. For Chip Erase, the DATA# polling is valid after the rising edge of the sixth WE# or CE# pulse in the six-cycle sequence. DATA# polling is valid after the last rising edge of the WE# or CE# pulse for chip erase or sector erase.

DATA# Polling must be performed at any address within a sector that is being programmed or erased and not a protected sector. Otherwise, DATA# polling may give an inaccurate result if the address used is in a protected sector.

Just prior to the completion of the embedded operations, DQ7 may change asynchronously when the output enable (OE#) is low. This means that the device is driving status information on DQ7 at one instant of time and valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status of valid data. Even if the device has completed the embedded operations and DQ7 has a valid data, the data output on DQ0-DQ6 may be still invalid. The valid data on DQ0-DQ7 will be read on the subsequent read attempts.

The flowchart for DATA# Polling (DQ7) is shown on Flowchart 5. The DATA# Polling (DQ7) timing diagram is shown in Figure 8.

RY/BY#: Ready/Busy

The RY/BY# is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or completed. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to Vcc.

In the output-low period, signifying Busy, the device is actively erasing or programming. This includes programming in the Erase Suspend mode. If the output is high, signifying the Ready, the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

DQ6: Toggle Bit I

The EN29SL800 provides a “Toggle Bit” on DQ6 to indicate to the host system the status of the embedded programming and erase operations. (See Table 6)

During an embedded Program or Erase operation, successive attempts to read data from the device at any address (by active OE# or CE#) will result in DQ6 toggling between “zero” and “one”. Once the embedded Program or Erase operation is completed, DQ6 will stop toggling and valid data will be read on the next successive attempts. During embedded Programming, the Toggle Bit is valid after the rising edge of the fourth WE# pulse in the four-cycle sequence. During Erase operation, the Toggle Bit is valid after the rising edge of the sixth WE# pulse for sector erase or chip erase.

In embedded Programming, if the sector being written to is protected, DQ6 will toggles for about 2 μs, then stop toggling without the data in the sector having changed. In Sector Erase or Chip Erase, if all selected sectors are protected, DQ6 will toggle for about 100 μs. The chip will then return to the read mode without changing data in all protected sectors.

The flowchart for the Toggle Bit (DQ6) is shown in Flowchart 6. The Toggle Bit timing diagram is shown in Figure 9.

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1.” This is a failure condition that indicates the program or erase cycle was not successfully completed. Since it is possible that DQ5 can become a 1 when the device has successfully completed its operation and has returned to read mode, the user must check again to see if the DQ6 is toggling after detecting a “1” on DQ5.

The DQ5 failure condition may appear if the system tries to program a “1” to a location that is previously programmed to “0.” **Only an erase operation can change a “0” back to a “1.”** Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, DQ5 produces a “1.” Under both these conditions, the system must issue the reset command to return the device to reading array data.

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the output on DQ3 can be used to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) When sector erase starts, DQ3 switches from “0” to “1.” This device does not support multiple sector erase command sequences so it is not very meaningful since it immediately shows as a “1” after the first 30h command. Future devices may support this feature.

DQ2: Erase Toggle Bit II

The “Toggle Bit” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence. DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to the following table to compare outputs for DQ2 and DQ6.

Flowchart 6 shows the toggle bit algorithm, and the section “DQ2: Toggle Bit” explains the algorithm. See also the “DQ6: Toggle Bit I” subsection. Refer to the Toggle Bit Timings figure for the toggle bit timing diagram. The DQ2 vs. DQ6 figure shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Flowchart 6 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Flowchart 6).

Write Operation Status

Operation		DQ7 (note2)	DQ6	DQ5 (note1)	DQ3	DQ2 (note2)	RY/BY#
Standard Mode	Embedded Program Algorithm	DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No Toggle	0	N/A	Toggle	1
	Reading within Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend Program	DQ7#	Toggle	0	N/A	N/A	0

1. DQ5 switches to ‘1’ when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See “DQ5:Exceeded Timing Limits” for more information.
2. DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.

Table 6. Status Register Bits

DQ	Name	Logic Level	Definition
7	DATA# POLLING	'1'	Erase Complete or erase Sector in Erase suspend
		'0'	Erase On-Going
		DQ7	Program Complete or data of non-erase Sector during Erase Suspend
		DQ7#	Program On-Going
6	TOGGLE BIT	'-1-0-1-0-1-0-1-'	Erase or Program On-going
		DQ6	Read during Erase Suspend
		'-1-1-1-1-1-1-1-'	Erase Complete
5	ERROR BIT	'1'	Program or Erase Error
		'0'	Program or Erase On-going
3	ERASE TIME BIT	'1'	Erase operation start
		'0'	Erase timeout period on-going
2	TOGGLE BIT	'-1-0-1-0-1-0-1-'	Chip Erase, Sector Erase or Erase suspend on currently addressed Sector. (When DQ5=1, Erase Error due to currently addressed Sector. Program during Erase Suspend on-going at current address
		DQ2	Erase Suspend read on non Erase Suspend Sector

Notes:

DQ7 DATA# Polling: indicates the P/E C status check during Program or Erase, and on completion before checking bits DQ5 for Program or Erase Success.

DQ6 Toggle Bit: remains at constant level when P/E operations are complete or erase suspend is acknowledged. Successive reads output complementary data on DQ6 while programming or Erase operation are on-going.

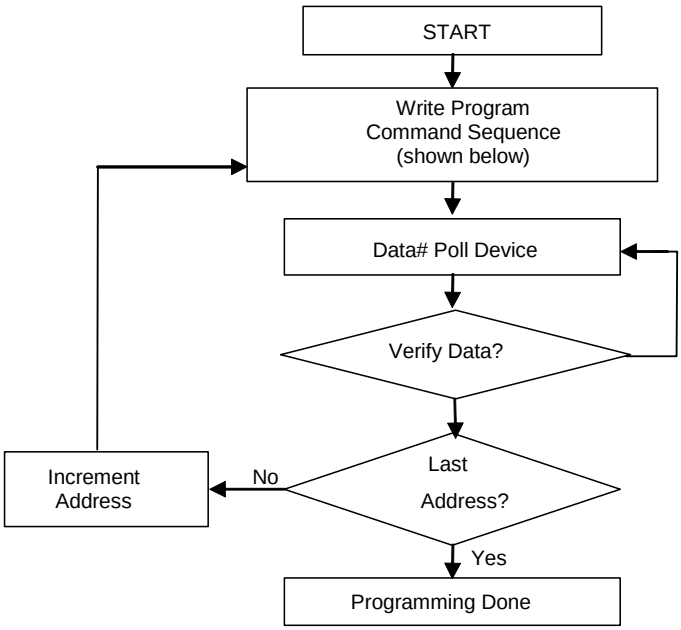
DQ5 Error Bit: set to "1" if failure in programming or erase

DQ3 Sector Erase Command Timeout Bit: Operation has started. Only possible command is Erase suspend (ES).

DQ2 Toggle Bit: indicates the Erase status and allows identification of the erased Sector.

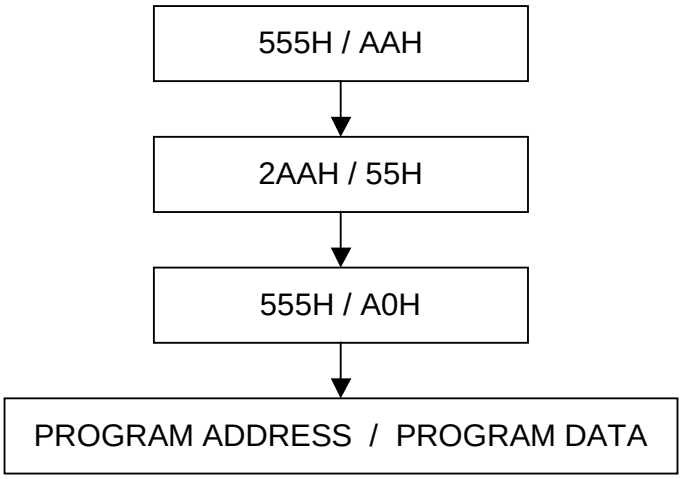
EMBEDDED ALGORITHMS

Flowchart 1. Embedded Program

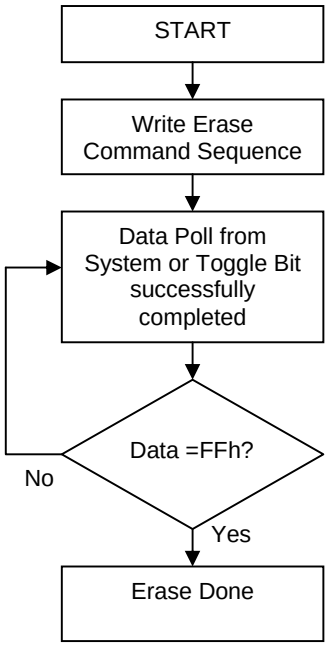


Flowchart 2. Embedded Program Command Sequence

See the Command Definitions section for more information on WORD mode.

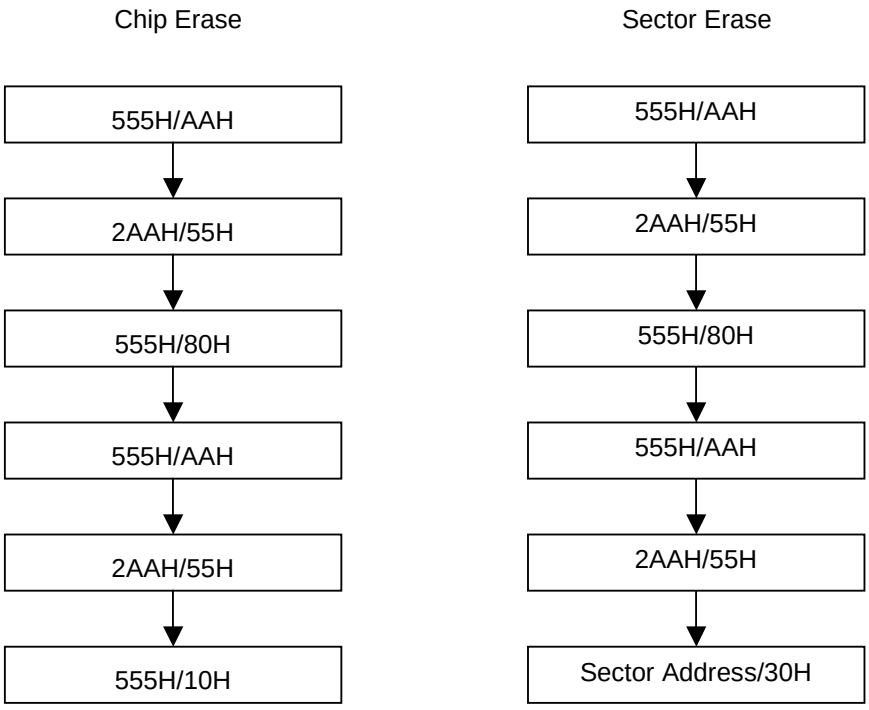


Flowchart 3. Embedded Erase

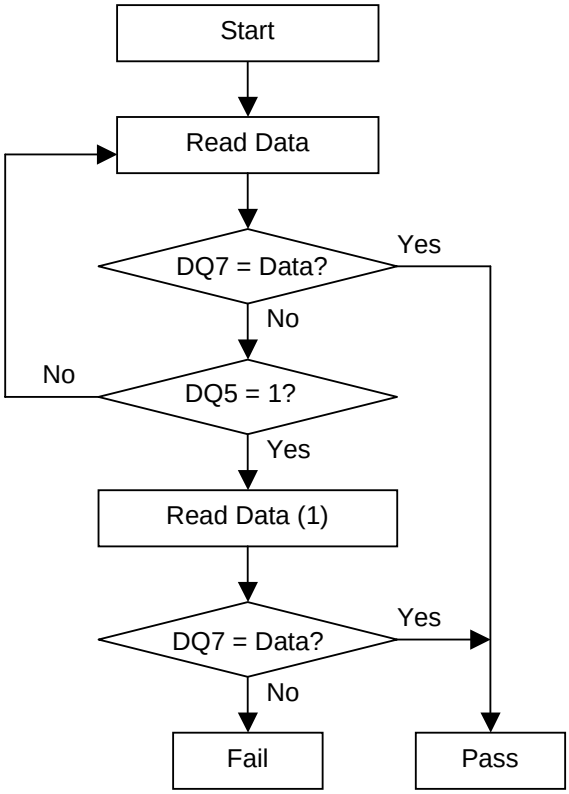


Flowchart 4. Embedded Erase Command Sequence

See the Command Definitions section for more information on WORD mode.

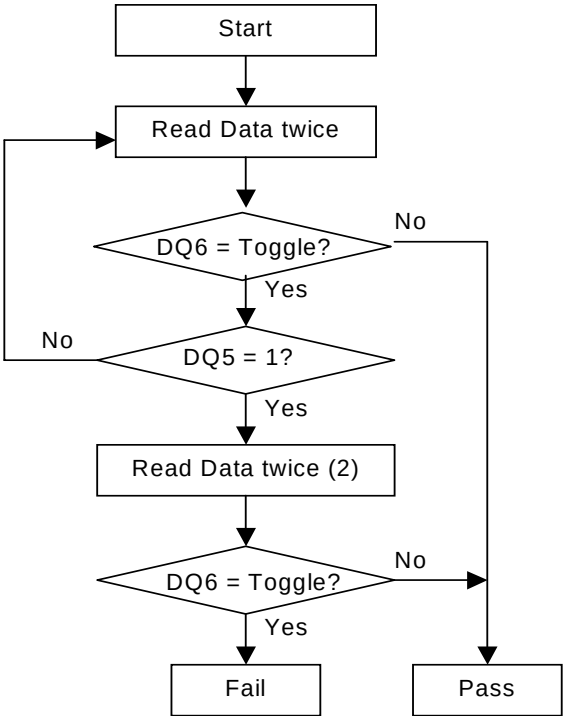


Flowchart 5. DATA# Polling Algorithm



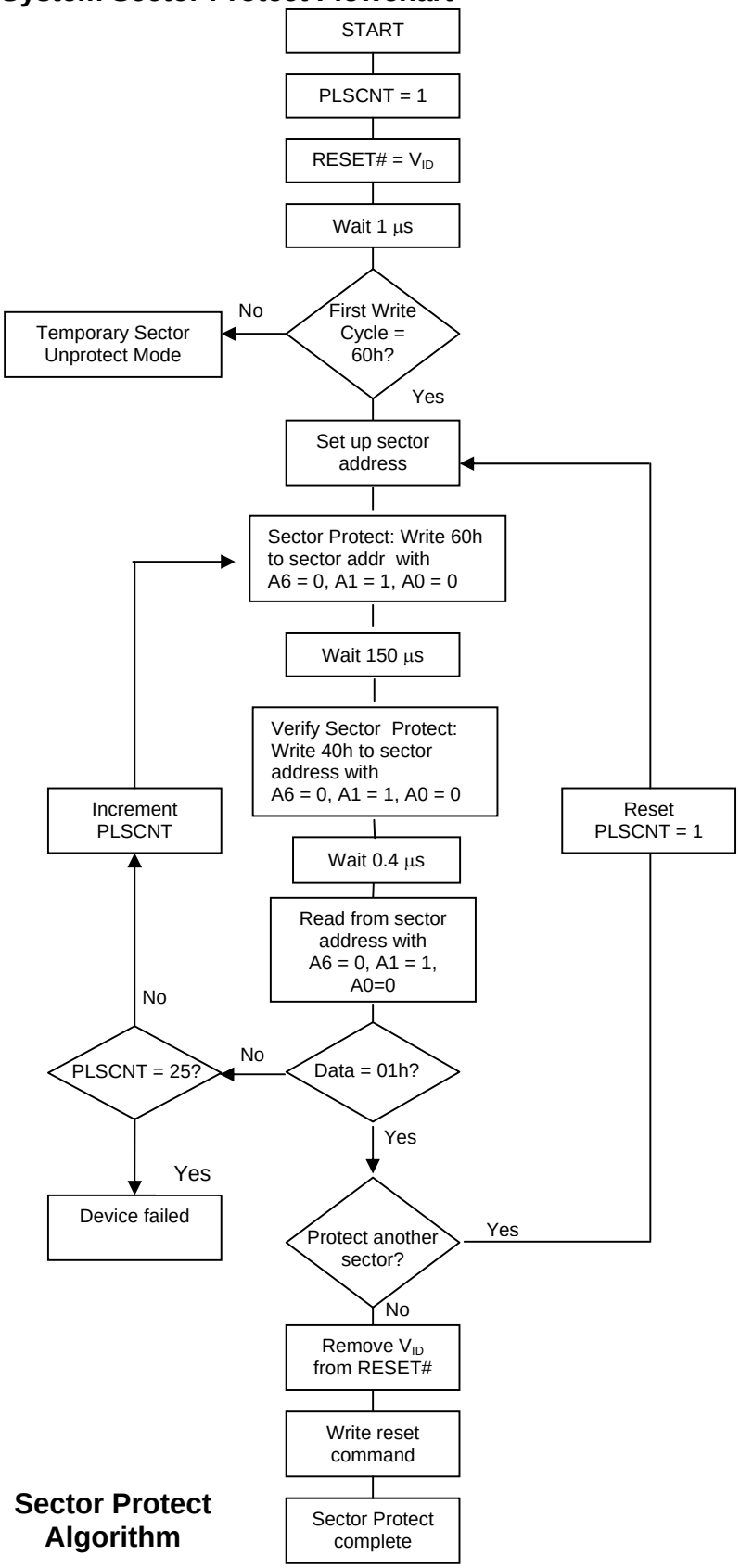
Notes:
(1) This second read is necessary in case the first read was done at the exact instant when the status data was in transition.

Flowchart 6. Toggle Bit Algorithm



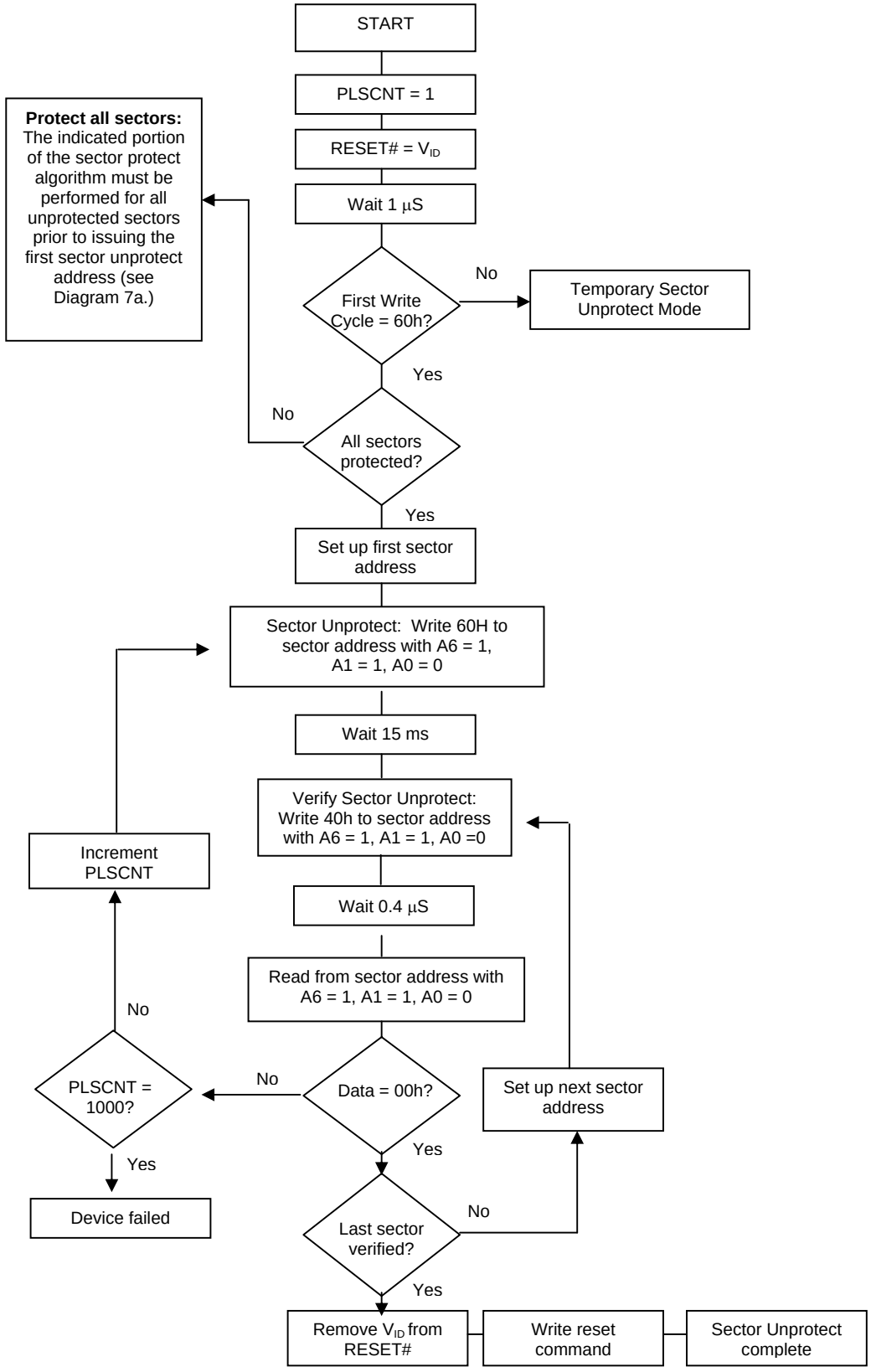
Notes:
(2) This second set of reads is necessary in case the first set of reads was done at the exact instant when the status data was in transition.

Flowchart 7a. In-System Sector Protect Flowchart



Sector Protect Algorithm

Flowchart 7b. In-System Sector Unprotect Flowchart



Sector Unprotect Algorithm

Table 7. DC Characteristics

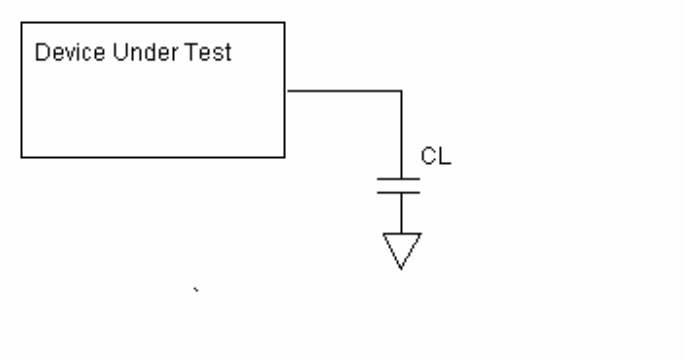
(T_a = 0°C to 70°C or - 40°C to 85°C; V_{CC} = 1.65-2.2V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	0V≤ V_{IN} ≤ Vcc			±3	µA
I_{LO}	Output Leakage Current	0V≤ V_{OUT} ≤ Vcc			±3	µA
I_{CC1}	Active Read Current (Byte mode)	CE# = V_{IL}, OE# = V_{IH}, F=5MHz		15	30	mA
	Active Read Current (Word mode)			15	30	mA
I_{CC2}	Supply Current (Standby - CMOS)	CE# = BYTE# = RESET# = Vcc (Note 1)		0.2	5.0	µA
I_{CC3}	VCC , Reset Current	CE# = BYTE# = RESET# = Vcc (Note 1)		0.2	5.0	µA
I_{CC4}	Supply Current (Program or Erase)	Byte program, Sector or Chip Erase in progress		15	30	mA
I_{CC5}	Automatic Sleep Mode	V_{IH} = Vcc ± 0.2 V V_{IL} = Vss ± 0.2 V		0.2	5.0	µA
V_{IL}	Input Low Voltage		-0.5		0.3 x VCC	V
V_{IH}	Input High Voltage		0.7 x Vcc		Vcc + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA			0.25	V
V_{OH}	Output High Voltage TTL	I_{OH} = -2.0 mA	0.85 x Vcc			V
	Output High Voltage CMOS	I_{OH} = -100 µA,	Vcc - 0.4V			V
V_{ID}	A9 Voltage (Electronic Signature)		9.0	10.0	11.0	V
I_{ID}	A9 Current (Electronic Signature)	A9 = V_{ID}			50	µA
V_{LKO}	Supply voltage (Erase and Program lock-out)		1.2		1.5	V

Notes

1. BYTE# pin can also be GND ± 0.3V. BYTE# and RESET# pin input buffers are always enabled so that they draw power if not at full CMOS supply voltages.

Test Conditions



Test Specifications

Test Conditions	-70	-90	Unit
Output Load	1 TTL gate		
Output Load Capacitance, C_L	15	100	pF
Input Rise and Fall times	5	5	ns
Input Pulse Levels	0.0-2.0	0.0-2.0	V
Input timing measurement reference levels	1/2 Vcc	1/2 Vcc	V
Output timing measurement reference levels	1/2 Vcc	1/2 Vcc	V

AC CHARACTERISTICS

Hardware Reset (Reset#)

(T_a = 0°C to 70°C or - 40°C to 85°C; V_{CC} = 1.65-2.2V)

Parameter Std	Description	Test Setup	Speed options		Unit
			-70	-90	
t_{READY}	Reset# Pin Low to Read or Write Embedded Algorithms	Max	20		µs
t_{READY}	Reset# Pin Low to Read or Write Non Embedded Algorithms	Max	500		ns
t_{RP}	Reset# Pulse Width	Min	500		ns
t_{RH}	Reset# High Time Before Read	Min	50		ns

Reset# Timings

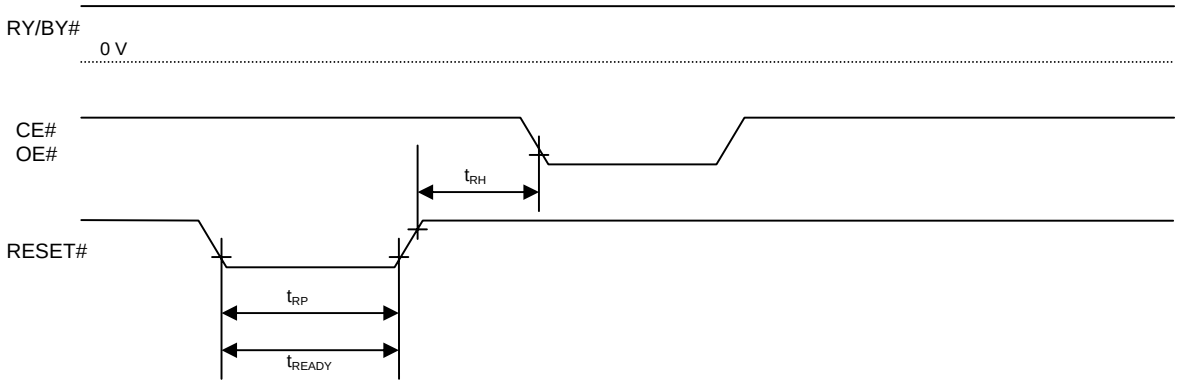


Figure 1. Reset Timing NOT During Embbedded

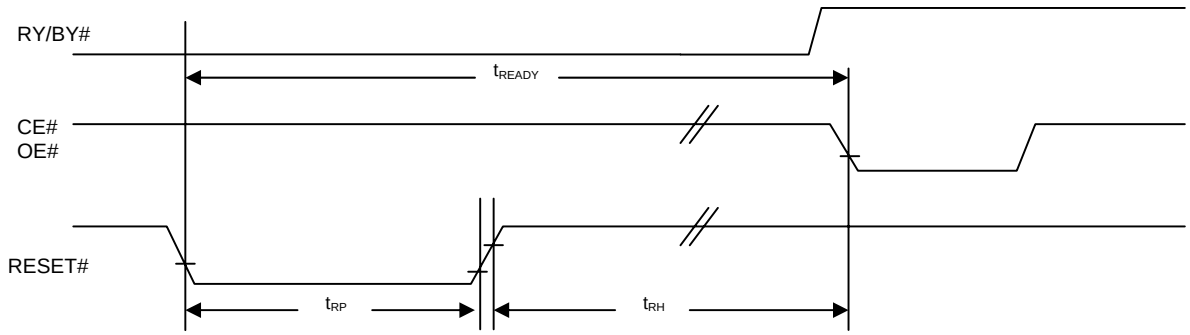


Figure 2. Reset Timings During Embedded

AC CHARACTERISTICS
Word / Byte Configuration (Byte#)

(T_a = 0°C to 70°C or - 40°C to 85°C; V_{CC} = 1.65-2.2V)

Std Parameter	Description		Speed		Unit
			-70	-90	
t_{BCS}	Byte# to CE# switching setup time	Min	0	0	ns
t_{CBH}	CE# to Byte# switching hold time	Min	0	0	ns
t_{RBH}	RY/BY# to Byte# switching hold time	Min	0	0	ns

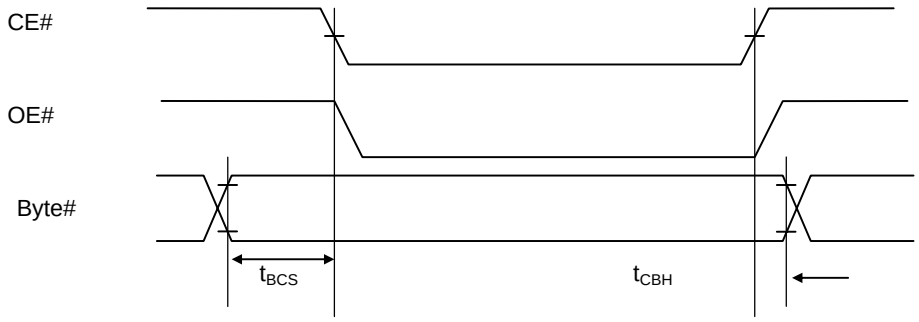


Figure 3. Byte# timings for Read Operations

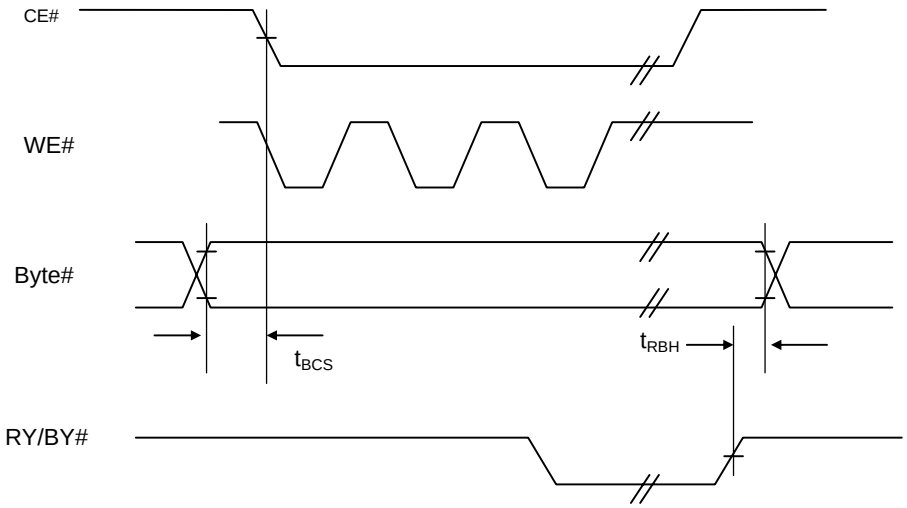


Figure 4. Byte# timings for Write Operations

Note: Switching BYTE# pin not allowed during embedded operations

Table 8. AC CHARACTERISTICS

(T_a = 0°C to 70°C or - 40°C to 85°C; V_{CC} = 1.65-2.2 V for 90ns , V_{CC} = 1.7-2.2 V for 70ns)

Read-only Operations Characteristics

Parameter Symbols		Description	Test Setup		Speed Options		
JEDEC	Standard				-70	-90	Unit
t_{AVAV}	t_{RC}	Read Cycle Time		Min	70	90	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	CE# = V_{IL} OE# = V_{IL}	Max	70	90	ns
t_{ELQV}	t_{CE}	Chip Enable To Output Delay	OE# = V_{IL}	Max	70	90	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		Max	30	35	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z		Max	20	20	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z		Max	20	20	ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, CE# or OE#, whichever occurs first		Min	0	0	ns

Notes:

For – 70 Vcc = 1.7-2.2 V
Output Load : 1 TTL gate and 15pF
Input Rise and Fall Times: 5ns
Input Rise Levels: 0.0 V to Vcc
Timing Measurement Reference Level, Input and Output: 1/2 Vcc

For all others: Vcc =1.65 – 2.2V
Output Load: 1 TTL gate and 100 pF
Input Rise and Fall Times: 5 ns
Input Pulse Levels: 0.0 V to Vcc
Timing Measurement Reference Level, Input and Output: 1/2 Vcc

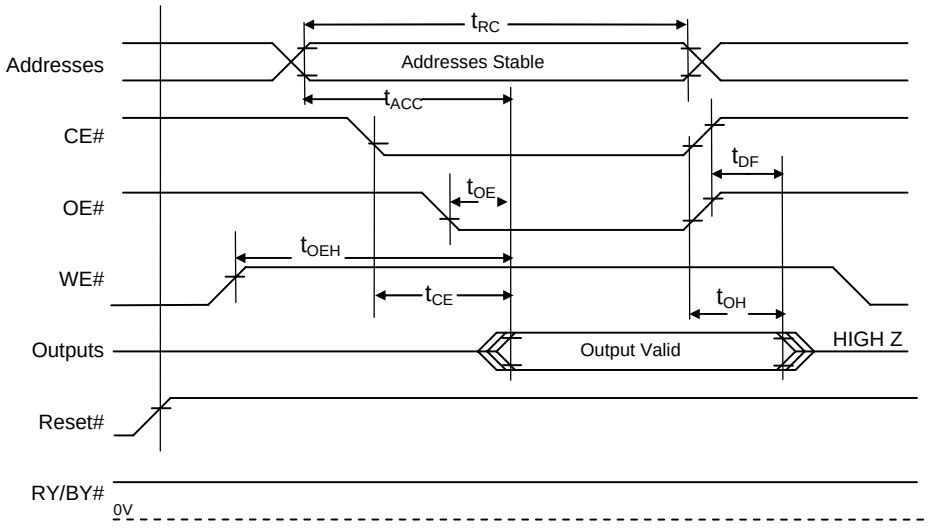


Figure 5. AC Waveforms for READ Operations

Table 9. AC CHARACTERISTICS

(T_a = 0°C to 70°C or - 40°C to 85°C; V_{CC} = 1.65-2.2V)

Write (Erase/Program) Operations

Parameter Symbols		Description		Speed Options		
JEDEC	Standard			-70	-90	Unit
t_{AVAV}	t_{WC}	Write Cycle Time	Min	70	90	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45	45	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	30	45	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0	0	ns
	t_{OES}	Output Enable Setup Time	Min	0	0	ns
t_{GHWL}	t_{GHWL}	Read Recovery Time before Write (OE# High to WE# Low)	Min	0	0	ns
t_{ELWL}	t_{CS}	CE# SetupTime	Min	0	0	ns
t_{WHEH}	t_{CH}	CE# Hold Time	Min	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	35	45	ns
t_{WHDL}	t_{WPH}	Write Pulse Width High	Min	20	20	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Word AND Byte Mode)	Typ	5	5	µs
			Max	7	7	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation	Typ	0.5	0.5	s

Table 10. AC CHARACTERISTICS

(T_a = 0°C to 70°C or - 40°C to 85°C; V_{CC} = 1.65-2.2V)

Write (Erase/Program) Operations

Alternate CE# Controlled Writes

Parameter Symbols				Speed Options		
JEDEC	Standard	Description		-70	-90	Unit
t_{AVAV}	t_{WC}	Write Cycle Time	Min	70	90	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45	45	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	30	45	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0	0	ns
	t_{OES}	Output Enable Setup Time	Min	0	0	ns
t_{GHEL}	t_{GHEL}	Read Recovery Time before Write (OE# High to CE# Low)	Min	0	0	ns
t_{WLEL}	t_{WS}	WE# SetupTime	Min	0	0	ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0	0	ns
t_{ELEH}	t_{CP}	CE# Pulse Width	Min	35	45	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High	Min	20	20	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (byte AND word mode)	Typ	5	5	µs
			Max	7	7	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation	Typ	0.5	0.5	s

Table 11. ERASE AND PROGRAMMING PERFORMANCE

Parameter		Limits			Comments
		Typ	Max	Unit	
Sector Erase Time		0.5	10	sec	Excludes 00H programming prior to erasure
Chip Erase Time		8		sec	
Byte Programming Time		5		µs	Excludes system level overhead
Word Programming Time		7		µs	
Chip Programming Time	Byte	5.3		sec	
	Word	3.7			
Erase/Program Endurance		100K		cycles	Minimum 100K cycles

Table 12. LATCH UP CHARACTERISTICS

Parameter Description	Min	Max
Input voltage with respect to V_{ss} on all pins except I/O pins (including A9, Reset# and OE#)	-1.0 V	12.0 V
Input voltage with respect to V_{ss} on all I/O Pins	-1.0 V	Vcc + 1.0 V
Vcc Current	-100 mA	100 mA

Note : These are latch up characteristics and the device should never be put under these conditions. Refer to Absolute Maximum ratings for the actual operating limits.

Table 14. 48-PIN TSOP PIN CAPACITANCE @ 25°C, 1.0MHz

(V_{CC} = 1.65-2.2V)

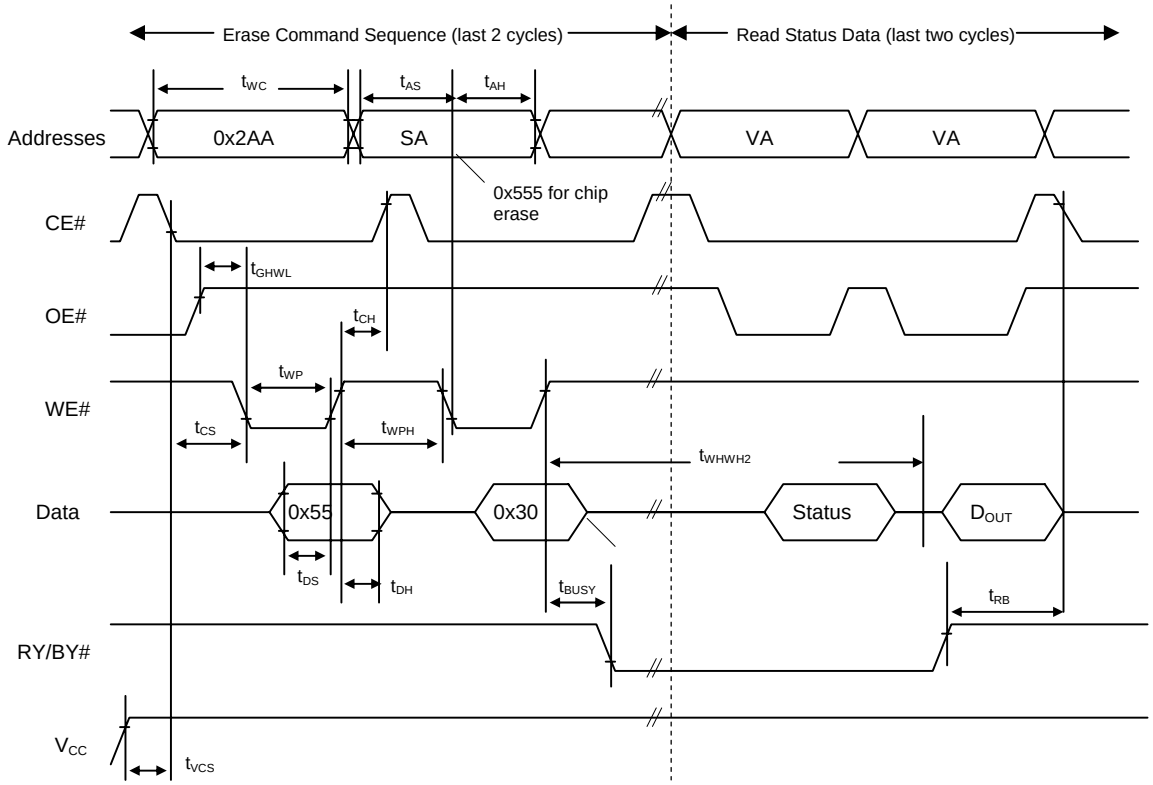
Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Table 15. DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

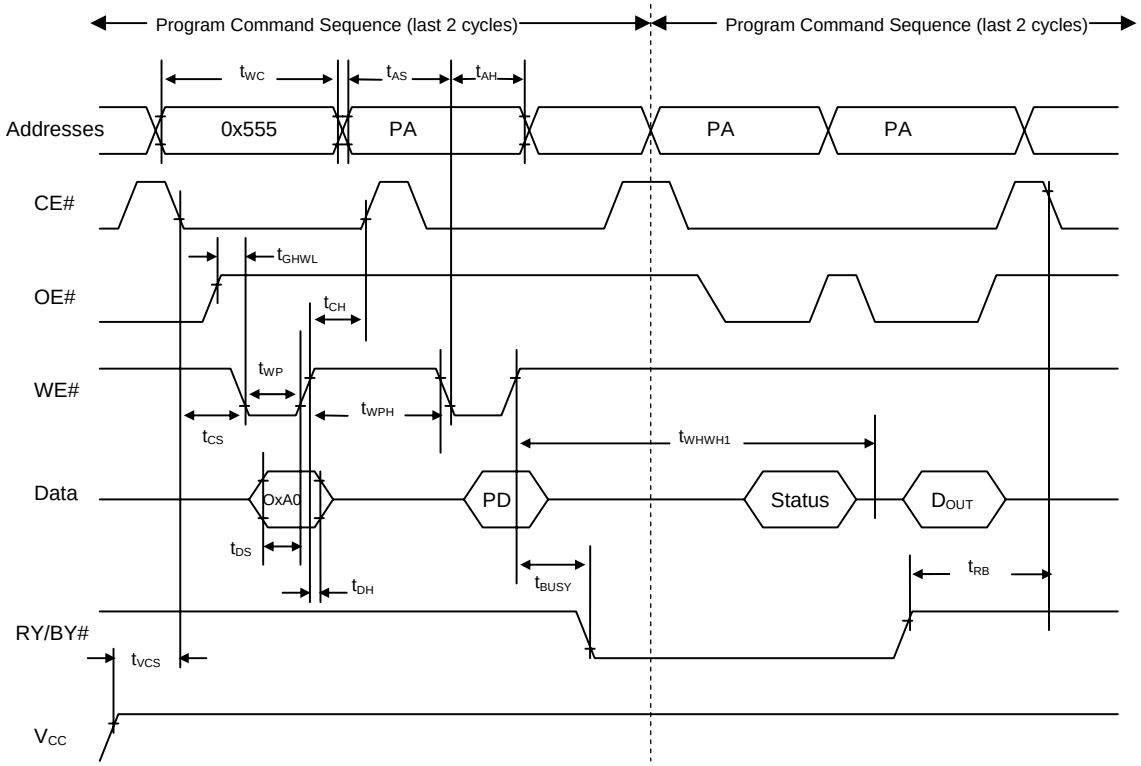
AC CHARACTERISTICS

Figure 6. AC Waveforms for Chip/Sector Erase Operations Timings



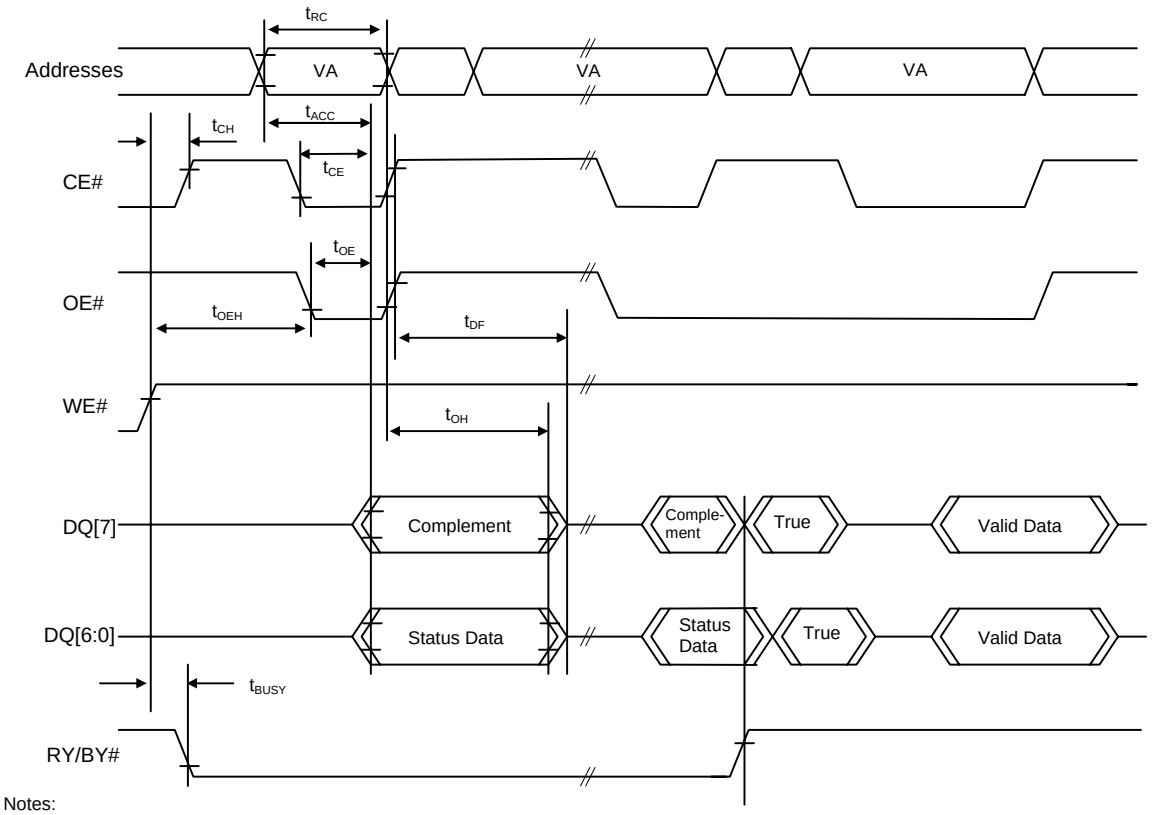
Notes:
1. SA=Sector Address (for sector erase), VA=Valid Address for reading status, D_{out}=true data at read address.
2. V_{cc} shown only to illustrate t_{vcs} measurement references. It cannot occur as shown during a valid command sequence.

Figure 7. Program Operation Timings



Notes:
1. PA=Program Address, PD=Program Data, D_{OUT} is the true data at the program address.
2. V_{CC} shown in order to illustrate t_{VCS} measurement references. It cannot occur as shown during a valid command sequence.

Figure 8. AC Waveforms for /DATA Polling During Embedded Algorithm Operations



Notes:
1. VA=Valid Address for reading Data# Polling status data
2. This diagram shows the first status cycle after the command sequence, the last status read cycle and the array data read cycle.

Figure 9. AC Waveforms for Toggle Bit During Embedded Algorithm Operations

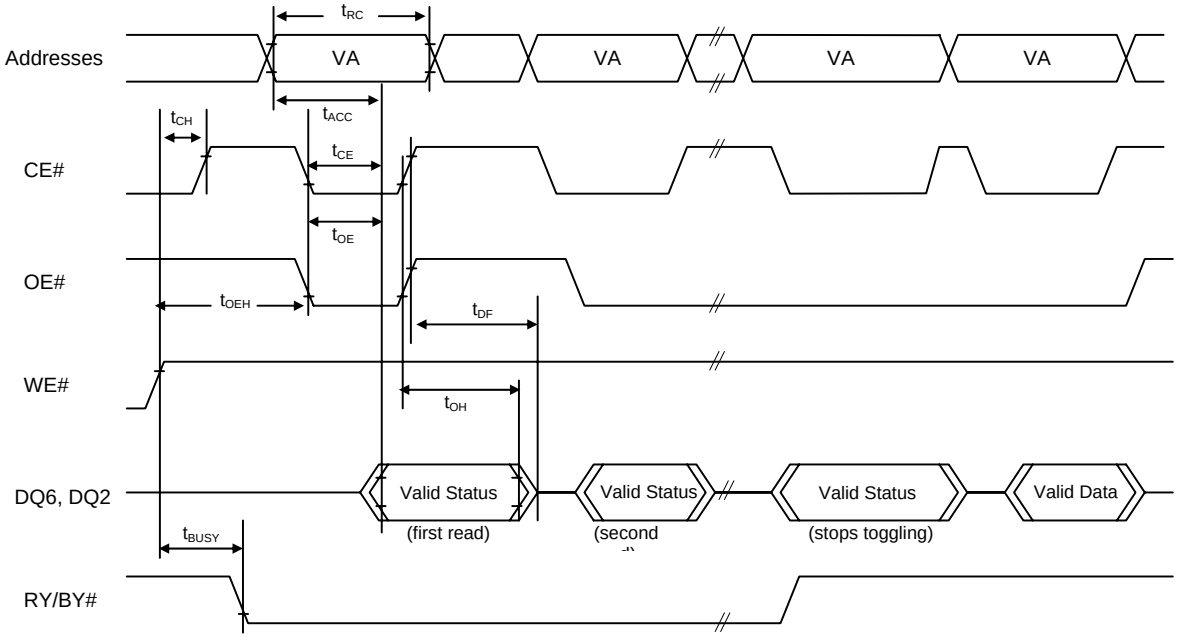
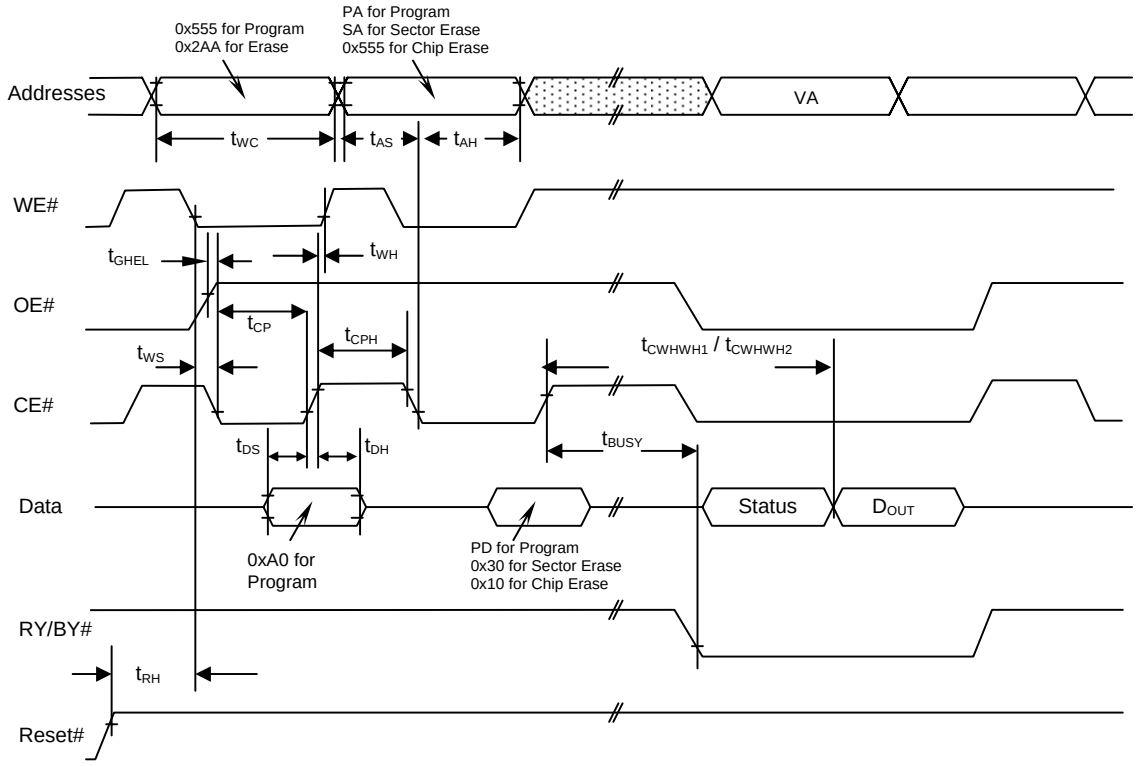


Figure 10. Alternate CE# Controlled Write Operation Timings



Notes:

PA = address of the memory location to be programmed.
PD = data to be programmed at byte address.
VA = Valid Address for reading program or erase status
D_{out} = array data read at VA
Shown above are the last two cycles of the program or erase command sequence and the last status read cycle
Reset# shown to illustrate t_{RH} measurement references. It cannot occur as shown during a valid command sequence.

Figure 11. DQ2 vs. DQ6

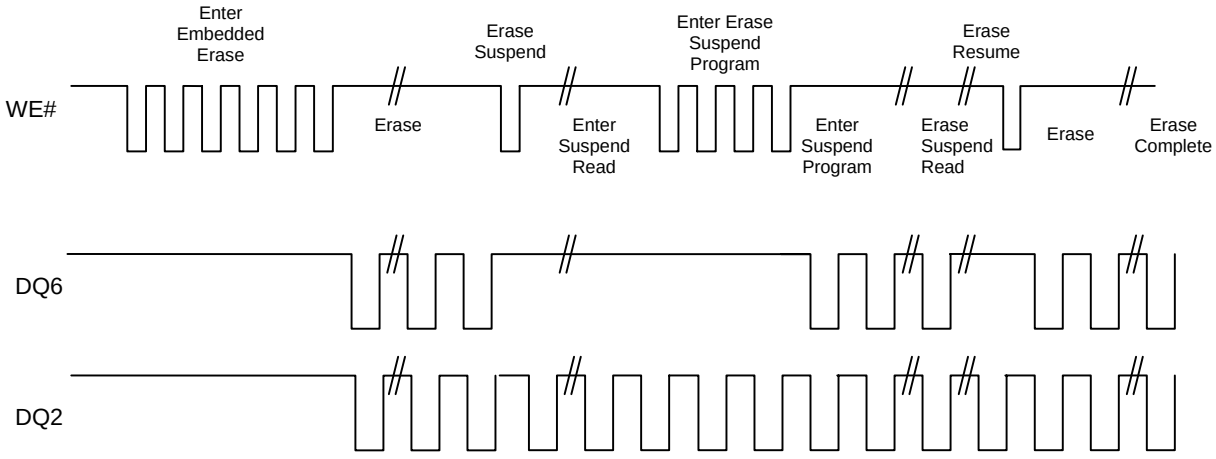
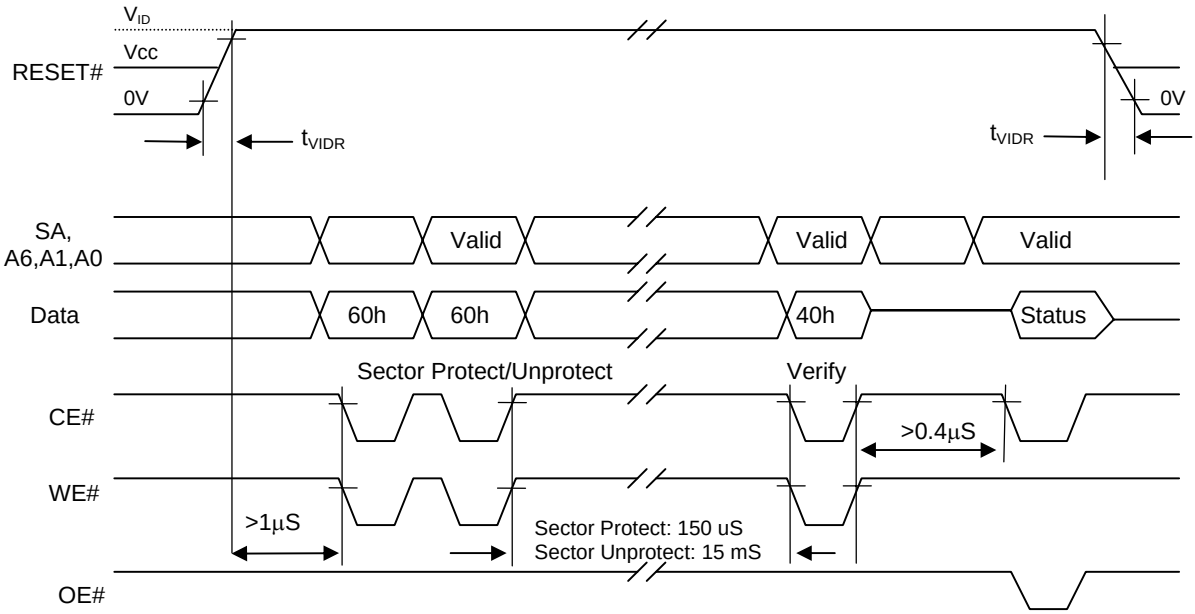


Figure 12. Sector Protect/Unprotect Timing Diagram



Notes:
Use standard microprocessor timings for this device for read and write cycles.
For Sector Protect, use A6=0, A1=1, A0=0. For Sector Unprotect, use A6=1, A1=1, A0=0.

Temporary Sector Unprotect

Parameter Std	Description		Speed Option		Unit
			-70	-90	
t_{VIDR}	V_{ID} Rise and Fall Time	Min	500		ns
t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4		µs

Figure 13. Temporary Sector Unprotect Timing Diagram

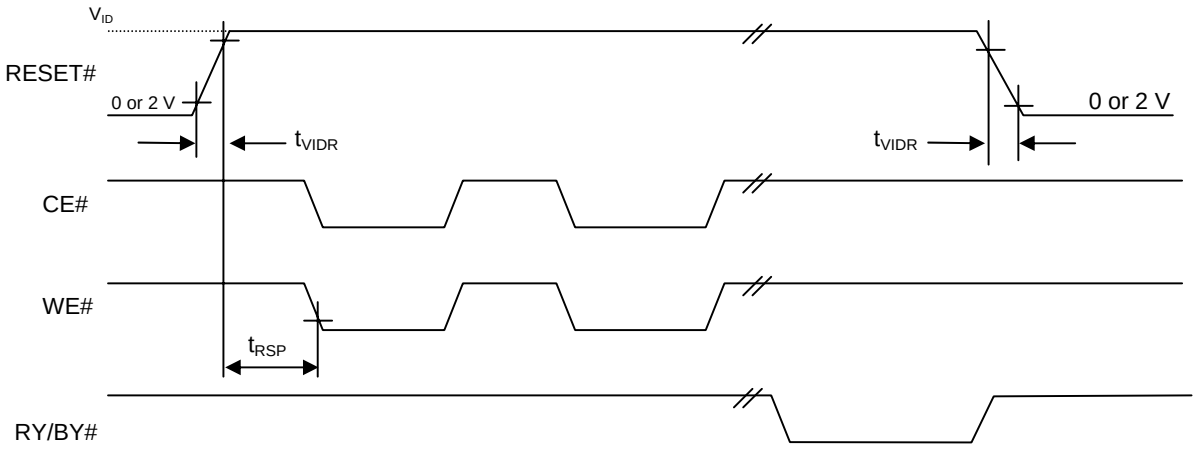
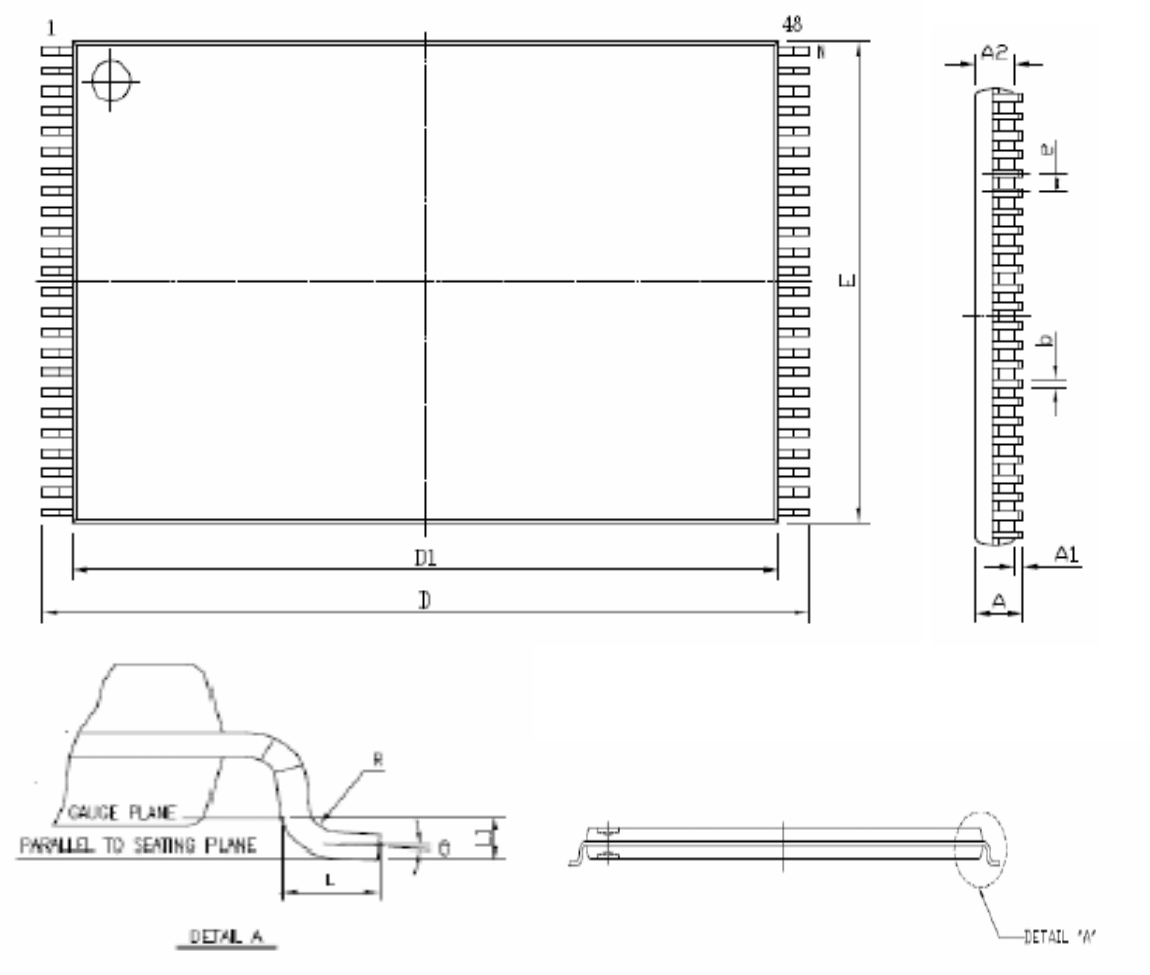


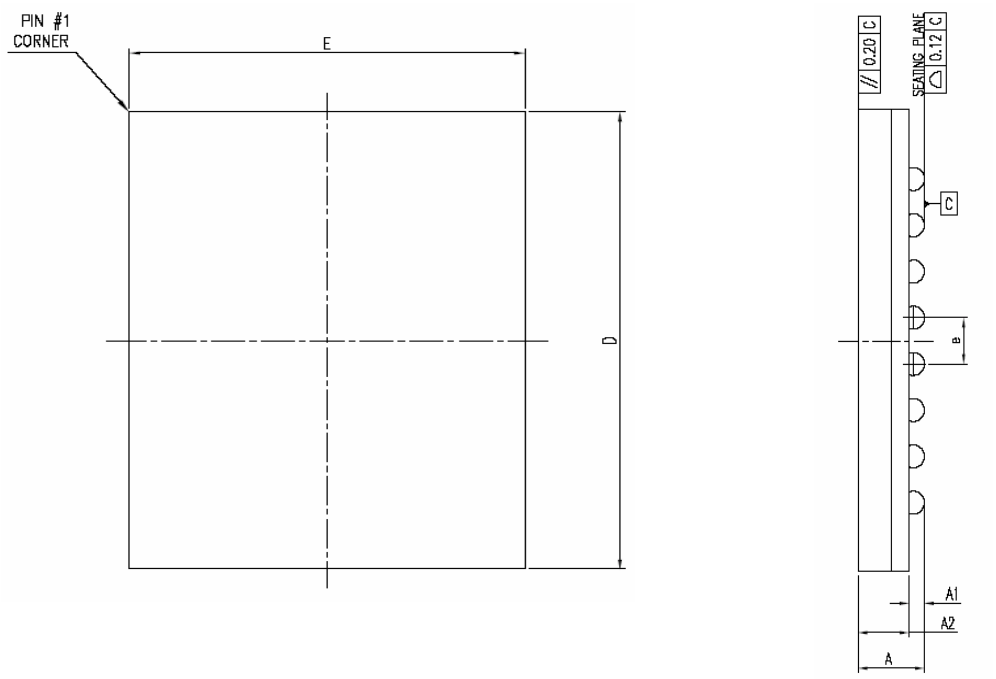
FIGURE 14. TSOP 12mm x 20mm

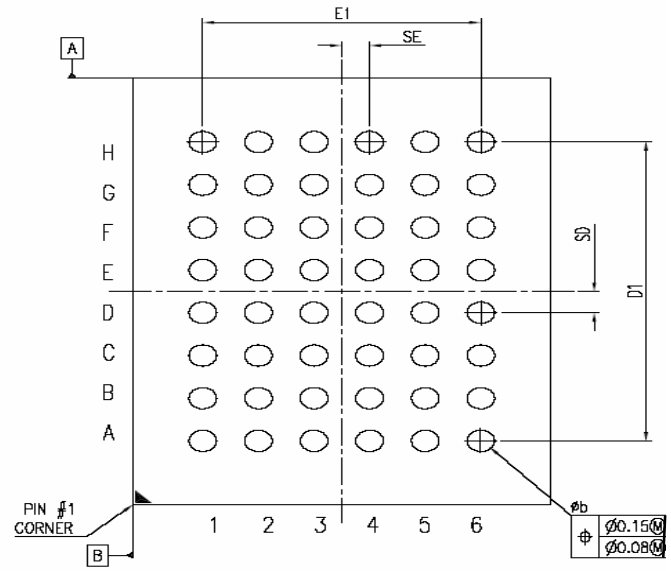


SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	- - -	- - -	1.20
A1	0.05	- - -	0.15
A2	0.95	1.00	1.05
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.9	12.00	12.10
e	- - -	0.50	- - -
b	0.17	0.22	0.27
L	0.5	0.60	0.70
L1	- - -	0.25	- - -
R	0.08	- - -	0.20
θ	0^0	3^0	5^0

Note : 1. Coplanarity: 0.1 mm
2. Max. allowable mold flash is 0.15 mm at the pkg ends, 0.25 mm between leads.

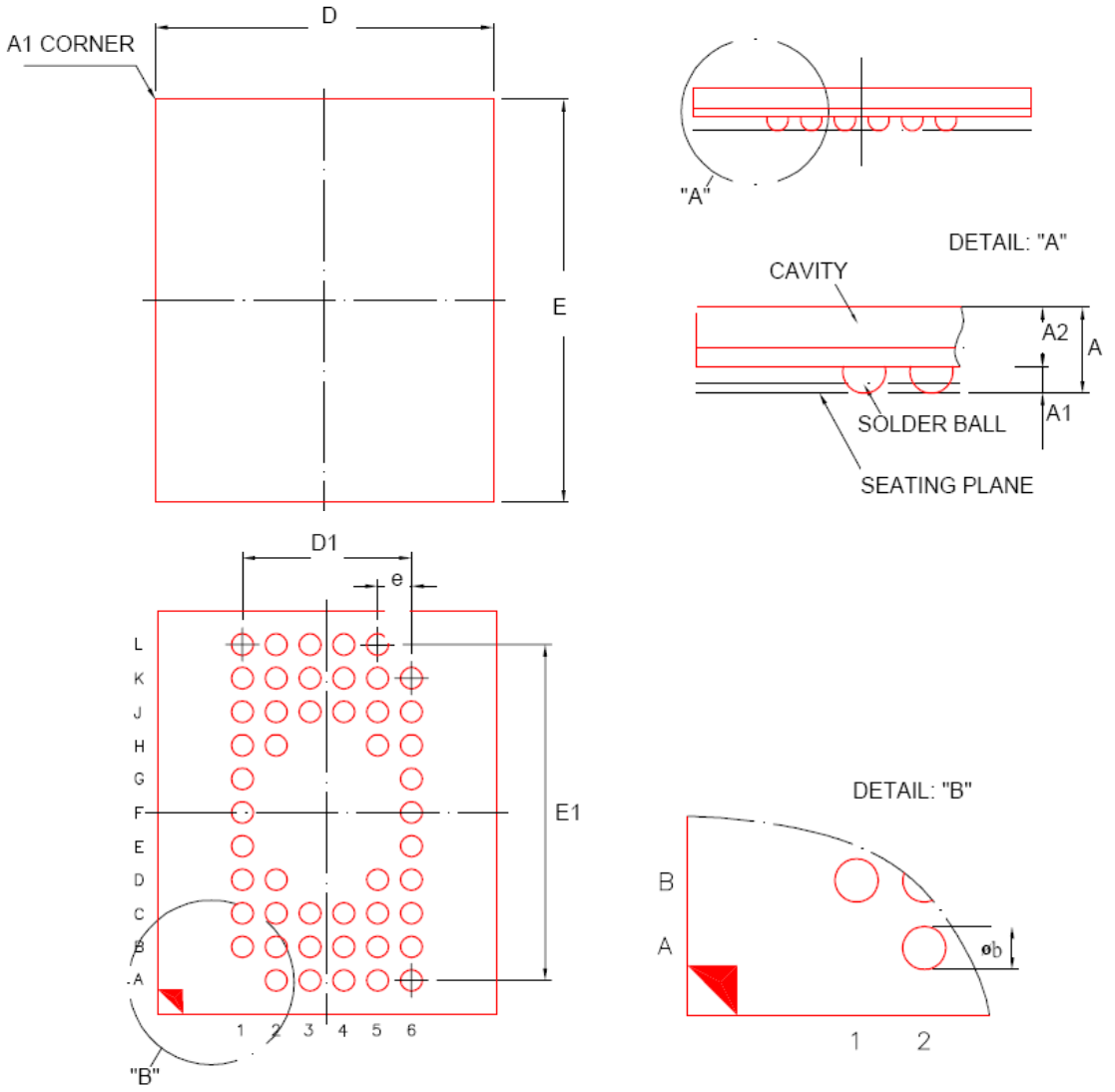
FIGURE 15. FBGA 6mm x 8mm





SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	- - -	- - -	1.31
A1	0.23	0.28	0.33
A2	0.86	0.92	0.98
D	7.90	8.00	8.10
E	5.90	6.00	6.10
D1	- - -	5.60	- - -
E1	- - -	4.00	- - -
SD	- - -	0.40	- - -
SE	- - -	0.40	- - -
e	- - -	0.80	- - -
b	0.35	0.40	0.45

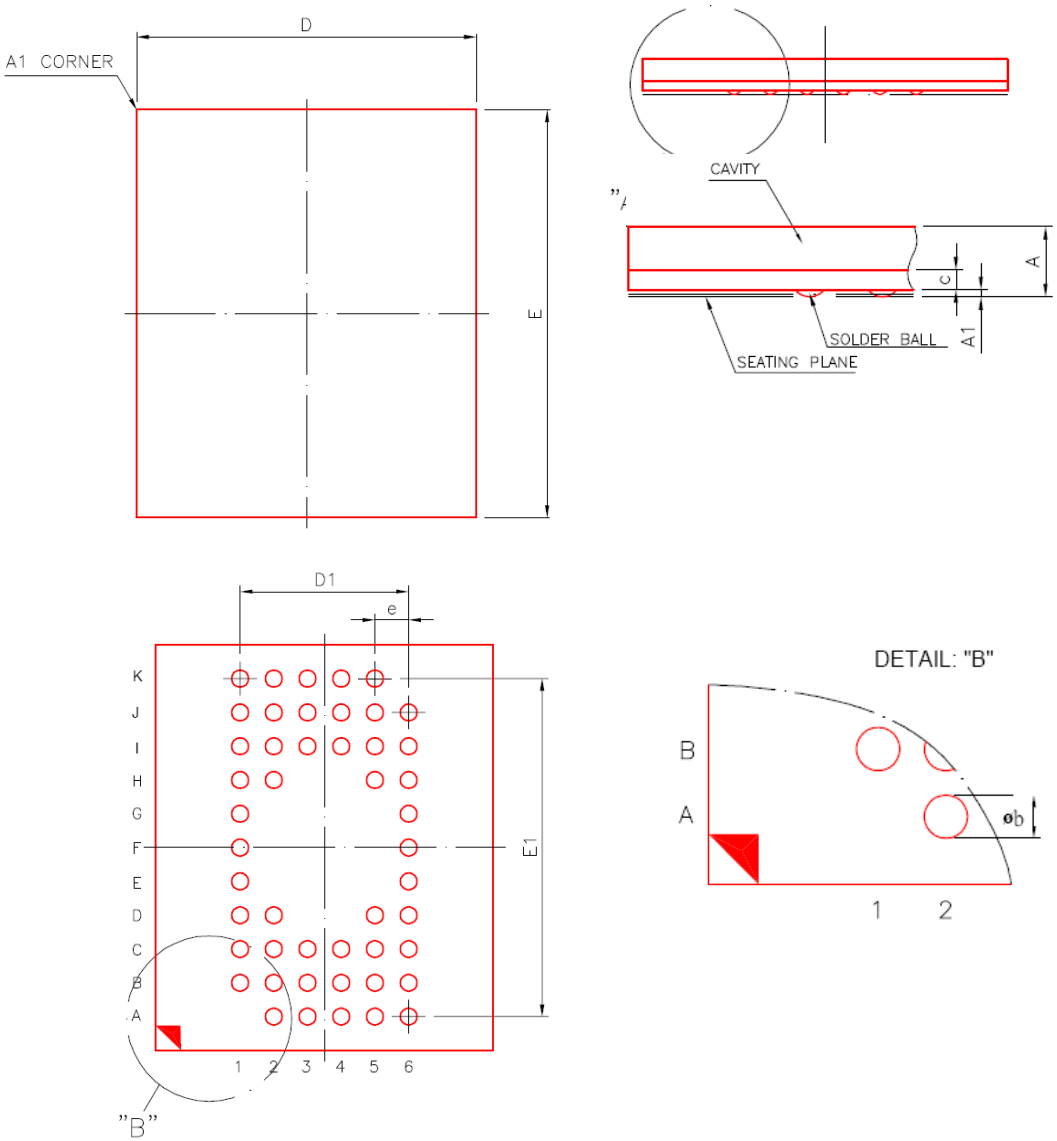
FIGURE 16. WFBGA 5mm x 6mm



SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	- - -	- - -	0.73
A1	0.16	0.21	0.26
A2	- - -	0.436	- - -
D	4.90	5.00	5.10
E	5.90	6.00	6.10
D1	- - -	2.50	- - -
E1	- - -	5.00	- - -
e	- - -	0.50	- - -
øb	0.27	0.32	0.37

Note : 1. Coplanarity: 0.1 mm

FIGURE 17. WLBGA 5mm x 6mm



SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	- - -	- - -	0.535
A1	0.02	0.05	0.08
D	4.90	5.00	5.10
E	5.90	6.00	6.10
D1	- - -	2.50	- - -
E1	- - -	5.00	- - -
e	- - -	0.50	- - -
øb	0.20	0.25	0.30

Note : 1. Coplanarity: 0.06 mm

ABSOLUTE MAXIMUM RATINGS

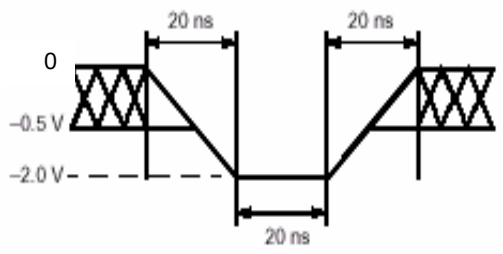
Parameter		Value	Unit
Storage Temperature		-65 to +125	°C
Plastic Packages		-65 to +125	°C
Ambient Temperature With Power Applied		-55 to +125	°C
Output Short Circuit Current[1]		200	mA
Voltage with Respect to Ground	A9, OE#, Reset# [2]	-0.5 to +11.5	V
	All other pins [3]	-0.5 to Vcc+0.5	V
	Vcc	-0.5 to +4.0	V

Notes:
1. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.
2. Minimum DC input voltage on A9, OE#, RESET# pins is –0.5V. During voltage transitions, A9, OE#, RESET# pins may undershoot V_{ss} to –1.0V for periods of up to 50ns and to –2.0V for periods of up to 20ns. See figure below. Maximum DC input voltage on A9, OE#, and RESET# is 11.5V which may overshoot to 12.5V for periods up to 20ns.
3. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may undershoot V_{ss} to –1.0V for periods of up to 50ns and to –2.0 V for periods of up to 20ns. See figure below. Maximum DC voltage on output and I/O pins is V_{cc} + 0.5 V. During voltage transitions, outputs may overshoot to V_{cc} + 1.5 V for periods up to 20ns. See figure below.
4. Stresses above the values so mentioned above may cause permanent damage to the device. These values are for a stress rating only and do not imply that the device should be operated at conditions up to or above these values. Exposure of the device to the maximum rating values for extended periods of time may adversely affect the device reliability.

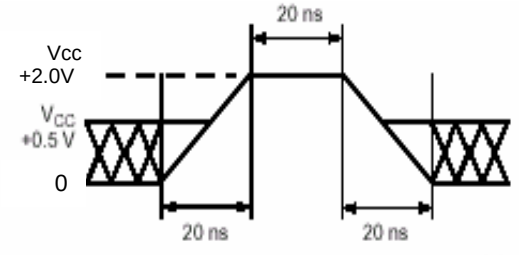
RECOMMENDED OPERATING RANGES[1]

Parameter	Value	Unit
Ambient Operating Temperature Commercial Devices Industrial Devices	0 to 70 -40 to 85	°C
Operating Supply Voltage Vcc	Regulated:2.0 to 2.2	V
	Full: 1.65 to 2.2	

1. Recommended Operating Ranges define those limits between which the functionality of the device is guaranteed.



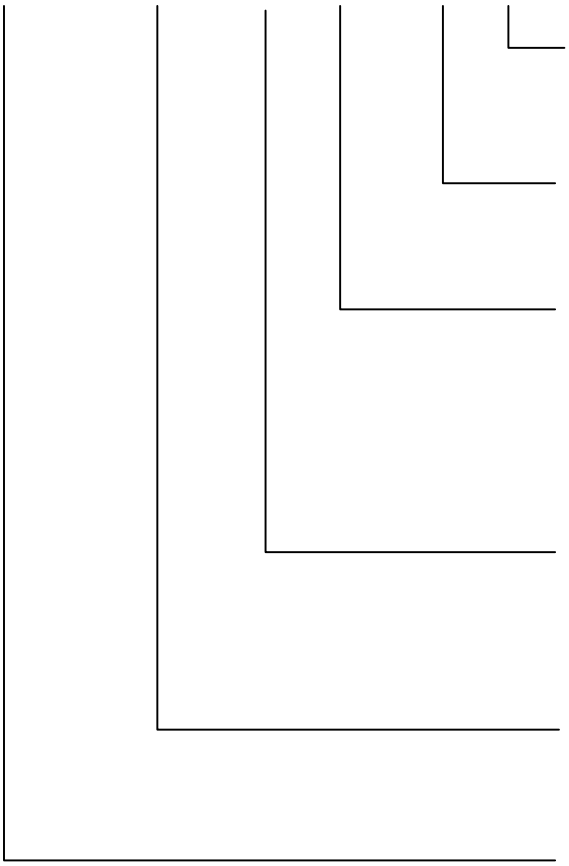
Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform

ORDERING INFORMATION

EN29SL800 T - 70 T C P



PACKAGING CONTENT
(Blank) = Conventional
P = Pb Free

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (-40°C to +85°C)

PACKAGE
T = 48-pin TSOP
B = 48-Ball Fine Pitch Ball Grid Array (FBGA)
0.80mm pitch, 6mm x 8mm package
M = 48-Ball Very-Very-Thin-Profile Fine Pitch
Ball Grid Array (WFBGA)
0.50mm pitch, 5mm x 6mm package
K = 48-Ball Very-Very-Thin-Profile Fine Pitch
Land Grid Array (WLGA)

SPEED
70 = 70ns
90 = 90ns

BOOT CODE SECTOR ARCHITECTURE
T = Top Sector
B = Bottom Sector

BASE PART NUMBER
EN = Eon Silicon Solution Inc.
29SL = FLASH, 1.8V Read Program Erase
800 = 8 Megabit (1024K x 8 / 512K x 16)

Revisions List

Revision No	Description	Date
A	Initial Release	2005/06/15
B	1 Change the FBGA package dimension to enhance the BGA substrate and ball strength i. Package Thickness A : 1.10 mm to 1.31 mm ii. Ball size b : 0.3 mm to 0.4 mm 2 TSOP package dimension change R from 0.08 mm max. to 0.08~0.20 mm 3 Remove ,Unlock Bypass, Unlock Bypass Program, and Unlock Bypass Reset, commands from Table 9. 4 Remove description of Unlock Bypass 5 Remove regulated voltage version and description 6 Correct manufacturer-id value in table 5, page 11 7 Modify test condition parameters in page 24,27 for 70ns read operation i. Vcc=1.7-2.2 V ii. Output Load 15pF iii. Input / Output reference level 1/2 Vcc	2006/04/14
C	1. Added WFBGA package option in page 1 2. Added WFBGA connection diagram in page 3 3. Added Figure 16 of WFBGA drawing in page 39 4. Added package code M for WFBGA in page 41 5. Changed typical active read current from 7 to 15 mA in page 1 6. Changed I_{CC1} typical from 7 to 15 mA; I_{CC1} max from 15 to 30 mA in Table 7 of page 24	2006/09/07
D	1. Added WLGA package option in page 1 2. Added WLGA connection diagram in page 3 3. Added Figure 17 of WLGA drawing in page 40 4. Added package code K for WLGA in page 42	2006/11/06