CHERRY SEMICONDUCTOR

CS-1525A/CS-1527A
CS-2525A/CS-2527A
## CS-3525A/CS-3527A
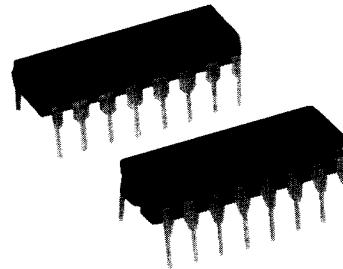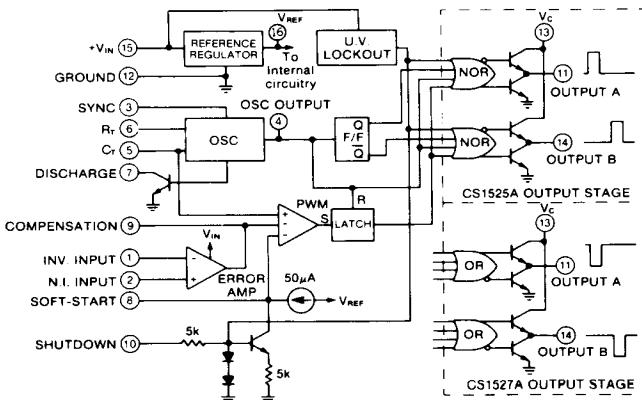
PULSE WIDTH MODULATOR CONTROL CIRCUIT
DUAL-NOR/DUAL-OR TOTEM POLE OUTPUTS

DESCRIPTION

The CS1525A/1527A series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used to implement all types of switching power supplies. The on-chip +5.1 volt reference is trimmed to ±1% initial accuracy and the input common-mode range of the error amplifier includes the reference voltage, eliminating external potentiometers and divider resistors. A Sync input to the oscillator allows multiple units to be slaved together, or a single unit to be synchronized to an external system clock. A single resistor between the C_T pin and the Discharge pin provides a wide range of deadtime adjustment. These devices also feature built-in soft-start circuity with only a timing capacitor required externally. A Shutdown pin controls both the soft-start circuitry and the output stages, providing instantaneous turn-off with soft-start recycle for slow turn-on. These functions are also controlled by an under-voltage lockout which keeps the outputs off and the soft-start capacitor discharged for input voltages less than that required for normal operation. Another unique feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200mA. The CS1525A output stage features NOR logic, giving a LOW output for an OFF state. The CS1527A utilizes OR logic which results in a HIGH output level when OFF.
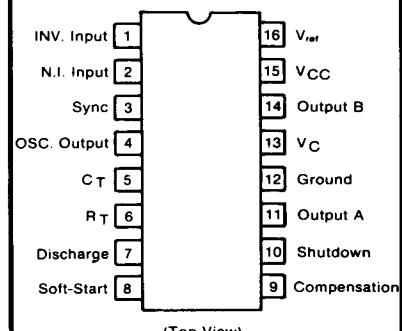
FEATURES:

- 8 to 35V operation
- 5.1V reference trimmed to ±1%
- 100Hz to 500kHz oscillator range
- Separate oscillator sync terminal
- Adjustable deadtime control
- Internal soft-start
- Input undervoltage lockout
- Latching PWM to prevent multiple pulses
- Dual source/sink output drivers

PIN CONNECTIONS

INV. Input	1	16	V_{ref}
N.I. Input	2	15	V_{CC}
Sync	3	14	Output B
OSC. Output	4	13	V_C
C_T	5	12	Ground
R_T	6	11	Output A
Discharge	7	10	Shutdown
Soft-Start	8	9	Compensation

(Top View)

BLOCK DIAGRAM

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ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, (+V$_{IN}$) .... +40V
Collector Supply Voltage (V$_C$) .... +40V
Logic Inputs .... -0.3V to +5.5V
Analog Inputs .... -0.3V to +V$_{IN}$
Output Current, Source or Sink 500mA
Reference Output Current 50mA
Oscillator Charging Current 5mA
Power Dissipation at T$_A$ = +25°C (Note 2) 1000mW
Thermal Resistance, Junction to Ambient .... 100°C/W
Power Dissipation at T$_C$ = +25°C (Note 3) 2000mW
Thermal Resistance, Junction to Case .... 60°C/W
Operating Junction Temperature .... -55°C to +150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) .... +300°C

Notes 1. Values beyond which damage may occur.
    2. Derate at 10mW/°C for ambient temperatures above +50°C.
    3. Derate at 16mW/°C for case temperatures above +25°C.

RECOMMENDED OPERATING CONDITIONS (Note 4)

Input Voltage (+V$_{IN}$) .... +8V to +35V
Collector Supply Voltage (V$_C$) .... +4.5V to +35V
Sink/Source Load Current (steady state)............ 0 to 100mA
Sink/Source Load Current (peak) .... 0 to 400mA
Reference Load Current .... 0 to 20mA
Oscillator Frequency Range .... 100Hz to 400kHz
Oscillator Timing Resistor ....2kΩ to 150kΩ
Oscillator Timing Capacitor ....001μF to 0.1μF
Dead Time Resistor Range .... 0 to 500Ω
Operating Ambient Temperature Range
    CS1525A, CS1527A ....-55°C to +125°C
    CS2525A, CS2527A ....-25°C to +85°C
    CS3525A, CS3527A ....0°C to +70°C

Notes 4. Range over which the device is functional and parameter limits
    are guaranteed.

ELECTRICAL CHARACTERISTICS (+V$_{IN}$ = 20V, and over operating temperature, unless otherwise specified)

PARAMETER	TEST CONDITIONS	CS1525A/CS2525A CS1527A/CS2527A			CS3525A CS3527A			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T$_A$ = 25°C	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	V$_{IN}$ = 8 to 35V		10	20		10	20	mV
Load Regulation	I$_L$ = 0 to 20mA		20	50		20	50	mV
Temperature Stability (Note 5)	Over Operating Range		20	50		20	50	mV
Total Output Variation (Note 5)	Line, Load and Temperature	5.00		5.20	4.95		5.25	V
Short Circuit Current	V$_{REF}$ = 0, T$_A$ = 25°C		80	100		80	100	mA
Output Noise Voltage (Note 5)	10Hz ≥ f ≥ 10kHz, T$_A$ = 25°C		40	200		40	200	μVrms
Long Term Stability (Note 5)	T$_A$ = 125°C, 1000 Hrs.		20	50		20	50	mv
Oscillator Section (Note 6)								
Initial Accuracy (Note 5 & 6)	T$_A$ = 25°C		±2	±6		±2	±6	%
Voltage Stability (Note 5 & 6)	V$_{IN}$ = 8 to 35V		±0.3	±1		±1	±2	%
Temperature Stability (Note 5)	Over Operating Range		±3	±6		±3	±6	%
Minimum Frequency	R$_T$ = 150kΩ, C$_T$ = 0.1μF		100			100		Hz
Maximum Frequency	R$_T$ = 2kΩ, C$_T$ = 1nF	400			400			kHz
Current Mirror	I$_{RT}$ = 2mA	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude (Note 5 & 6)		3.0	3.5		3.0	3.5		V
Clock Width (Note 5 & 6)	T$_A$ = 25°C	0.3	0.5	1.0	0.3	0.5	1.0	μs
Sync Threshold		1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current	Sync Voltage = 3.5V		1.0	2.5		1.0	2.5	mA
Error Amplifier Section (V$_{CM}$ = 5.1V)								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	10		1	10	μA
Input Offset Current				1			1	μA
DC Open Loop Gain	R$_L$ ≥ 10 Meg Ω	60	75		60	75		dB
Gain-Bandwidth Product (Note 5)	A$_V$ = 0dB, T$_A$ = 25°C	1	2		1	2		MHz
Output Low Level			0.2	0.5		0.2	0.5	V
Output High Level		3.8	5.6		3.8	5.6		V
Common Mode Rejection	V$_{CM}$ = 1.5 to 5.2V	60	75		60	75		dB
Supply Voltage Rejection	V$_{IN}$ = 8 to 35V	50	60		50	60		dB

Notes 5. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
    6. Tested at f$_{OSC}$ = 40khz (R$_T$ = 3.6kΩ, C$_T$ = .01μF, R$_D$ = 0Ω).

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ELECTRICAL CHARACTERISTICS (+V_{IN} = 20V, and over operating temperature, unless otherwise specified)

PARAMETER	TEST CONDITIONS	CS1525A/CS2525A CS1527A/CS2527A			CS3525A CS3527A			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
PWM Comparator								
Minimum Duty-Cycle				0			0	%
Maximum Duty-Cycle		45	49		45	49		%
Input Threshold (Note 6)	Zero Duty-Cycle	0.6	0.9		0.6	0.9		V
Input Threshold (Note 6)	Maximum Duty-Cycle		3.3	3.6		3.3	3.6	V
Input Bias Current (Note 5)			.05	1.0		.05	1.0	μA
Soft-Start Section								
Soft Start Current	$V_{SHUTDOWN}$ = 0V	25	50	80	25	50	80	μA
Soft Start Voltage	$V_{SHUTDOWN}$ = 2V		0.4	0.6		0.4	0.6	V
Shutdown Input Current	$V_{SHUTDOWN}$ = 2.5V		0.4	1.0		0.4	1.0	mA
Output Drivers (Each Output) (V_C = 20V)								
Output Low Level	I_{SINK} = 20mA		0.2	0.4		0.2	0.4	V
	I_{SINK} = 100mA		1.0	2.0		1.0	2.0	V
Output High Level	I_{SOURCE} = 20mA	18	19		18	19		V
	I_{SOURCE} = 100mA	17	18		17	18		V
Undervoltage Lockout	V_{COMP} and V_{SS} = High	6	7	8	6	7	8	V
Collector Leakage (Note 7)	V_C = 35V			200			200	μA
Rise Time (Note 5)	C_L = 1nF, T_A = 25°C		100	600		100	600	ns
Fall Time (Note 5)	C_L = 1nf, T_A = 25°C		50	300		50	300	ns
Shutdown Delay (Note 5)	V_{SD} = 3V, C_s = 0, T_A = 25°C		0.2	0.5		0.2	0.5	μs
Total Standby Current								
Supply Current	V_{IN} = 35V		14	20		14	20	mA

Notes 5. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
     6. Tested at f_{OSC} = 40khz (R_T = 3.6kΩ, C_T = .01μF, R_D = 0Ω).
     7. Applies to CS1525A/2525A/3525A only, due to polarity of output pulses.

APPLICATION INFORMATION

Shutdown Options (see block diagram, front page)

1. An external open collector comparator or transistor can be used to pull down the Compensation pin (9). This will set the PWM latch and turn off both outputs. Pulse-by-pulse protection can be accomplished if the shutdown signal is momentary, since the PWM latch will be reset with each clock pulse.

2. Shutdown can also be accomplished by pulling down on the SOFT-START pin (8). When using this approach, shutdown will not affect the amplifier compensation network; however, if a SOFT-START capacitor is used, it must be discharged, possibly slowing shutdown response

3. Applying a positive-going signal to the Shutdown pin (10) will provide the most rapid shutdown of the out-puts if a soft-start capacitor is not used at Pin 8. An external soft-start capacitor at Pin 8 will slow shutdown response due to the discharge time of the soft-start capacitor. Discharge current is approximately twice the charging current.

4. The shutdown terminal can be used to set the PWM latch on a pulse-by-pulse basis if there is no external capacitance on Pin 8. Soft-start characteristics may still be accomplished by applying an external capacitor, blocking diode and charging resistor to the Compensation Pin (9).

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FIGURE 1—OSCILLATOR SCHEMATIC
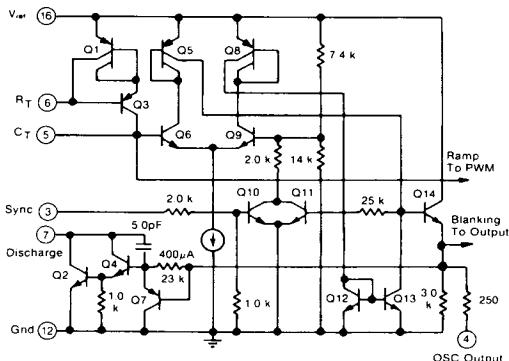
FIGURE 2—OSCILLATOR CHARGE TIME versus R_T
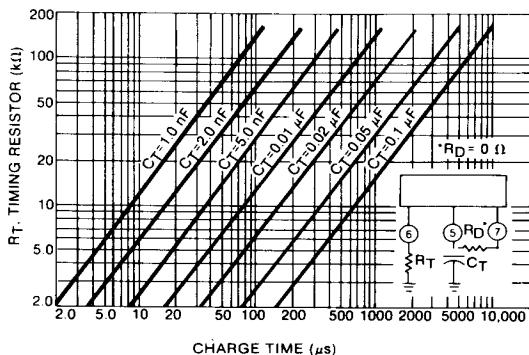
FIGURE 3—OSCILLATOR DISCHARGE TIME versus R_D
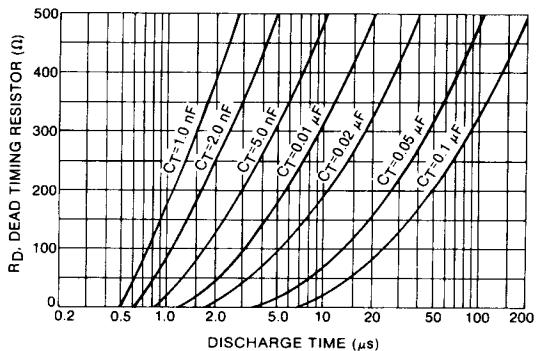
FIGURE 4— ERROR AMPLIFIER SCHEMATIC
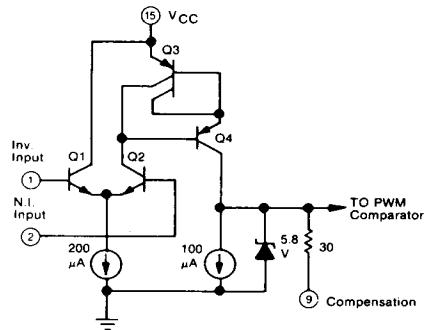
FIGURE 5—ERROR AMPLIFIER OPEN-LOOP FREQUENCY RESPONSE
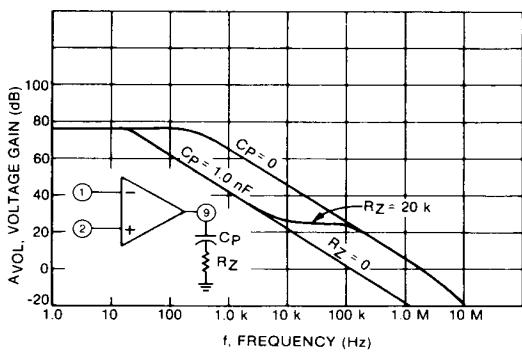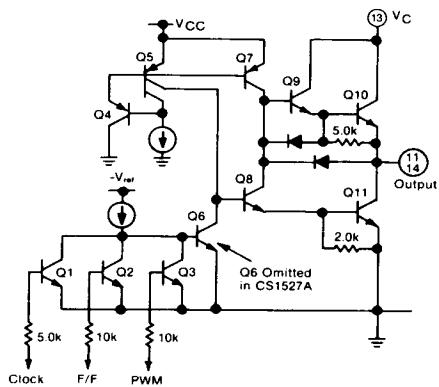
FIGURE 6—OUTPUT CIRCUIT (1/2 CIRCUIT SHOWN)

**FIGURE 7—CS1525A/2525A/3525A
OUTPUT SATURATION CHARACTERISTICS**
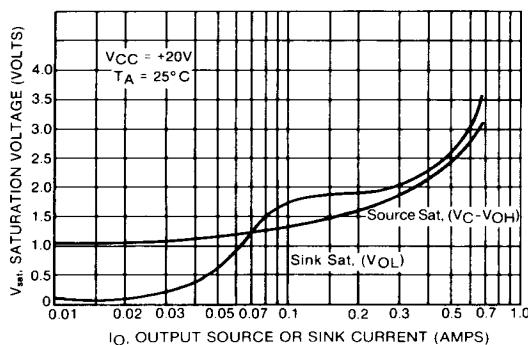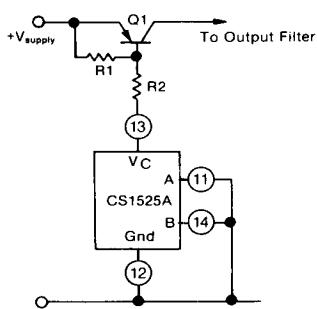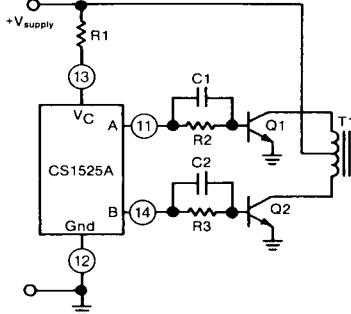

FIGURE 8—SINGLE ENDED SUPPLY
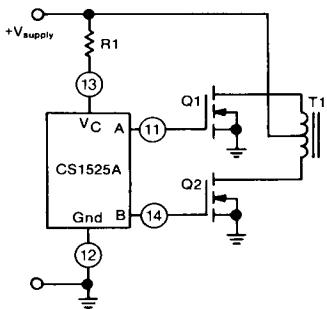
For single-ended supplies, the driver outputs are grounded. The VC terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

FIGURE 9—PUSH-PULL CONFIGURATION
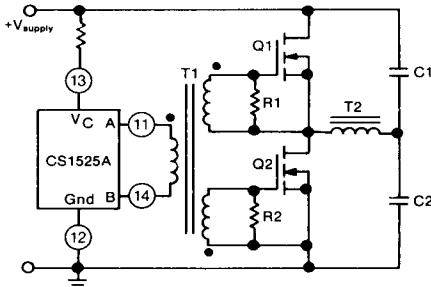
In conventional push-pull bipolar designs, forward base drive is controlled by R1-R3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C1 and C2.

FIGURE 10—DRIVING POWER FETS
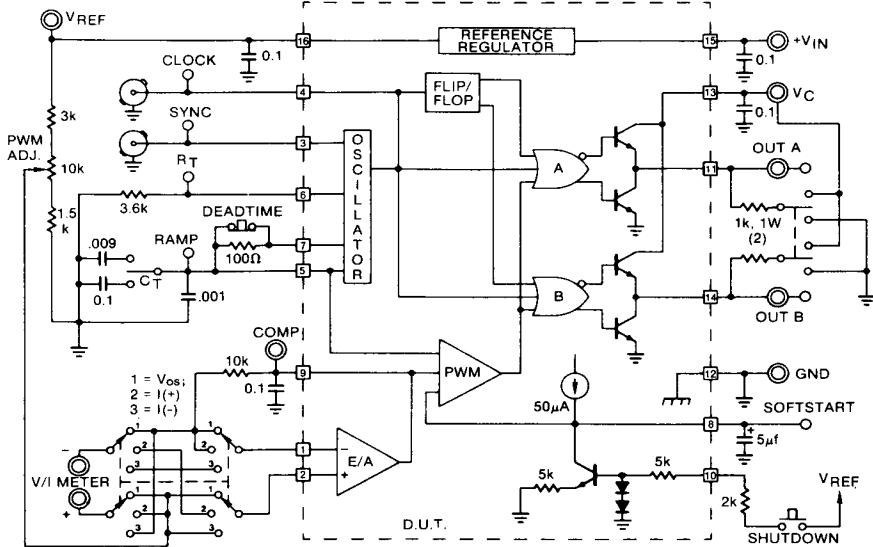

The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.
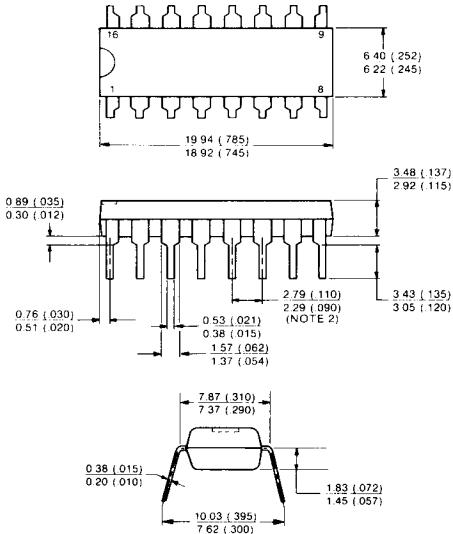
**FIGURE 11—DRIVING TRANSFORMERS IN A
HALF-BRIDGE CONFIGURATION**

Low power transformers can be driven directly by the CS1525A. Automatic reset occurs during deadtime, when both ends of the primary winding are switched to ground.

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CS1525A/1527A LAB TEST FIXTURE schematic:

- V_{REF} — REFERENCE REGULATOR — 16 — 0.1 — 15 — +V_{IN} — 0.1
- CLOCK — 4 — FLIP/FLOP — 13 — V_C — 0.1
- SYNC — 3
- 3k
- PWM ADJ. — 10k
- R_T — 6 — OSCILLATOR — A — 11 — OUT A
- 1.5 k — 3.6k
- DEADTIME — 7 — 100Ω
- .009 — RAMP
- C_T — 5 — .001 — B — 14 — OUT B
- 0.1
- 1k, 1W (2)
- COMP — 9 — PWM
- 10k — 0.1
- 1 = V_{os}; 2 = I(+); 3 = I(-)
- V/I METER — 1 — E/A — 2
- 50µA
- 12 — GND
- SOFTSTART — 8 — 5µf
- 5k — 5k — 2k — V_{REF}
- 10 — SHUTDOWN
- D.U.T.
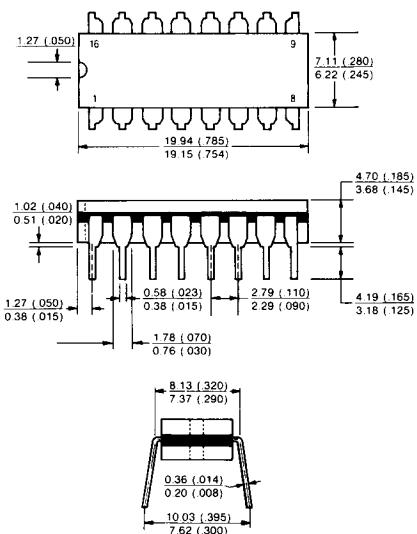
CS-2525A, CS-3525A
CS-2527A, CS-3527A
MECHANICAL SPECIFICATIONS: PLASTIC
16 PIN N PACKAGE

6.40 (.252) / 6.22 (.245)
19.94 (.785) / 18.92 (.745)
3.48 (.137) / 2.92 (.115)
0.89 (.035) / 0.30 (.012)
2.79 (.110) / 2.29 (.090) (NOTE 2)
3.43 (.135) / 3.05 (.120)
0.76 (.030) / 0.51 (.020)
0.53 (.021) / 0.38 (.015)
1.57 (.062) / 1.37 (.054)
7.87 (.310) / 7.37 (.290)
0.38 (.015) / 0.20 (.010)
1.83 (.072) / 1.45 (.057)
10.03 (.395) / 7.62 (.300)

NOTES:
1. DIMENSIONS SHOWN ARE IN MILLIMETERS. THOSE IN PARENTHESES ARE IN INCHES.
2. TOLERANCES ARE NON-ACCUMULATIVE.

CS-1525A, CS-2525A, CS-3525A
CS-1527A, CS-2527A, CS-3527A
MECHANICAL SPECIFICATIONS: CERAMIC (CERDIP)
16 PIN J PACKAGE

1.27 (.050)
7.11 (.280) / 6.22 (.245)
19.94 (.785) / 19.15 (.754)
4.70 (.185) / 3.68 (.145)
1.02 (.040) / 0.51 (.020)
0.58 (.023) / 0.38 (.015)
2.79 (.110) / 2.29 (.090)
4.19 (.165) / 3.18 (.125)
1.27 (.050) / 0.38 (.015)
1.78 (.070) / 0.76 (.030)
8.13 (.320) / 7.37 (.290)
0.36 (.014) / 0.20 (.008)
10.03 (.395) / 7.62 (.300)

NOTES:
1. DIMENSIONS SHOWN ARE IN MILLIMETERS. THOSE IN PARENTHESES ARE IN INCHES.
2. TOLERANCES ARE NON-ACCUMULATIVE.

CHERRY SEMICONDUCTOR

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