µP Supervisory Circuits

HALOGEN FREE LEAD FREE™ RoHS Compliance

FEATURES

- **Accurate under voltage system monitoring**
- **$\overline{\text{RESET}}$ guaranteed valid for V_{CC} = 1.0V**
- **6µA supply current**
- **200ms RESET pulse width**
- **Watchdog timer function 1.6 sec timeout**
- **Brownout detection system reset for use with 3.0, 3.6, and 5.0 volt systems**
- **Pin and function compatible with the MAX705/706/813L products**
- **Operating Range from -40°C to +85°C**
- **Available in SOIC 8-lead and MSOP 8-lead packages**

APPLICATIONS

- **Microprocessor and microcontroller based systems**
- **Intelligent instruments**
- **Control systems**
- **Critical µP monitors**
- **Portable equipment**

DESCRIPTION

The CAT705, CAT706, and CAT813 provide reset and monitoring functions for the electronic systems. Each device monitors the system voltage and maintains a reset output until that voltage reaches the device's specified trip value and then maintains the reset output active condition until the device's internal timer allows the system power supply to stabilize.

The CAT705, CAT706, and CAT813 have a watchdog input which can be used to monitor a system signal and cause a reset to be issued if the signal fails to change state prior to a timeout condition.

The CAT705 and CAT706 provide a manual $\overline{\text{RESET}}$ input which initiate reset if pulled low. The CAT705, CAT706 and CAT813 provide a RESET output which is low for the CAT705 and CAT706, but high for the CAT813.

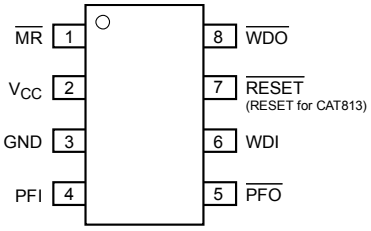
There is a secondary supply monitor included for power-fail warning (pin PFI).

The CAT706 has a threshold voltage 4.40V. The CAT705/ CAT813 have a threshold voltage of 4.65V.

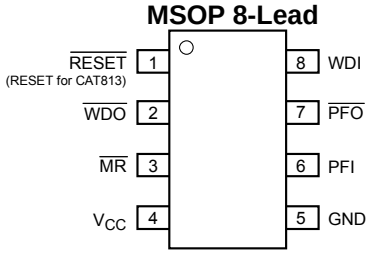
For Ordering Information details, see page 13.

PIN CONFIGURATION

SOIC 8-Lead



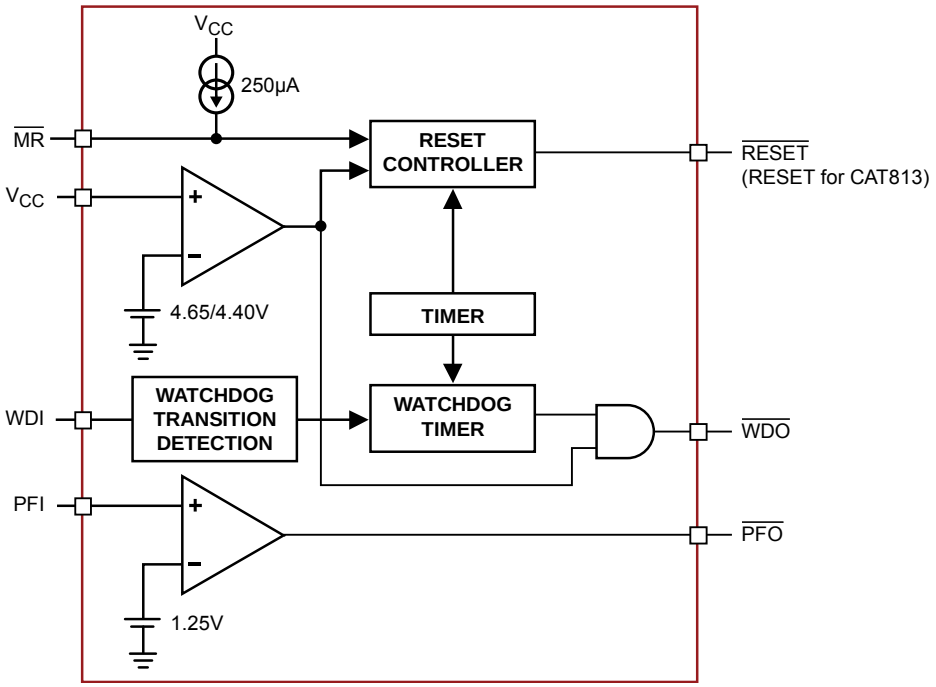
MSOP 8-Lead



PIN FUNCTIONS

Pin Name	Function
$\overline{\text{MR}}$	Manual Reset input
V_{CC}	Power Supply
GND	Ground
PFI	Power Fail voltage monitor Input.
$\overline{\text{PFO}}$	Power Fail Output
WDI	Watchdog Timer Input
$\overline{\text{RESET}}$	CMOS Push-Pull Active Low Reset Output (CAT705 & CAT706)
RESET	CMOS Push-Pull Active High Reset Output (CAT813)
$\overline{\text{WDO}}$	Watchdog Timer Output

BLOCK DIAGRAM



Device	RESET	RESET	MR	WDI	WDO	PFI
CAT705	@ 4.65 V		x	x	x	@ 1.25 V
CAT706	@ 4.40 V		x	x	x	@ 1.25 V
CAT813		@ 4.65 V	x	x	x	@ 1.25 V

ABSOLUTE MAXIMUM RATINGS[1]

Parameters	Ratings	Units
Supply Voltage	6.5	V
All other pins	-0.3 to (V_{CC} + 0.3)	V
Output Current RST, $\overline{RST}$,$\overline{WDO}$	20	mA
Continuous Power Dissipations (T_A = +70ºC)		
SOIC 8-lead (derate 5.9mW/ºC above +70ºC)	471	mW
MSOP 8-lead (derate 4.1mW/ºC above +70ºC)	330	
Storage Temperature	-65 to 150	ºC
Lead Soldering (10 seconds max)	+300	ºC
ESD Rating: Human Body Model	2000	V
ESD Rating: Machine Model	200	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Range	Units
V_{CC} (T_A = -40ºC to +85ºC)	1.2 to 5.5	V
All Other Pins	-0.1 to (V_{CC} + 0.1)	V
Ambient Temperature	-40 to +85	ºC

Notes:

(1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

ELECTRICAL OPERATING CHARACTERISTICS

V_{CC} = 4.5V to 5.5V for CAT705, CAT706, CAT813 versions;
V_{CC} = 3.0V to 3.6V for the CAT706 R/S/T versions,
-40ºC ≤ T_A ≤ +85ºC unless otherwise noted.
Typical values at T_A = 25ºC and V_{CC} = 5V for CAT705, CAT706 versions;
V_{CC} = 3.3V for the CAT706 T/S versions; V_{CC} = 3.0V for the CAT706 R version.(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current	CAT705 CAT706 CAT813		6	17	µA
		CAT706 (R/S/T Versions)		4	12	µA
V_{RST}	Reset Threshold	CAT705 & CAT813 at -40ºC ≤ T_A ≤ +85ºC	4.50	4.65	4.75	V
		CAT706 at -40ºC ≤ T_A ≤ +85ºC	4.25	4.40	4.50	V
		CAT706T at -40ºC ≤ T_A ≤ +85ºC	3.00	3.08	3.15	V
		CAT706S at -40ºC ≤ T_A ≤ +85ºC	2.85	2.93	3.00	V
		CAT706R at -40ºC ≤ T_A ≤ +85ºC	2.55	2.63	2.70	V
	Reset Threshold Tempco			40		ppm/ºC
	Reset Threshold Hysteresis	CAT705 & CAT813		10		mV
		CAT706		5		mV
t_{RD}	V_{CC} to Reset Delay(2)	V_{CC} = V_{TH} to (V_{TH} - 100mV)		20		µs
t_{RP}	Reset Active Timeout Period		140	200	400	ms
V_{OH}	$\overline{\text{RESET}}$ Output High Voltage	CAT705 & CAT706, V_{CC} = $V_{RST\ max}$, I_{SOURCE} = -120µA	V_{CC} - 1.5V			V
		CAT705 & CAT706, V_{CC} = $V_{RST\ max}$, I_{SOURCE} = -30µA	0.8 x V_{CC}			
V_{OL}	$\overline{\text{RESET}}$ Output Low Voltage	CAT705 & CAT706, V_{CC} = $V_{RST\ min}$, I_{SINK} = 3.2mA			0.4	
		CAT705 &CAT706, V_{CC} = 1.2V I_{SINK} = 100µA			0.3	
V_{OH}	RESET Output High Voltage	CAT813, V_{CC} = $V_{RST\ max}$, I_{SOURCE} = -120µA	V_{CC} - 1.5V			V
		CAT813, V_{CC} = $V_{RST\ max}$, I_{SOURCE} = -30µA	0.8 x V_{CC}			
V_{OL}	RESET Output Low Voltage	CAT813, V_{CC} = $V_{RST\ min}$, I_{SINK} = 3.2mA			0.4	V
		CAT813, V_{CC} = 1.2V I_{SINK} = 100µA			0.3	

Notes:
(1) Over-temperature limits are guaranteed by design and not production tested.
(2) The RESET short-circuit current is the maximum pull-up current when reset is driven low by a bidirectional output.

ELECTRICAL OPERATING CHARACTERISTICS (continued)

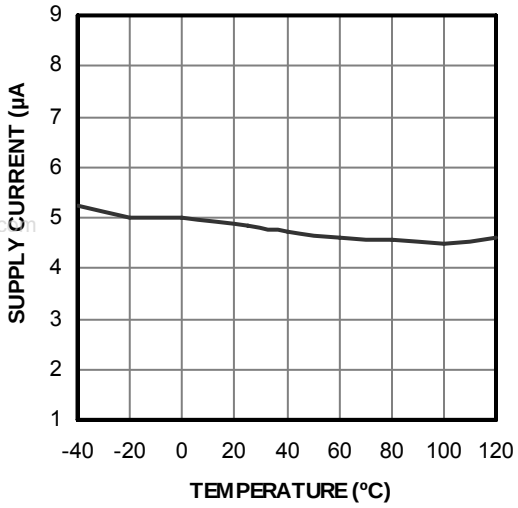
V_{CC} = 4.50V to 5.5V for CAT705, CAT706 & CAT813 versions;
V_{CC} = 3.0V to 3.6V for the CAT706 R/S/T version,
-40°C ≤ T_A ≤ +85°C unless otherwise noted.
Typical values at T_A = 25°C and V_{CC} = 5V for CAT705, CAT706, & CAT813 versions;
V_{CC} = 3.3V for the CAT706 T/S versions; V_{CC} = 3.0V for the CAT706 R version.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
WATCHDOG INPUT (CAT705, CAT706 & CAT813)						
t_{WD}	Watchdog Timeout Period		1.00	1.60	2.25	s
t_{WDI}	WDI Pulse Width	V_{IL} = 0.4V, V_{IH} = 0.8 x V_{CC}	50			ns
V_{IL}	WDI Input Voltage[3]				0.3 x V_{CC}	V
V_{IH}			0.7 x V_{CC}			
	WDI Input Current[4]	WDI = V_{CC}, Time Average		50	150	µA
		WDI = 0V, Time Average	-150	-50		
	WDO Output Voltage	I_{SOURCE} = -800µA	V_{CC} – 1.5	V_{CC} – 0.25		V
		I_{SINK} = 1.2mA		0.1	0.4	
MANUAL RESET INPUT(CAT705, CAT706 & CAT813)						
V_{IL}	$\overline{MR}$ Input Voltage				0.3 x V_{CC}	V
V_{IH}			0.7 x V_{CC}			
	$\overline{MR}$ Pull-up Current	$\overline{MR}$ = 0V	40	70	140	µA
t_{PB}	$\overline{MR}$ Pulse Width		1			µs
t_{PDLY}	$\overline{MR}$ low to Reset Delay[5]				5	µs
	PFI Input Threshold	V_{CC} = 5V	1.2	1.25	1.3	V
	PFI Input Current		-25	0.01	25	nA
	$\overline{PFO}$ Output Voltage	I_{SOURCE} = -800µA	V_{CC} - 1.5V			V
		I_{SINK} = 3.2mA			0.4	V

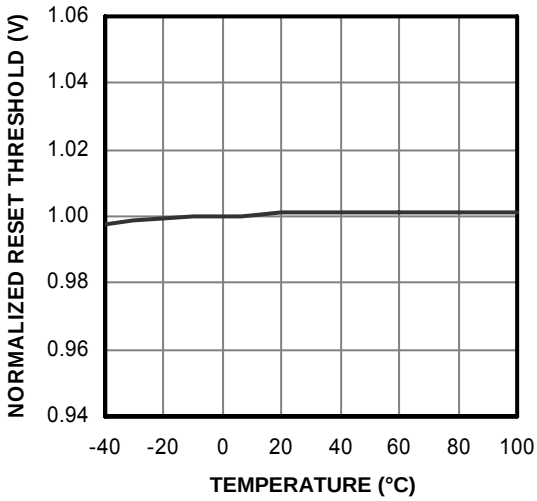
Notes:
(3) WDI is internally serviced within the watchdog period if WDI is left open.
(4) The WDI input current is specified as an average input current when the WDI input is driven high or low. The WDI input if connected to a three-stated output device can be disabled in the tristate mode as long as the leakage current is less than 10µA and a maximum capacitance of less than 200pF. To clock the WDI input in the active mode the drive device must be able to source or sink at least 200µA when active.
(5) $\overline{RESET}$ for CAT705 & CAT706 & RESET for CAT813.

TYPICAL ELECTRICAL OPERATING CHARACTERISTICS TABLES

V_{CC} Supply Current vs. Temperature



Normalized Reset Threshold Voltage vs. Temperature



FUNCTIONAL DESCRIPTION

PROCESSOR RESET

The CAT705, CAT706 & CAT813 detect supply voltage (V_{CC}) conditions that are below the specified voltage trip value (V_{RST}) and provide a reset output to maintain correct system operation. On power-up, $\overline{\text{RESET}}$ (or RESET for the CAT813) are kept active for a minimum delay t_{RP} of 140ms after the supply voltage (V_{CC}) rises above V_{RST} to allow the power supply and processor to stabilize. When V_{CC} drops below the voltage trip value (V_{RST}), the reset output signals $\overline{\text{RESET}}$ (or RESET) are pulled active. $\overline{\text{RESET}}$ (or RESET) is specifically designed to provide the reset input signals for processors. This provides reliable and consistent operation as power is turned on, off or during brownout conditions by maintaining the processor operation in known conditions.

MANUAL RESET

The CAT705, CAT706 & CAT813 each have a Manual Reset ($\overline{\text{MR}}$) input to allow for alternative control of the reset outputs. The $\overline{\text{MR}}$ input is designed for direct connection to a pushbutton (see Figure 1). The $\overline{\text{MR}}$ input is internally pulled up by 52kΩ resistor and must be pulled low to cause the reset outputs to go active. Internally, this input is debounced and timed such that $\overline{\text{RESET}}$ (or RESET) signals of at least 140ms minimum will be generated. The min 140ms t_{RP} delay commences as the Manual Reset input is released from the low level. (see Figure 2)

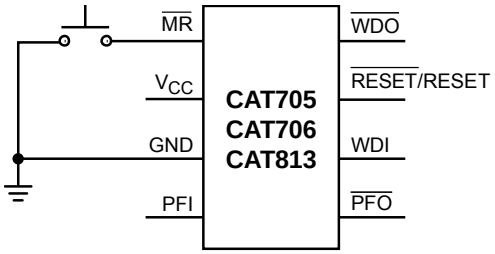


Figure 1. Pushbutton RESET

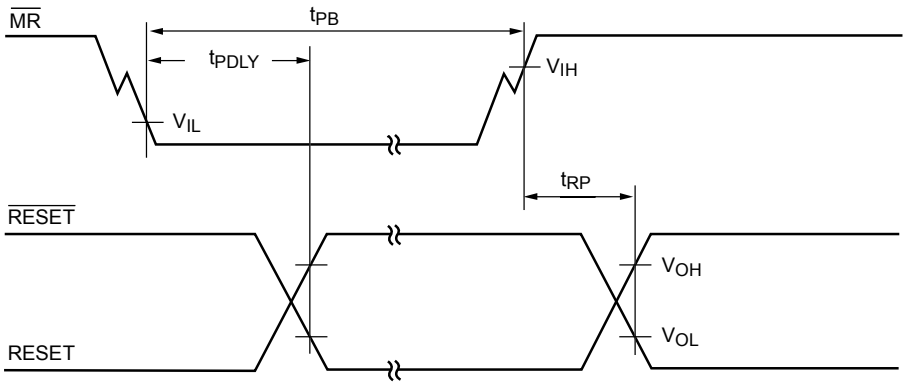


Figure 2. Timing Diagram – Pushbutton RESET

WATCHDOG TIMER

The CAT705, CAT706, & CAT813 provide a Watchdog input (WDI). The watchdog timer function forces $\overline{\text{RESET}}$ (and RESET in the CAT813) signals active when the WDI input does not have a transition from low-to-high or high-to-low within 1.12 seconds. Timeout of the watchdog starts when $\overline{\text{RESET}}$ (RESET on the CAT813) becomes inactive. If a transition occurs on the WDI input pin prior to the watchdog time-out, the watchdog timer is reset and begins to time-out again. If the watchdog timer is allowed to time-out, then the reset output(s) will go active for t_{RP} and once released will repeat the watchdog timeout process.

Figure 3 below shows a typical implementation of a watchdog function. Any processor signal that repeats dependant on the normal operation of the processor or directed by the software operating on the processor can be used to strobe the watchdog input. The most reliable is a dedicated I/O output transitioned by a specific software instruction.

The watchdog can be disabled by floating (or tri-stating) the WDI input (see Figure 4). If the watchdog is disabled the WDI pin will be pulled low for the first 7/8th's of the watchdog period (t_{WD}) and pulled high for the last 1/8th of the watchdog period. This pulling low of the WDI input and then high is used to detect an open or tri-state condition and will continue to repeat until the WDI input is driven high or low.

For most efficient operation of devices with the watchdog function the WDI input should be held low the majority of the time and only strobed high as required to reset the watchdog timer.

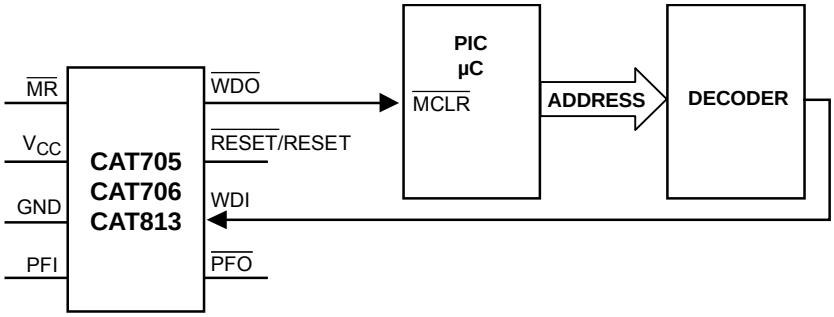


Figure 3. Watchdog Timer

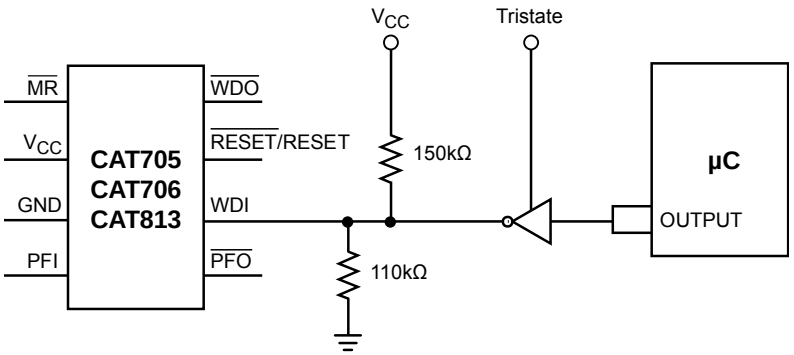


Figure 4. Watchdog Disable Circuit

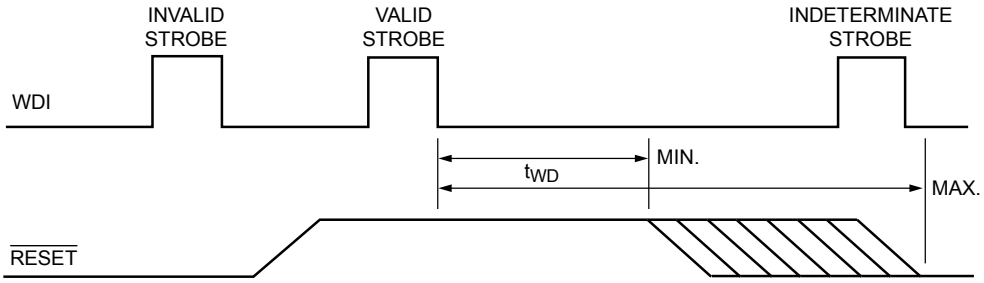


Figure 5. Timing Diagram – Strobe Input

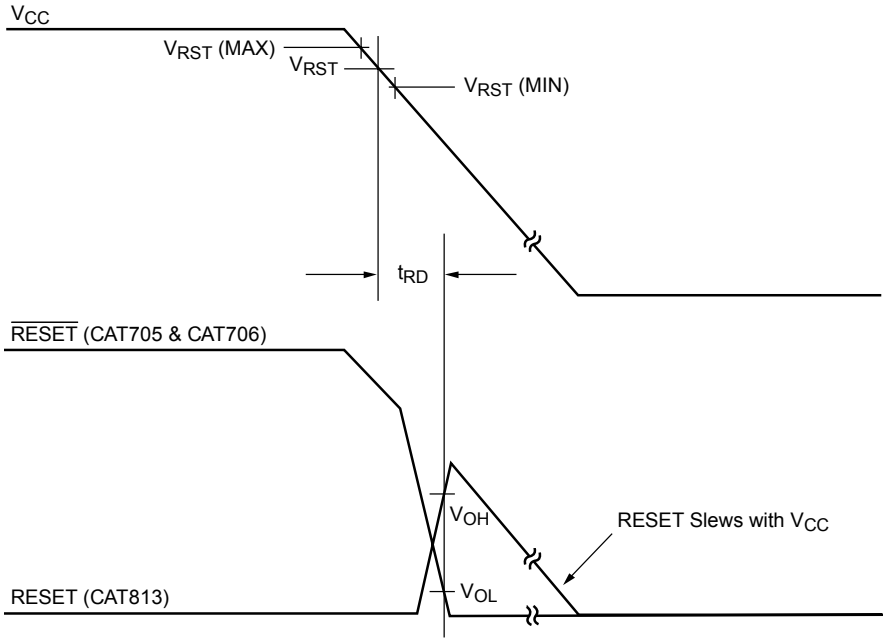


Figure 6. Timing Diagram – Power Down

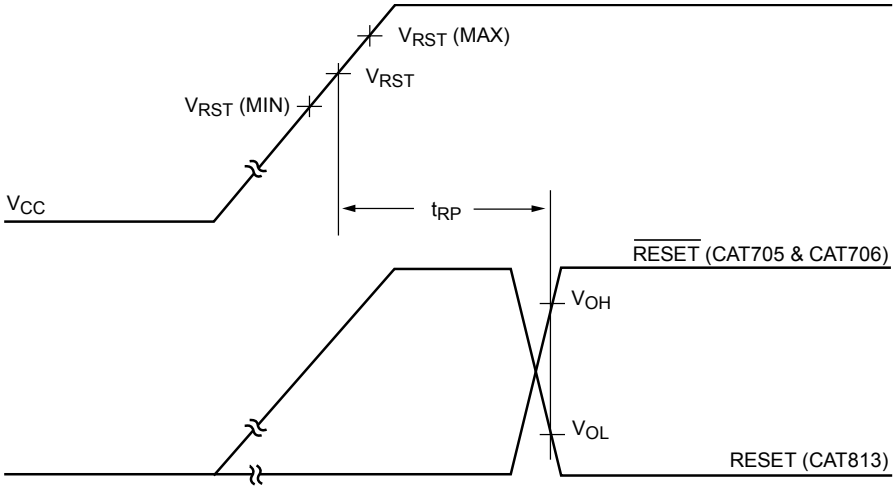


Figure 7. Timing Diagram – Power Up

APPLICATION NOTES

µP's with Bidirectional Reset Pins

The $\overline{\text{RESET}}$ output can be pulled low by processors like the 68HC11 allowing for a system reset issued by the processor. The maximum pullup current that can be sourced by the CAT705 & CAT706 1.5mA (and by the CAT706 T/R/S is 800µA) allowing the processor to pull the output low even when the CAT70x is pulling it high.

Power Transients

Generally short duration negative-going transients of less than 2µs on the power supply at V_{RST} minimum will not cause a reset condition. However the lower the voltage of the transient the shorter the required time to cause a reset output. These issues can usually be remedied by the proper location of bypass capacitance on the circuit board.

OUTPUT VALID CONDITIONS

The $\overline{\text{RESET}}$ output uses a push-pull output which can maintain a valid output down to a **V_{CC} of 1.0 volts**. To sink current below 0.8V a resistor can be connected from $\overline{\text{RESET}}$ to Ground (see Figure 8.) This arrangement will maintain a valid value on the $\overline{\text{RESET}}$ output during both power up and down but will draw current when the $\overline{\text{RESET}}$ output is in the high state. A resistor value of about 100kΩ should be adequate in most situations to maintain a low condition valid output down to V_{CC} equal to 1.0V.

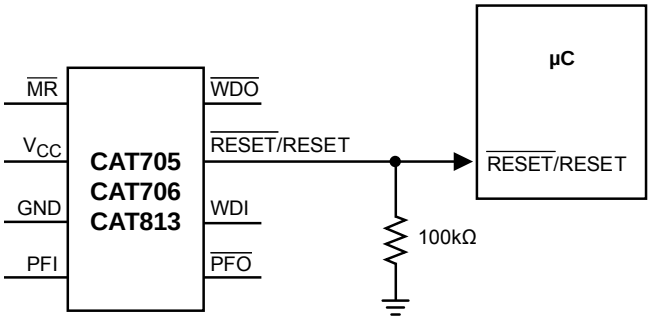


Figure 8. $\overline{\text{RESET}}$ Valid for V_{CC} < 1.0V

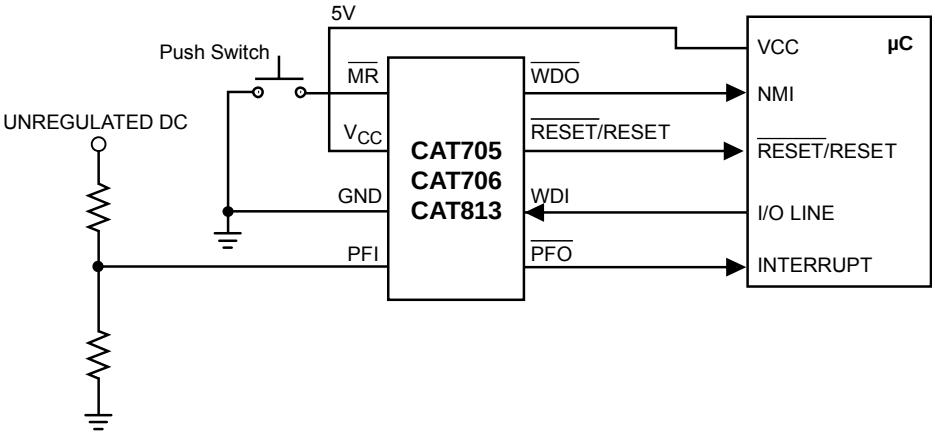
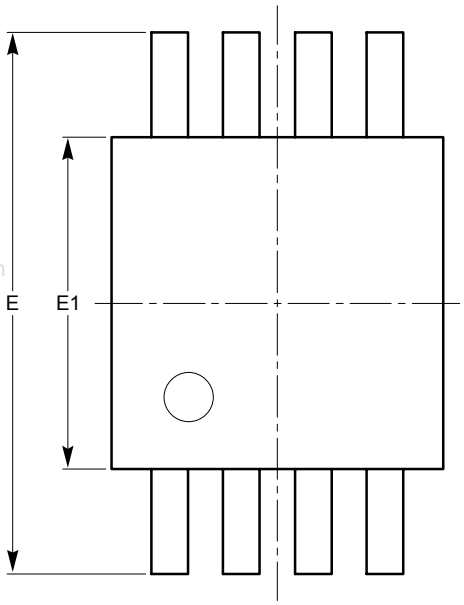


Figure 9. Typical Operating Circuit

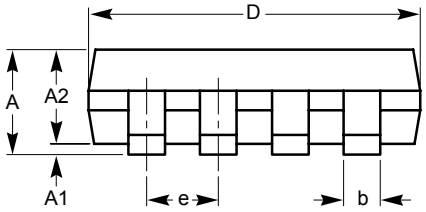
PACKAGE OUTLINE DRAWING

MSOP 8-Lead 3.0 x 3.0mm (Z) (1) (2)

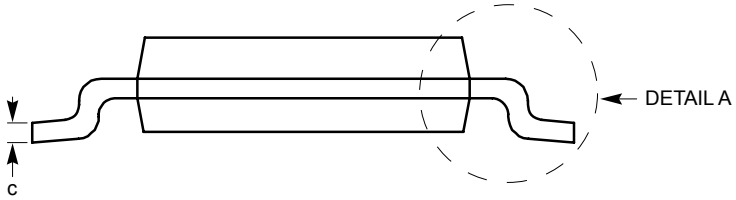


TOP VIEW

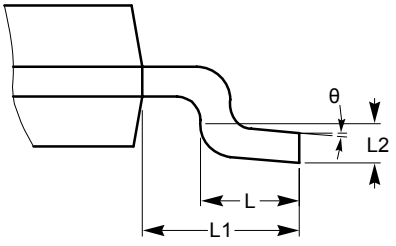
SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05	0.10	0.15
A2	0.75	0.85	0.95
b	0.22		0.38
c	0.13		0.23
D	2.90	3.00	3.10
E	4.80	4.90	5.00
E1	2.90	3.00	3.10
e		0.65 BSC	
L	0.40	0.60	0.80
L1		0.95 REF	
L2		0.25 BSC	
θ	0°		6°



SIDE VIEW



END VIEW

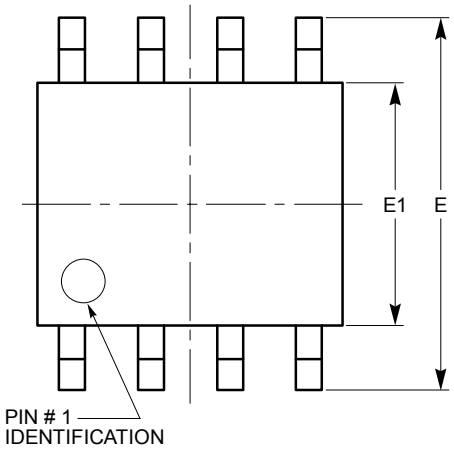


DETAIL A

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

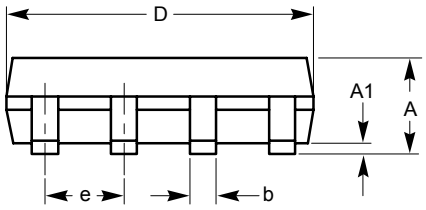
Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-187

SOIC 8-Lead 150 mils (V) [1] [2]

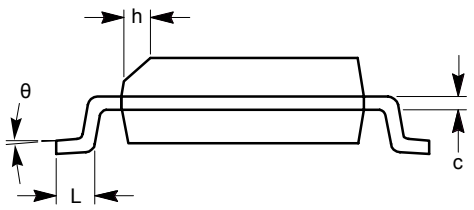


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0°		8°



SIDE VIEW

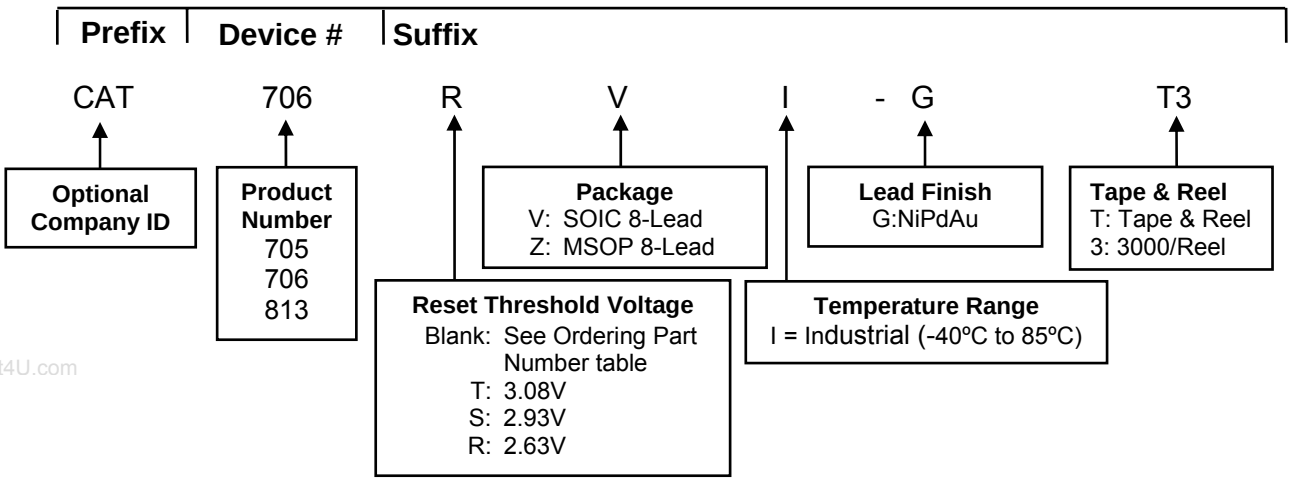


END VIEW

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

EXAMPLE OF ORDERING INFORMATION



TOP MARKING INFORMATION (FOR ALL THRESHOLDS)

NiPdAu Finish (-G)

Device #	Package	Top Marking
CAT705	MSOP	ABRT
CAT706	MSOP	ABRT
CAT813	MSOP	ABRS

ORDERING PART NUMBER

Order Part Number	Threshold Voltage
CAT705VI-G	4.65V
CAT705ZI-G	
CAT706VI-G	4.40V
CAT706ZI-G	
CAT706RVI-G	2.63
CAT706RZI-G	
CAT706SVI-G	2.93
CAT706SZI-G	
CAT706TVI-G	3.08
CAT706TZI-G	
CAT813VI-G	4.65V
CAT813ZI-G	

Notes:

(1) All packages are RoHS-compliant (Lead-free, Halogen-free).

(2) The standard lead finish is NiPdAu.

(3) This device used in the above example is a CAT706RVI -GT3 (2.63V, SOIC 8-Lead, Industrial Temperature, NiPdAu, Tape & Reel, 3,000/reel)

(4) Contact factory for package availability.

REVISION HISTORY

Date	Rev.	Reason
01/21/08	A	Initial Issue

Catalyst Semiconductor, Inc.
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Document No: MD-3030
Revision: A
Issue date: 01/21/08