64K x16 bit Low Power CMOS Static RAM

FEATURES SUMMARY

- Process Technology : 0.6•• CMOS
- Organization : 64K x16
- Data Byte Control : $\overline{LB}$=I/O1~8, $\overline{UB}$=I/O9~16
- Power Supply Voltage : 5.0V ••10%
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  44-TSOP(II)-Forward/Reverse

GENERAL DESCRIPTION

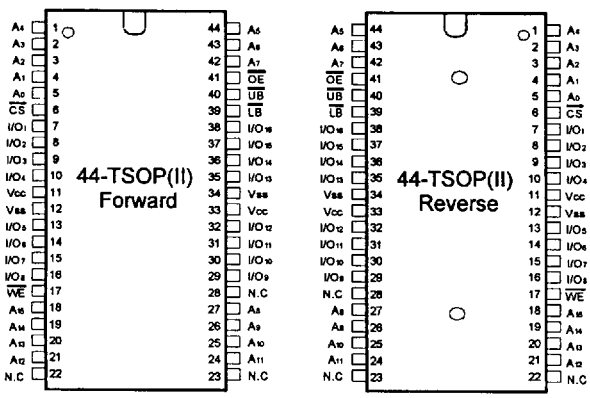
The KM6161000B family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range(V)	Speed	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max)	Operating (I_{CC2})	
KM6161000BLT/LT-L KM6161000BLR/LR-L	Commercia (0~70••)	4.5 to 5.5	55*/70	100/20••	120mA	44-TSOP(II) Forward/Reverse
KM6161000BLTI/LTI-L KM6161000BLRI/LRI-L	Industrial (-40~85••)	4.5 to 5.5	70/100	100/50••		

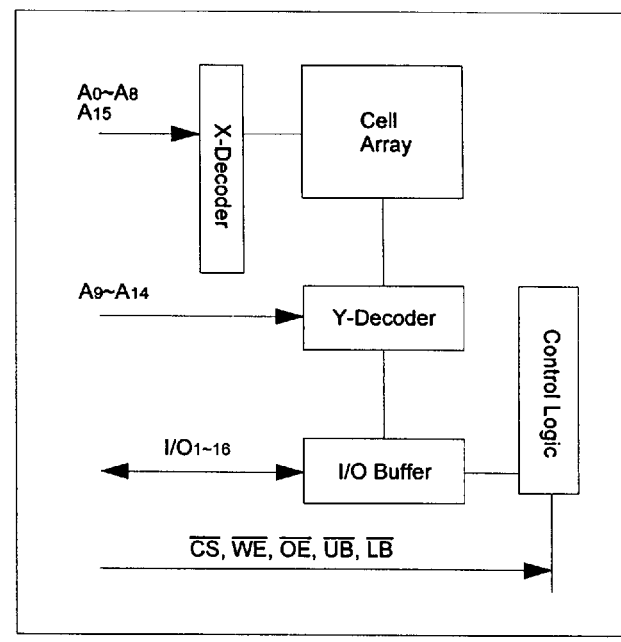
* The parameter is measured with 30pF test load.

PIN DESCRIPTION



Name	Function	Name	Function
A0~A15	Address Inputs	$\overline{LB}$	Lower Byte (I/O1~8)
$\overline{WE}$	Write Enable Input	$\overline{UB}$	Upper Byte(I/O9~16)
$\overline{CS}$	Chip Select Input	Vcc	Power
$\overline{OE}$	Output Enable Input	Vss	Ground
I/O1~16	Data Inputs/Outputs	N.C	No Connection

FUNCTIONAL BLOCK DIAGRAM

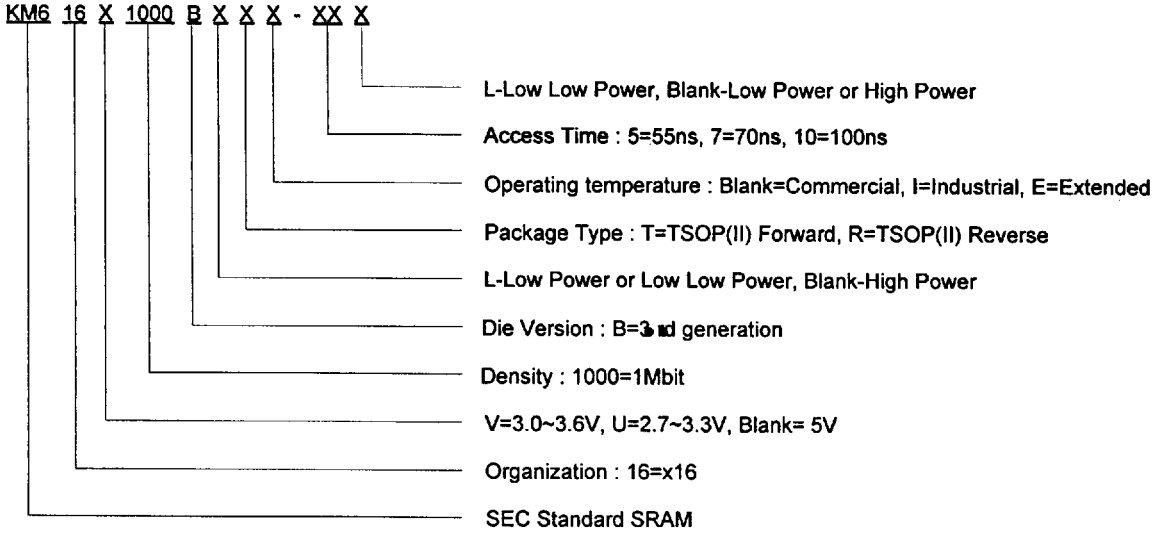


PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Product (0~70••)		Industrial Temp Products (-40~85••)	
Part Name	**Function**	**Part Name**	**Function**
KM6161000BLT-5	44-TSOP(II), F, 5V, 55ns, L-pwr	KM6161000BLTI-5	44-TSOP(II), F, 5V, 70ns, L-pwr
KM6161000BLT-5L	44-TSOP(II), F, 5V, 55ns, LL-pwr	KM6161000BLTI-5L	44-TSOP(II), F, 5V, 70ns, LL-pwr
KM6161000BLT-7	44-TSOP(II), F, 5V, 70ns, L-pwr	KM6161000BLTI-7	44-TSOP(II), F, 5V, 100ns, L-pwr
KM6161000BLT-7L	44-TSOP(II), F, 5V, 70ns, LL-pwr	KM6161000BLTI-7L	44-TSOP(II), F, 5V, 100ns, LL-pwr
KM6161000BLR-5	44-TSOP(II), R, 5V, 55ns, L-pwr	KM6161000BLRI-5	44-TSOP(II), R, 5V, 70ns, L-pwr
KM6161000BLR-5L	44-TSOP(II), R, 5V, 55ns, LL-pwr	KM6161000BLRI-5L	44-TSOP(II), R, 5V, 70ns, LL-pwr
KM6161000BLR-7	44-TSOP(II), R, 5V, 70ns, L-pwr	KM6161000BLRI-7	44-TSOP(II), R, 5V, 100ns, L-pwr
KM6161000BLR-7L	44-TSOP(II), R, 5V, 70ns, LL-pwr	KM6161000BLRI-7L	44-TSOP(II), R, 5V, 100ns, LL-pwr

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to 7.0	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-65 to 150	••	-
Operating Temperature	T_A	0 to 70	••	KM6161000BLT/LT-L KM6161000BLR/LR-L
		-40 to 85	••	KM6161000BLTI/LTI-L KM6161000BLRI/LRI-L
Soldering temperature and time	T_{SOLDER}	260••, 10sec (Lead Only)	-	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stres s rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied . Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	Vcc	4.5	5	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	2.2	-	Vcc+0.5	V
Input low voltage	V_{IL}	-0.5***	-	0.8	V

* 1) Commercial Product : Ta=0 to 70 ••, unless otherwise specified
2) Industrial Product : Ta=-40 to 85 ••, unless otherwise specified
** Ta=25••
*** Vil(min)=-3.0V for •• 50ns pulse width

CAPACITANCE* (f=1MHz, TA=25••)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	8	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		I_{LI}	V_{IN}=V_{SS} to V_{CC}		-1	-	1	••
Output leakage current		I_{LO}	$\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL}, $\overline{UB}$=V_{IH} or $\overline{LB}$=V_{IH}, V_{IO}=V_{SS} to V_{CC}		-1	-	1	••
Operating power supply current Average operatingcurrent		I_{CC}	$\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}, I_{IO}=0mA	Read	-	-	10	mA
				Write	-	-	35	
		I_{CC1}	Cycle time=1•• 100% duty $\overline{CS}$••0.2V, I_{IO}=0mA	Read	-	-	15	mA
				Write	-	-	40	
		I_{CC2}	Min cycle, 100% duty, $\overline{CS}$=V_{IL}, I_{IO}=0mA		-	-	120	mA
Output low voltage		V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage		V_{OH}	I_{OH}=-1.0mA		2.4	-	-	V
Standby Current(TTL)		I_{SB}	$\overline{CS}$=V_{IH}		-	-	3	mA
Standby Current (CMOS)	KM6161000BL/L-L	I_{SB1}	$\overline{CS}$••V_{CC}-0.2V V_{IN}••V_{CC}-0.2V or V_{IN}••0.2V	L(Low Power)	-	-	100	••
				LL(L Low Power)	-	-	20	
	KM6161000BLI/LI-L			L(Low Power)	-	-	100	••
				LL(L Low Power)	-	-	50	

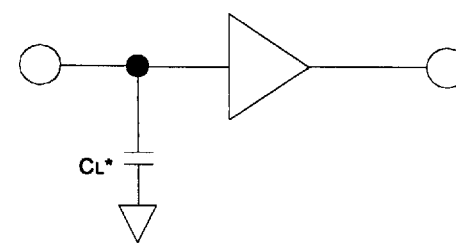
* 1) Commercial Product : T_A=0 to 70••, Unless otherwise specified
2) Industrial Product : T_A=-40 to 85••, Unless otherwise specified
** TA=25••

A.C CHARACTERISTICS

TEST CONDITIONS(1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.8 to 2.4V	-
Input rising and falingl time	5ns	-
input and output reference voltage	1.5V	-
Output load (See right)	C_L=100••+1TTL **C_L=30••+1TTL	-

* See DC Operating conditions
** Test load for 55ns product



* Including scope and jig capacitance

TEST CONDITIONS(2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM6161000BL/L-L	0~70••	5.0V •• 10%	55*/70ns	Commercial
KM6161000BLI/LI-L	-40~85••	5.0V •• 10%	70/100ns	Industrial

* The parameter is measured with 30pF test load.

PARAMETER LIST FOR EACH SPEED BIN

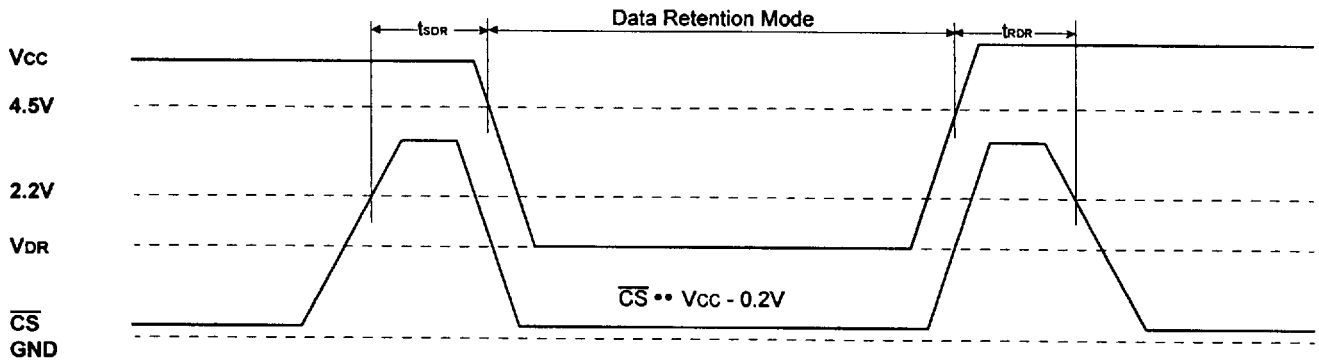
Parameter List		Symbol	Speed Bins						Units
			55ns		70ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	55	-	70	-	100	-	ns
	Address access time	tAA	-	55	-	70	-	100	ns
	Chip select to output	tCO	-	55	-	70	-	100	ns
	Output enable to valid output	tOE	-	25	-	35	-	50	ns
	$\overline{UB}$,$\overline{LB}$ Access Time	tBA	-	25	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	$\overline{UB}$,$\overline{LB}$ enable to low-Z output	tBLZ	5	-	5	-	5	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	20	0	25	0	30	ns
	$\overline{UB}$,$\overline{LB}$ disable to high-Z output	tBHZ	0	20	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	20	0	25	0	30	ns
	Output hold from address change	tOH	10	-	15	-	15	-	ns
Write	Write cycle time	tWC	55	-	70	-	100	-	ns
	Chip select to end of write	tCW	45	-	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	60	-	80	-	ns
	Write pulse width	tWP	40	-	50	-	70	-	ns
	$\overline{UB}$, $\overline{LB}$ valid to end of write	tBW	45	-	60	-	80	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	30	0	35	ns
	Data to write time overlap	tDW	25	-	30	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	ns

DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
VCC for data retention	VDR		$\overline{CS}$•• Vcc-0.2V		2.0	-	5.5	V
Data retention current	IDR	KM6161000B Family	Vcc=3.0V $\overline{CS}$•• Vcc-0.2V	L-Ver LL-Ver	- -	- -	50 15	••
		KM6161000BI Family		L-Ver LL-Ver	- -	- -	50 15	••
Data retention set-up time	tSDR		See data retention waveform		0	-	-	ms
Recovery time	tRDR				5	-	-	

* 1) Commercial Product : Ta=0 to 70••, unless otherwise specified
2) Industrial Product : Ta=-40 to 85••, unless otherwise specified
** Ta=25••

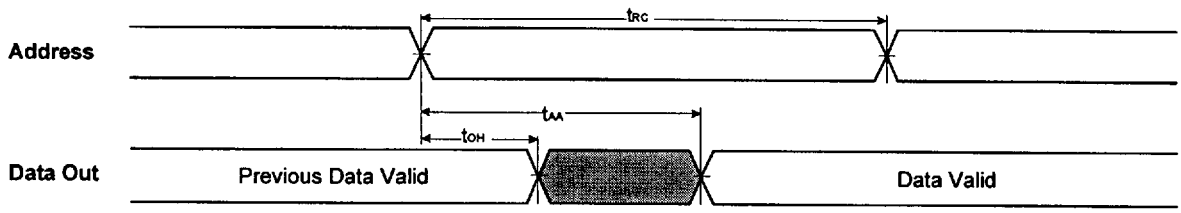
DATA RETENTION TIMING DIAGRAM



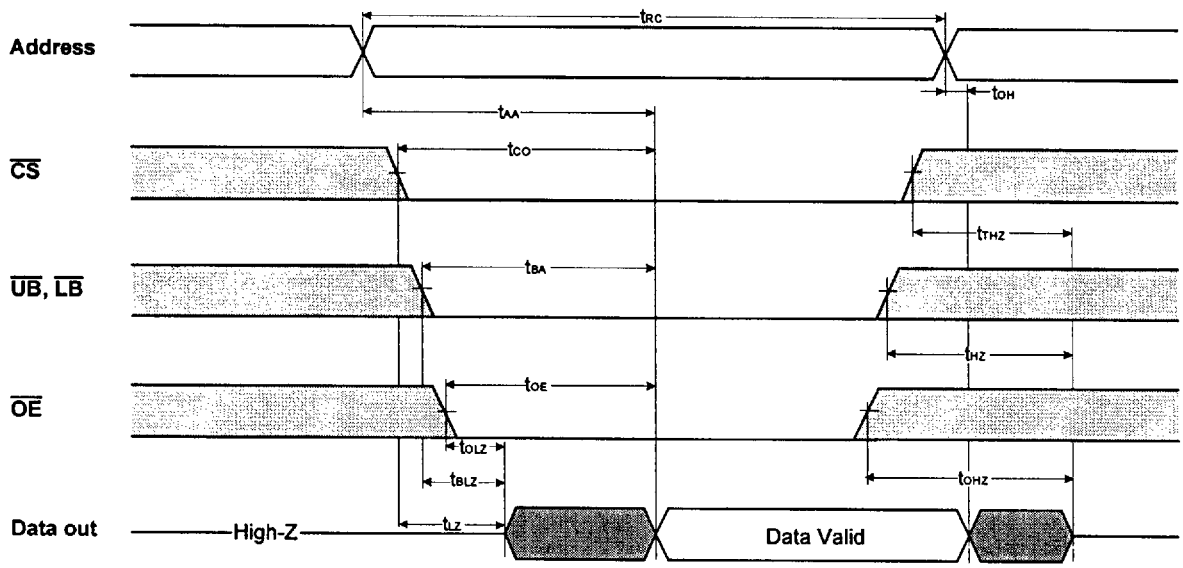
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH}, $\overline{UB}$ or and $\overline{LB}$=V_{IL})



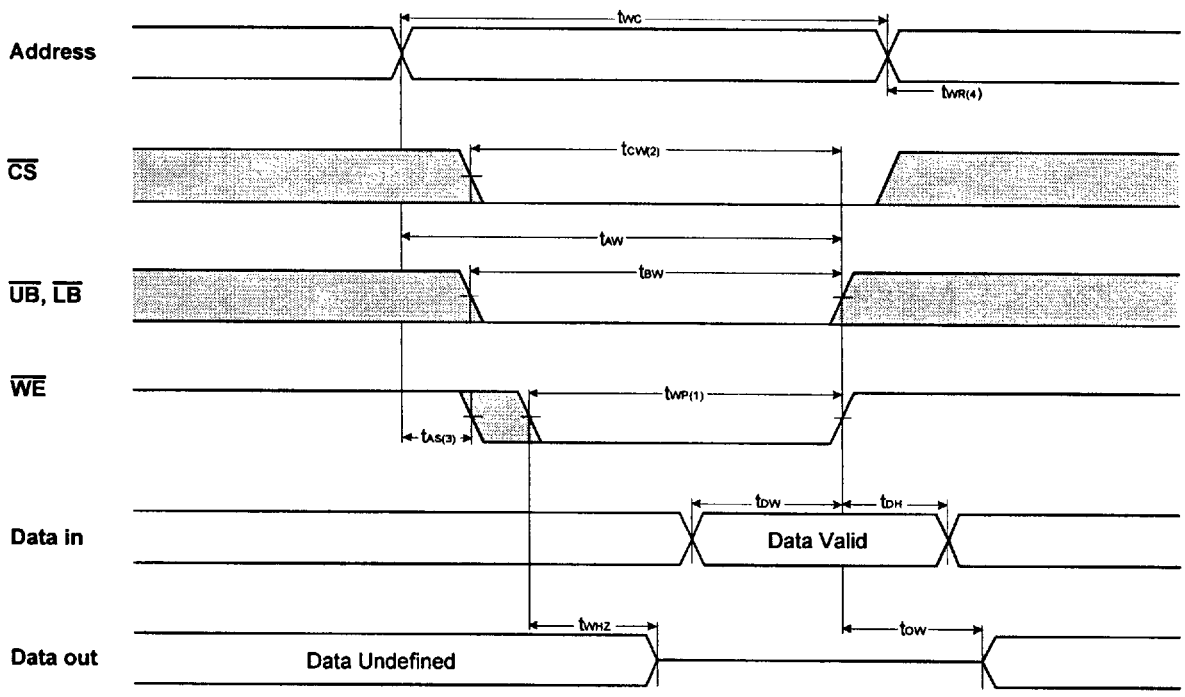
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



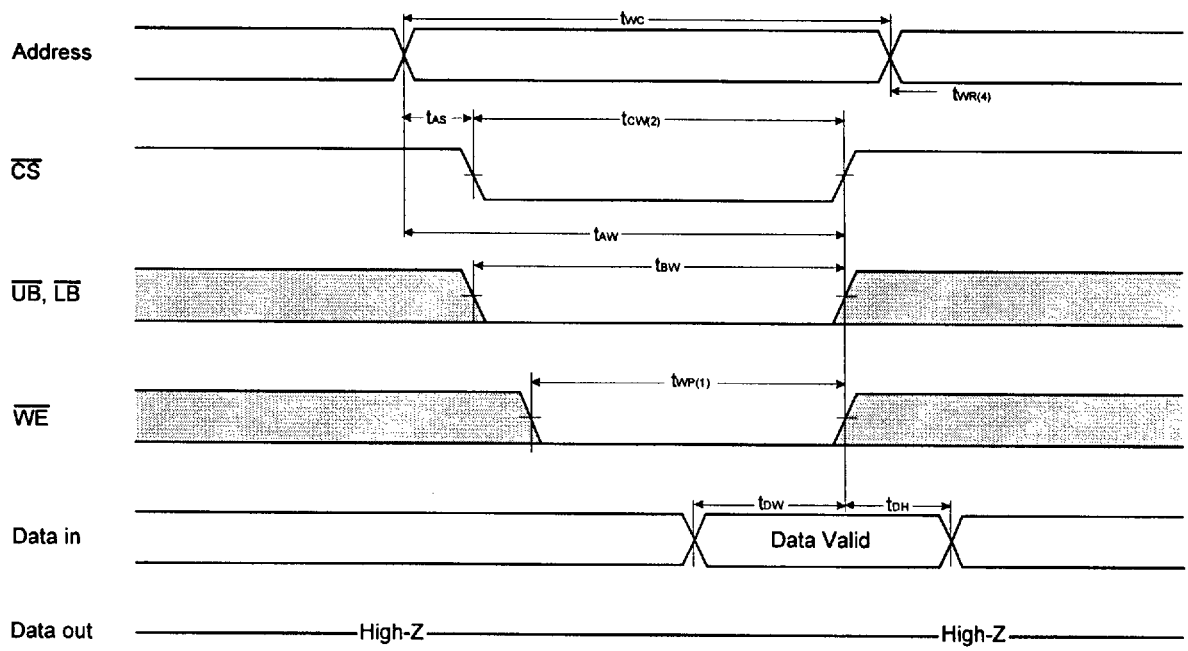
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.

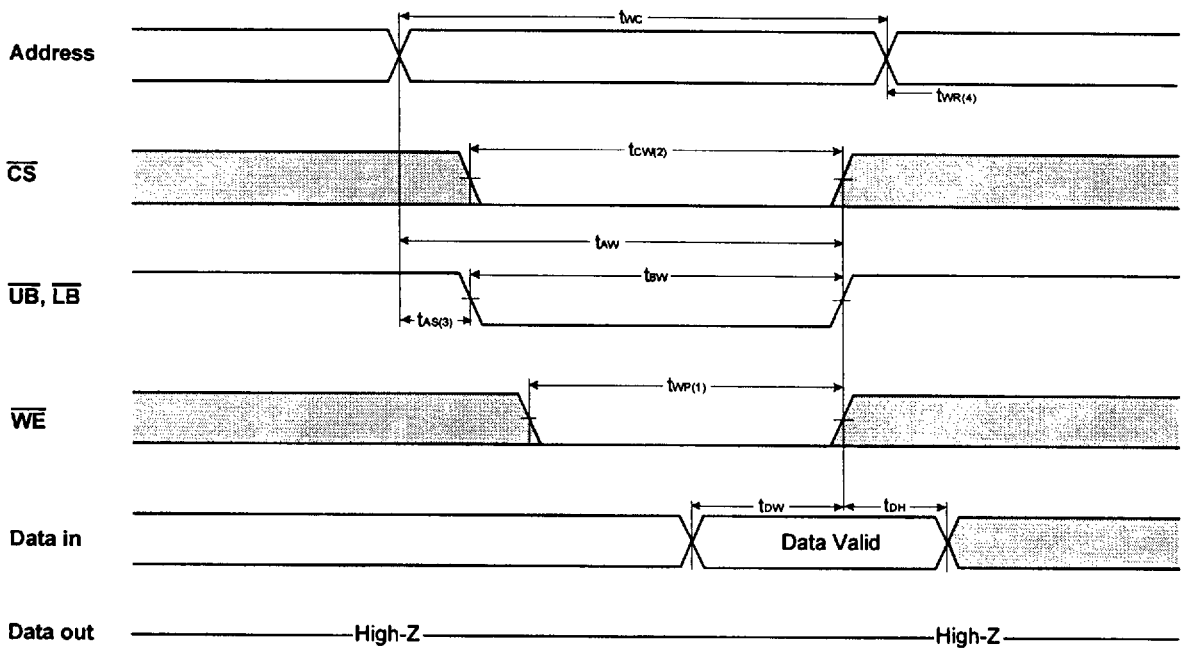
TIMING WAVEFORM OF WRITE CYCLE (1)($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE (2)($\overline{CS}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3)($\overline{UB}$, $\overline{LB}$ Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultenious asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end or write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

FUNCTIONAL DESCRIPTION

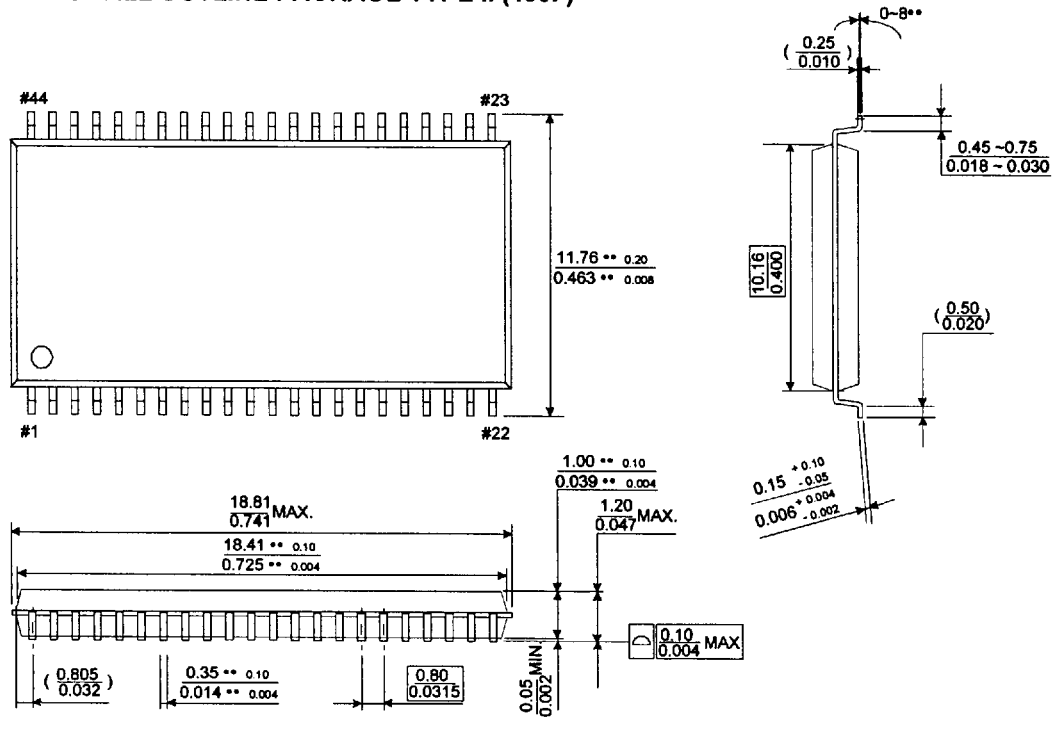
$\overline{CS}$	$\overline{LB}$	$\overline{UB}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O1~8	I/O9~16	Current Mode
H	X	X	X	X	Not Select	High-Z	High-Z	I_{SB1}
L	X	X	H	H	Output Disable	High-Z	High-Z	Icc
L	H	H	X	X		High-Z	High-Z	
L	L H L	H L L	H	L	Read	Dout High-Z Dout	High-Z Dout Dout	Icc
L	L H L	H L L	L	X	Write	Din High-Z Din	High Din Din	Icc

* X means dont care (Must be in low or high state)

PACKAGE DIMENSIONS

Unit :Millimeter(Inch)

44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)



44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400R)