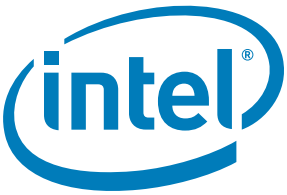

Intel® Core™2 Extreme Processor QX9775Δ

Datasheet

February 2008

Document Number:319128-001

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Revision History

Revision	Description	Date
-001	Initial release	February 2008

Intel® Core™2 Extreme Processor QX9775$^{\Delta}$ Features

- Available at 3.2 GHz
- FSB frequency at 1600 MHz
- Enhanced Intel Speedstep® Technology
- Supports Intel® 64$^{\Phi}$ architecture
- Supports Intel® Virtualization Technology
- Supports Execute Disable Bit capability
- Binary compatible with applications running on previous members of the Intel microprocessor line
- Intel® Wide Dynamic Execution
- Intel® Advanced Smart Cache
- Intel® Smart Memory Access
- Intel® Intelligent Power Capability
- Intel® Advanced Digital Media Boost
- Optimized for 32-bit applications running on advanced 32-bit operating systems
- Two 6 MB Level 2 caches
- Intel® HD Boost utilizing new SSE4 instructions for improved multimedia performance, especially for video encoding and photo processing
- System Management mode
- 24-way cache associativity provides improved cache hit rate on load/store operations
- 771-land Package

The Intel Core™2 Extreme processor QX9775, designed for dual-socket configurations, delivers Intel's most advanced processor for professional multimedia content creation and for intense visual gaming. The processor is designed to deliver performance across applications and usages where end-users can truly appreciate and experience the performance.

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1 Introduction

The Intel® Core™2 Extreme processor QX9775 is a server/workstation processor using four 45-nm Hi-k next generation Intel® Core™ microarchitecture cores. The processor is manufactured on Intel's 45 nanometer process technology combining high performance with the power efficiencies of a low-power microarchitecture. The Intel® Core™2 Extreme processor QX9775 maintains the tradition of compatibility with IA-32 software.

Note: For this document, Intel® Core™2 Extreme processor QX9775 is referred to as "processor".

Key processor features include on-die, primary 32-kB instruction cache and 32-kB write-back data cache in each core and 12 MB (2 x 6 MB) Level 2 cache with Intel® Advanced Smart Cache Architecture. The processors' Data Prefetch Logic speculatively fetches data to the L2 cache before an L1 cache requests occurs, resulting in reduced effective bus latency and improved performance. The 1600 MHz Front Side Bus (FSB) is a quad-pumped bus running from a 400 MHz system clock making 12.80 GBytes per second data transfer rates possible.

Enhanced thermal and power management capabilities are implemented including Intel® Thermal Monitor (TM1), Thermal Monitor 2 (TM2) and Enhanced Intel SpeedStep® Technology. These technologies are targeted for dual processor configurations in enterprise environments. TM1 and TM2 provide efficient and effective cooling in high temperature situations. Enhanced Intel SpeedStep Technology provides power management capabilities to servers and workstations.

Processor features also include Intel® Wide Dynamic Execution, enhanced floating point and multi-media units, Streaming SIMD Extensions 2 (SSE2), Streaming SIMD Extensions 3 (SSE3), and Streaming SIMD Extensions 4.1 (SSE4.1). Advanced Dynamic Execution improves speculative execution and branch prediction internal to the processor. The floating point and multi-media units include 128-bit wide registers and a separate register for data movement. SSE3 instructions provide highly efficient double-precision floating point, SIMD integer, and memory management operations.

The processor supports Intel® 64 Architecture as an enhancement to Intel's IA-32 architecture. This enhancement allows the processor to execute operating systems and applications written to take advantage of the 64-bit extension technology. Further details on Intel® 64 Architecture and its programming model can be found in the Intel® 64 and IA-32 Architectures Software Developer's Manual, at http://www.intel.com/products/processor/manuals/.

In addition, the processor supports the Execute Disable Bit functionality. When used in conjunction with a supporting operating system, Execute Disable allows memory to be marked as executable or non executable. This feature can prevent some classes of viruses that exploit buffer overrun vulnerabilities and can thus help improve the overall security of the system. Further details on Execute Disable can be found at http://www.intel.com/cd/ids/developer/asmo-na/eng/149308.htm.

The processor supports Intel® Virtualization Technology for hardware-assisted virtualization within the processor. Intel Virtualization Technology is a set of hardware enhancements that can improve virtualization solutions. Intel Virtualization Technology is used in conjunction with Virtual Machine Monitor software enabling multiple, independent software environments inside a single platform. Further details on Intel Virtualization Technology can be found at http://developer.intel.com/technology/platform-technology/virtualization/index.htm.

The processor is intended for high performance server and workstation systems. The processor supports a Dual Independent Bus (DIB) architecture with one processor on each bus, up to two processor sockets in a system. The DIB architecture provides improved performance by allowing increased FSB speeds and bandwidth. The processor is packaged in an FC-LGA Land Grid Array package with 771 lands for improved power delivery. It uses a surface mount LGA771 socket that supports Direct Socket Loading (DSL).

The Intel® Core™2 Extreme processor QX9775-based platforms implement independent core voltage (V_{CC}) power planes for each processor. FSB termination voltage (V_{TT}) is shared and must connect to all FSB agents. The processor core voltage uses power delivery guidelines specified by VRM/EVRD 11.0 and its associated load line (see *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.0 Design Guidelines* for further details). VRM/EVRD 11.0 will support the power requirements of all frequencies of the processor.

The processor supports a1600 MHz Front Side Bus operations. The FSB uses a split-transaction, deferred reply protocol and Source-Synchronous Transfer (SST) of address and data to improve performance. The processor transfers data four times per bus clock (4X data transfer rate, as in AGP 4X). Along with the 4X data bus, the address bus can deliver addresses two times per bus clock and is referred to as a 'double-clocked' or a 2X address bus. In addition, the Request Phase completes in one clock cycle. The FSB is also used to deliver interrupts.

Signals on the FSB use Assisted Gunning Transceiver Logic (AGTL+) level voltages. Section 2.1 contains the electrical specifications of the FSB.

1.1 Terminology

A '#' symbol after a signal name refers to an active low signal, indicating a signal is in the asserted state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as address or data), the '#' symbol implies that the signal is inverted. For example, D[3:0] = 'HLHL' refers to a hex 'A', and D[3:0]# = 'LHLH' also refers to a hex 'A' (H= High logic level, L= Low logic level).

Commonly used terms are explained here for clarification:

- Intel® Core™2 Extreme processor QX9775 – Intel® 64-bit microprocessor intended for dual processor desktops. The processor is based on Intel's 45 nanometer process, and packaged in the FC-LGA package with four processor cores.
- **FC-LGA (Flip Chip Land Grid Array) Package** – The processor package is a Land Grid Array, consisting of a processor core mounted on a pinless substrate with 771 lands, and includes an integrated heat spreader (IHS).
- **LGA771 socket** – The processor interfaces to the baseboard through this surface mount, 771 Land socket. See the *LGA771 Socket Design Guidelines* for details regarding this socket.
- **Processor core** – Processor core with integrated L1 cache. L2 cache and system bus interface are shared between the two cores on the die. All AC timing and signal integrity specifications are at the pads of the system bus interface.
- **Front Side Bus (FSB)** – The electrical interface that connects the processor to the chipset. Also referred to as the processor system bus or the system bus. All memory and I/O transactions, as well as interrupt messages, pass between the processor and chipset over the FSB.
- **Dual Independent Bus (DIB)** – A front side bus architecture with one processor on each of several processor buses, rather than a processor bus shared between

two processor agents. The DIB architecture provides improved performance by allowing increased FSB speeds and bandwidth.

- **Functional Operation** – Refers to the normal operating conditions in which all processor specifications, including DC, AC, FSB, signal quality, mechanical and thermal are satisfied.
- **Storage Conditions** – Refers to a non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor lands should not be connected to any supply voltages, have any I/Os biased or receive any clocks. Upon exposure to “free air” (that is, unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
- **Priority Agent** – The priority agent is the host bridge to the processor and is typically known as the chipset.
- **Symmetric Agent** – A symmetric agent is a processor which shares the same I/O subsystem and memory array, and runs the same operating system as another processor in a system. Systems using symmetric agents are known as Symmetric Multiprocessing (SMP) systems.
- **Integrated Heat Spreader (IHS)** – A component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
- **Thermal Design Power (TDP)** – Processor thermal solutions should be designed to meet this target. It is the highest expected sustainable power while running known power intensive applications. TDP is not the maximum power that the processor can dissipate.
- **Intel® 64 Architecture** – An enhancement to Intel's IA-32 architecture that allows the processor to execute operating systems and applications written to take advantage of the 64-bit extension technology.
- **Enhanced Intel SpeedStep® Technology** – Technology that provides power management capabilities to servers and workstations.
- **Platform Environment Control Interface (PECI)** – A proprietary one-wire bus interface that provides a communication channel between Intel processor and external thermal monitoring devices, for use in fan speed control. PECI communicates readings from the processor’s digital thermometer. PECI replaces the thermal diode available in previous processors.
- **Intel® Virtualization Technology** – Processor virtualization, which when used in conjunction with Virtual Machine Monitor software enables multiple, robust independent software environments inside a single platform.
- **VRM (Voltage Regulator Module)** – DC-DC converter built onto a module that interfaces with a card edge socket and supplies the correct voltage and current to the processor based on the logic state of the processor VID bits.
- **EVRD (Enterprise Voltage Regulator Down)** – DC-DC converter integrated onto the system board that provides the correct voltage and current to the processor based on the logic state of the processor VID bits.
- **V_{CC}** – The processor core power supply.
- **V_{SS}** – The processor ground.
- **V_{TT}** – FSB termination voltage.

1.2 References

Material and concepts available in the following documents may be beneficial when reading this document.

Document	Location
Intel® Core™2 Extreme Processor QX9775 Specification Update	http://www.intel.com/design/processor/specupdt/319129.htm
Intel® Core™2 Extreme Processor QX9775 Thermal and Mechanical Design Guidelines Addendum (TMDG)	http://www.intel.com/design/processor/designex/319130.htm
LGA771 Socket Mechanical Design Guide	http://www.intel.com/design/xeon/guides/313871.htm
Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.0 Design Guidelines	http://www.intel.com/design/processor/applnots/313214.htm
AP-485, Intel® Processor Identification and the CPUID Instruction	http://www.intel.com/design/processor/applnots/241618.htm
Intel® 64 and IA-32 Intel Architecture Software Developer's Manuals *Volume 1: Basic Architecture* *Volume 2A: Instruction Set Reference, A-M* *Volume 2B: Instruction Set Reference, N-Z* *Volume 3A: System Programming Guide* *Volume 3B: System Programming Guide*	http://www.intel.com/products/processor/manuals/
Intel® 64 and IA-32 Intel® Architecture Optimization Reference Manual	http://www.intel.com/products/processor/manuals/
Intel® 64 and IA-32 Intel® Software Developer's Manual Documentation Changes	http://www.intel.com/products/processor/manuals/

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2 Electrical Specifications

2.1 Front Side Bus and GTLREF

Most processor FSB signals use Assisted Gunning Transceiver Logic (AGTL+) signaling technology. This technology provides improved noise margins and reduced ringing through low voltage swings and controlled edge rates. AGTL+ buffers are open-drain and require pull-up resistors to provide the high logic level and termination. AGTL+ output buffers differ from GTL+ buffers with the addition of an active PMOS pull-up transistor to “assist” the pull-up resistors during the first clock of a low-to-high voltage transition. Platforms implement a termination voltage level for AGTL+ signals defined as V_{TT}. Because platforms implement separate power planes for each processor (and chipset), separate V_{CC} and V_{TT} supplies are necessary. This configuration allows for improved noise tolerance as processor frequency increases. Speed enhancements to data and address buses have made signal integrity considerations and platform design methods even more critical than with previous processor families.

The AGTL+ inputs require reference voltages (GTLREF_DATA_MID, GTLREF_DATA_END, GTLREF_ADD_MID, and GTLREF_ADD_END) which are used by the receivers to determine if a signal is a logical 0 or a logical 1. GTLREF_DATA_MID and GTLREF_DATA_END is used for the 4X front side bus signaling group and GTLREF_ADD_MID and GTLREF_ADD_END is used for the 2X and common clock front side bus signaling groups. GTLREF_DATA_MID, GTLREF_DATA_END, GTLREF_ADD_MID, and GTLREF_ADD_END must be generated on the baseboard (See Table 2-18 for GTLREF_DATA_MID, GTLREF_DATA_END, GTLREF_ADD_MID, and GTLREF_ADD_END specifications). Termination resistors (R_{TT}) for AGTL+ signals are provided on the processor silicon and are terminated to V_{TT}. The on-die termination resistors are always enabled on the processor to control reflections on the transmission line. Intel chipsets also provide on-die termination, thus eliminating the need to terminate the bus on the baseboard for most AGTL+ signals.

Some FSB signals do not include on-die termination (R_{TT}) and must be terminated on the baseboard. See Table 2-8 for details regarding these signals.

The AGTL+ bus depends on incident wave switching. Therefore, timing calculations for AGTL+ signals are based on flight time as opposed to capacitive deratings. Analog signal simulation of the FSB, including trace lengths, is highly recommended when designing a system. Contact your Intel Field Representative to obtain the processor signal integrity models, which includes buffer and package models.

2.2 Power and Ground Lands

For clean on-chip processor core power distribution, the processor has 223 V_{CC} (power) and 267 V_{SS} (ground) inputs. All V_{CC} lands must be connected to the processor power plane, while all V_{SS} lands must be connected to the system ground plane. The processor V_{CC} lands must be supplied with the voltage determined by the processor Voltage IDentification (VID) signals. See Table 2-3 for VID definitions.

Twenty two lands are specified as V_{TT}, which provide termination for the FSB and provides power to the I/O buffers. The platform must implement a separate supply for these lands which meets the V_{TT} specifications outlined in Table 2-12.

2.3 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large average current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Larger bulk storage (C_{BULK}), such as electrolytic capacitors, supply voltage during longer lasting changes in current demand by the component, such as coming out of an idle condition. Similarly, they act as a storage well for current when entering an idle condition from a running condition. Care must be taken in the baseboard design to ensure that the voltage provided to the processor remains within the specifications listed in Table 2-12. Failure to do so can result in timing violations or reduced lifetime of the component.

2.3.1 V_{CC} Decoupling

Vcc regulator solutions need to provide bulk capacitance with a low Effective Series Resistance (ESR), and the baseboard designer must assure a low interconnect resistance from the regulator (EVRD or VRM pins) to the LGA771 socket. Bulk decoupling must be provided on the baseboard to handle large voltage swings. The power delivery solution must insure the voltage and current specifications are met (as defined in Table 2-12).

2.3.2 V_{TT} Decoupling

Bulk decoupling must be provided on the baseboard. Decoupling solutions must be sized to meet the expected load. To insure optimal performance, various factors associated with the power delivery solution must be considered including regulator type, power plane and trace sizing, and component placement. A conservative decoupling solution consists of a combination of low ESR bulk capacitors and high frequency ceramic capacitors.

2.3.3 Front Side Bus AGTL+ Decoupling

The processor integrates signal termination on the die, as well as a portion of the required high frequency decoupling capacitance on the processor package. However, additional high frequency capacitance must be added to the baseboard to properly decouple the return currents from the FSB. Bulk decoupling must also be provided by the baseboard for proper AGTL+ bus operation.

2.4 Front Side Bus Clock (BCLK[1:0]) and Processor Clocking

BCLK[1:0] directly controls the FSB interface speed as well as the core frequency of the processor. As in previous processor generations, the processor core frequency is a multiple of the BCLK[1:0] frequency. The processor bus ratio multiplier is set during manufacturing. The default setting is for the maximum speed of the processor. It is possible to override this setting using software (see the *Intel® 64 and IA-32 Architectures Software Developer's Manual*). This permits operation at lower frequencies than the processor's tested frequency.

The processor core frequency is configured during reset by using values stored internally during manufacturing. The stored value sets the highest bus fraction at which the particular processor can operate. If lower speeds are desired, the appropriate ratio can be configured via the CLOCK_FLEX_MAX MSR. For details of operation at core frequencies lower than the maximum rated processor speed, refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manual.*

Clock multiplying within the processor is provided by the internal phase locked loop (PLL), which requires a constant frequency BCLK[1:0] input, with exceptions for spread spectrum clocking. Processor DC specifications for the BCLK[1:0] inputs are provided in Table 2-19. These specifications must be met while also meeting signal integrity requirements as outlined in Table 2-19. The processor uses differential clocks. Table 2-1 contains processor core frequency to FSB multipliers and their corresponding core frequencies.

Table 2-1. Core Frequency to FSB Multiplier Configuration

Core Frequency to FSB Multiplier	Core Frequency with 400.000 MHz Bus Clock	Notes
1/6	2.40 GHz	1, 2, 3
1/7	2.80 GHz	1, 2
1/7.5	3 GHz	1, 2
1/8	3.20 GHz	1, 2
1/8.5	3.40 GHz	1, 2
1/9	3.60 GHz	1, 2
1/9.5	3.80 GHz	1, 2
1/10	4 GHz	1, 2
1/10.5	4.20 GHz	1, 2
1/11	4.40 GHz	1, 2
1/11.5	4.60 GHz	1, 2
1/12	4.80 GHz	1, 2
1/12.5	5 GHz	1, 2
1/13	5.20 GHz	1, 2

NOTES:
1. Listed frequencies are not necessarily committed production frequencies.
2. For valid processor core frequencies, see the *Intel® Core™2 Extreme processor QX9775 Specification Update*
3. The lowest bus ratio supported by the processor is 1/6.

2.4.1 Front Side Bus Frequency Select Signals (BSEL[2:0])

Upon power up, the FSB frequency is set to the maximum supported by the individual processor. BSEL[2:0] are CMOS outputs which must be pulled up to V_{TT}, and are used to select the FSB frequency. Refer to Table 2-14 for DC specifications. Table 2-2 defines the possible combinations of the signals and the frequency associated with each combination. The frequency is determined by the processor(s), chipset, and clock synthesizer. All FSB agents must operate at the same core and FSB frequency.

Table 2-2. BSEL[2:0] Frequency Table

BSEL2	BSEL1	BSEL0	Bus Clock Frequency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	400 MHz
1	1	1	Reserved

2.4.2 PLL Power Supply

An on-die PLL filter solution is implemented on the processor. The V_{CCPLL} input is used for this configuration in Intel® Core™2 Extreme processor QX9775 -based platforms. Refer to Table 2-12 for DC specifications.

2.5 Voltage Identification (VID)

The Voltage Identification (VID) specification for the processor is defined by the *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.0 Design Guidelines*. The voltage set by the VID signals is the reference VR output voltage to be delivered to the processor Vcc pins. VID signals are open drain outputs, which must be pulled up to V_{TT}. Refer to Table 2-15 for the DC specifications for these signals. A voltage range is provided in Table 2-12 and changes with frequency. The specifications have been set such that one voltage regulator can operate with all supported frequencies.

Individual processor VID values may be calibrated during manufacturing such that two devices at the same core frequency may have different default VID settings. This is reflected by the VID range values provided in Table 2-3.

The processor uses six voltage identification signals, VID[6:1], to support automatic selection of power supply voltages. Table 2-3 specifies the voltage level corresponding to the state of VID[6:1]. A '1' in this table refers to a high voltage level and a '0' refers to a low voltage level. If the processor socket is empty (VID[6:1] = 111111), or the voltage regulation circuit cannot supply the voltage that is requested, the voltage regulator must disable itself. See the *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.0 Design Guidelines* for further details.

Although the *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.0 Design Guidelines* defines VID[7:0], VID7 and VID0 are not used on the processor; VID7 is always hard wired low at the voltage regulator.

The processor provides the ability to operate while transitioning to an adjacent VID and its associated processor core voltage (V_{CC}). This will represent a DC shift in the load line. It should be noted that a low-to-high or high-to-low voltage state change may result in as many VID transitions as necessary to reach the target core voltage. Transitions above the specified VID are not permitted. Table 2-12 includes VID step sizes and DC shift ranges. Minimum and maximum voltages must be maintained as shown in Table 2-13 and Table 2-2.

The VRM or EVRD used must be capable of regulating its output to the value defined by the new VID. DC specifications for dynamic VID transitions are included in Table 2-12 and Table 2-13. Refer to the *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.0 Design Guidelines* for further details.

Power source characteristics must be assured to be stable whenever the supply to the voltage regulator is stable.

Table 2-3. Voltage Identification Definition

HEX	VID6	VID5	VID4	VID3	VID2	VID1	V_{CC_MAX}	HEX	VID6	VID5	VID4	VID3	VID2	VID1	V_{CC_MAX}
7A	1	1	1	1	0	1	0.8500	3C	0	1	1	1	1	0	1.2375
78	1	1	1	1	0	0	0.8625	3A	0	1	1	1	0	1	1.2500
76	1	1	1	0	1	1	0.8750	38	0	1	1	1	0	0	1.2625
74	1	1	1	0	1	0	0.8875	36	0	1	1	0	1	1	1.2750
72	1	1	1	0	0	1	0.9000	34	0	1	1	0	1	0	1.2875
70	1	1	1	0	0	0	0.9125	32	0	1	1	0	0	1	1.3000
6E	1	1	0	1	1	1	0.9250	30	0	1	1	0	0	0	1.3125
6C	1	1	0	1	1	0	0.9375	2E	0	1	0	1	1	1	1.3250
6A	1	1	0	1	0	1	0.9500	2C	0	1	0	1	1	0	1.3375
68	1	1	0	1	0	0	0.9625	2A	0	1	0	1	0	1	1.3500
66	1	1	0	0	1	1	0.9750	28	0	1	0	1	0	0	1.3625
64	1	1	0	0	1	0	0.9875	26	0	1	0	0	1	1	1.3750
62	1	1	0	0	0	1	1.0000	24	0	1	0	0	1	0	1.3875
60	1	1	0	0	0	0	1.0125	22	0	1	0	0	0	1	1.4000
5E	1	0	1	1	1	1	1.0250	20	0	1	0	0	0	0	1.4125
5C	1	0	1	1	1	0	1.0375	1E	0	0	1	1	1	1	1.4250
5A	1	0	1	1	0	1	1.0500	1C	0	0	1	1	1	0	1.4375
58	1	0	1	1	0	0	1.0625	1A	0	0	1	1	0	1	1.4500
56	1	0	1	0	1	1	1.0750	18	0	0	1	1	0	0	1.4625
54	1	0	1	0	1	0	1.0875	16	0	0	1	0	1	1	1.4750
52	1	0	1	0	0	1	1.1000	14	0	0	1	0	1	0	1.4875
50	1	0	1	0	0	0	1.1125	12	0	0	1	0	0	1	1.5000
4E	1	0	0	1	1	1	1.1250	10	0	0	1	0	0	0	1.5125
4C	1	0	0	1	1	0	1.1375	0E	0	0	0	1	1	1	1.5250
4A	1	0	0	1	0	1	1.1500	0C	0	0	0	1	1	0	1.5375
48	1	0	0	1	0	0	1.1625	0A	0	0	0	1	0	1	1.5500
46	1	0	0	0	1	1	1.1750	08	0	0	0	1	0	0	1.5625
44	1	0	0	0	1	0	1.1875	06	0	0	0	0	1	1	1.5750
42	1	0	0	0	0	1	1.2000	04	0	0	0	0	1	0	1.5875
40	1	0	0	0	0	0	1.2125	02	0	0	0	0	0	1	1.6000
3E	0	1	1	1	1	1	1.2250	00	0	0	0	0	0	0	OFF[1]

NOTES:

1. When the “111111” VID pattern is observed, the voltage regulator output should be disabled.
2. The VID range includes VID transitions that may be initiated by thermal events, assertion of the FORCEPR# signal (see Section 5.2.4), Extended HALT state transitions (see Section 6.2.2), or Enhanced Intel SpeedStep® Technology transitions (see Section 6.3). **The Extended HALT state must be enabled for the processor to remain within its specifications.**
3. Once the VRM/EVRD is operating after power-up, if either the Output Enable signal is de-asserted or a specific VID off code is received, the VRM/EVRD must turn off its output (the output should go to high impedance) within 500 ms and latch off until power is cycled. Refer to *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.0 Design Guidelines*.

Table 2-4. Loadline Selection Truth Table for LL_ID[1:0]

LL_ID1	LL_ID0	Description
0	0	Reserved
0	1	Intel® Core™2 Extreme processor QX9775
1	0	Reserved
1	1	Reserved

NOTE: The LL_ID[1:0] signals are used to select the correct loadline slope for the processor.

Table 2-5. Market Segment Selection Truth Table for MS_ID[1:0]

MS_ID1	MS_ID0	Description
0	0	Reserved
0	1	Reserved
1	0	Reserved
1	1	Intel® Core™2 Extreme processor QX9775

NOTE: The MS_ID[1:0] signals are provided to indicate the Market Segment for the processor and may be used for future processor compatibility or for keying.

2.6 Reserved, Unused, and Test Signals

All Reserved signals must remain unconnected. Connection of these signals to V_{CC}, V_{TT}, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future processors. See Chapter 4 for a land listing of the processor and the location of all Reserved signals.

For reliable operation, always connect unused inputs or bidirectional signals to an appropriate signal level. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs can be left unconnected; however, this may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bidirectional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. For unused AGTL+ input or I/O signals, use pull-up resistors of the same value as the on-die termination resistors (R_{TT}). For details see Table 2-18.

TAP, CMOS Asynchronous inputs, and CMOS Asynchronous outputs do not include on-die termination. Inputs and utilized outputs must be terminated on the baseboard. Unused outputs may be terminated on the baseboard or left unconnected. Note that leaving unused outputs unterminated may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing.

The TESTHI signals must be tied to the processor V_{TT} using a matched resistor, where a matched resistor has a resistance value within ± 20% of the impedance of the board transmission line traces. For example, if the trace impedance is 50 Ω, then a value between 40 Ω and 60 Ω is required.

The TESTHI signals must use individual pull-up resistors as detailed below. A matched resistor must be used for each signal:

- TESTHI10 – cannot be grouped with other TESTHI signals
- TESTHI11 – cannot be grouped with other TESTHI signals
- TESTHI12 - cannot be grouped with other TESTHI signals

2.7 Front Side Bus Signal Groups

The FSB signals have been combined into groups by buffer type. AGTL+ input signals have differential input buffers, which use GTLREF_DATA and GTLREF_ADD as reference levels. In this document, the term “AGTL+ Input” refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, “AGTL+ Output” refers to the AGTL+ output group as well as the AGTL+ I/O group when driving. AGTL+ asynchronous outputs can become active anytime and include an active PMOS pull-up transistor to assist during the first clock of a low-to-high voltage transition.

With the implementation of a source synchronous data bus comes the need to specify two sets of timing parameters. One set is for common clock signals whose timings are specified with respect to rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.) and the second set is for the source synchronous signals which are relative to their respective strobe lines (data and address) as well as rising edge of BCLK0. Asynchronous signals are still present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle. Table 2-6 identifies which signals are common clock, source synchronous and asynchronous.

Table 2-6. FSB Signal Groups (Sheet 1 of 2)

Signal Group	Type	Signals[1]
AGTL+ Common Clock Input	Synchronous to BCLK[1:0]	BPRI#, DEFER#, RESET#, RS[2:0]#, RSP#, TRDY#;
AGTL+ Common Clock Output	Synchronous to BCLK[1:0]	BPM4#, BPM[2:1]#, BPMb[2:1]#
AGTL+ Common Clock I/O	Synchronous to BCLK[1:0]	ADS#, AP[1:0]#, BINIT#[2], BNR#[2], BPM5#, BPM3#, BPM0#, BPMb3#, BPMb0#, BR[1:0]#, DBSY#, DP[3:0]#, DRDY#, HIT#[2], HITM#[2], LOCK#, MCERR#[2]
AGTL+ Source Synchronous I/O	Synchronous to assoc. strobe	<table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>REQ[4:0]#, A[16:3]#, A[37:36]#</td><td>ADSTB0#</td></tr><tr><td>A[35:17]#</td><td>ADSTB1#</td></tr><tr><td>D[15:0]#, DBI0#</td><td>DSTBP0#, DSTBN0#</td></tr><tr><td>D[31:16]#, DBI1#</td><td>DSTBP1#, DSTBN1#</td></tr><tr><td>D[47:32]#, DBI2#</td><td>DSTBP2#, DSTBN2#</td></tr><tr><td>D[63:48]#, DBI3#</td><td>DSTBP3#, DSTBN3#</td></tr></table>
AGTL+ Strobes I/O	Synchronous to BCLK[1:0]	ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#
Open Drain Output	Asynchronous	FERR#/PBE#, IERR#, PROCHOT#, THERMTRIP#, TDO
CMOS Asynchronous Input	Asynchronous	A20M#, FORCEPR#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, STPCLK#
CMOS Asynchronous Output	Asynchronous	BSEL[2:0], VID[6:1]
FSB Clock	Clock	BCLK[1:0]

Table 2-6. FSB Signal Groups (Sheet 2 of 2)

Signal Group	Type	Signals[1]
TAP Input	Synchronous to TCK	TCK, TDI, TMS, TRST#
TAP Output	Synchronous to TCK	TDO
Power/Other	Power/Other	COMP[3:0], GTLREF_ADD_MID, GTLREF_ADD_END, GTLREF_DATA_MID, GTLREF_DATA_END, LL_ID[1:0], MS_ID[1:0], PECI, RESERVED, SKTOCC#, TESTIN1, TESTIN2, TESTHI[12:10], V_{CC}, VCC_DIE_SENSE, VCC_DIE_SENSE2, VCCPLL, VID_SELECT, VSS_DIE_SENSE, VSS_DIE_SENSE2, V_{SS}, V_{TT}, VTT_OUT, VTT_SEL

NOTES:
1. Refer to Section 4.2 for signal descriptions.
2. These signals may be driven simultaneously by multiple agents (Wired-OR).

Table 2-7 outlines the signals which include on-die termination (R_{TT}). Table 2-8 outlines non AGTL+ signals including open drain signals. Table 2-9 provides signal reference voltages.

Table 2-7. AGTL+ Signal Description Table

AGTL+ signals with R_{TT}	AGTL+ signals with no R_{TT}
A[37:3]#, ADS#, ADSTB[1:0]#, AP[1:0]#, BINIT#, BNR#, BPRI#, D[63:0]#, DBI[3:0]#, DBSY#, DEFER#, DP[3:0]#, DRDY#, DSTBN[3:0]#, DSTBP[3:0]#, HIT#, HITM#, LOCK#, MCERR#, REQ[4:0]#, RS[2:0]#, RSP#, TRDY#	BPM[5:0]#, BPMb[3:0]#, RESET#, BR[1:0]#

Table 2-8. Non AGTL+ Signal Description Table

Signals with R_{TT}	Signals with no R_{TT}
FORCEPR#[1], PROCHOT#[2]	A20M#, BCLK[1:0], BSEL[2:0], COMP[3:0], FERR#/PBE#, GTLREF_ADD_MID, GTLREF_ADD_END, GTLREF_DATA_MID, GTLREF_DATA_END, IERR#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, LL_ID[1:0], MS_ID[1:0], PECI, PWRGOOD, SKTOCC#, SMI#, STPCLK#, TCK, TDI, TDO, TESTHI[12:8], THERMTRIP#, TMS, TRDY#, TRST#, VCC_DIE_SENSE, VCC_DIE_SENSE2, VID[6:1], VID_SELECT, VSS_DIE_SENSE, VSS_DIE_SENSE2, VTT_SEL

NOTES:
1. These signals have R_{TT} in the package with a 80 Ω pullup to V_{TT}.
2. These signals have R_{TT} in the package with a 50 Ω pullup to V_{TT}.

Table 2-9. Signal Reference Voltages

GTLREF	CMOS
A[37:3]#, ADS#, ADSTB[1:0]#, AP[1:0]#, BINIT#, BNR#, BPM[5:0]#, BPMb[3:0]#,BPRI#, BR[1:0]#, D[63:0]#, DBI[3:0]#, DBSY#, DEFER#, DP[3:0]#, DRDY#, DSTBN[3:0]#, DSTBP[3:0]#, FORCEPR#, HIT#, HITM#, LOCK#, MCERR#, RESET#, REQ[4:0]#, RS[2:0]#, RSP#, TRDY#	A20M#, LINT0/INTR, LINT1/NMI, IGNNE#, INIT#, PWRGOOD, SMI#, STPCLK#, TCK, TDI, TMS, TRST#

2.8 CMOS Asynchronous and Open Drain Asynchronous Signals

Legacy input signals such as A20M#, IGNNE#, INIT#, SMI#, and STPCLK# utilize CMOS input buffers. Legacy output signals such as FERR#/PBE#, IERR#, PROCHOT#, and THERMTRIP# utilize open drain output buffers. All of the CMOS and Open Drain signals are required to be asserted/deasserted for at least eight BCLKs in order for the processor to recognize the proper signal state. See Section 2.13 for the DC specifications. See Chapter 5 for additional timing requirements for entering and leaving the low power states.

2.9 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, it is recommended that the processor(s) be first in the TAP chain followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage. Similar considerations must be made for TCK, TDO, TMS, and TRST#. Two copies of each signal may be required with each driving a different voltage level.

2.10 Platform Environmental Control Interface (PECI) DC Specifications

PECI is an Intel proprietary one-wire interface that provides a communication channel between Intel processors and chipset components to external thermal monitoring devices. The processor contains Digital Thermal Sensor (DTS) sprinkled both inside and outside the cores in a die. These sensors are implemented as analog-to-digital converters calibrated at the factory for reasonable accuracy to provide a digital representation of relative processor temperature. PECI provides an interface to relay the highest DTS temperature within a die to external devices for thermal/fan speed control. More detailed information may be found in the *Platform Environment Control Interface (PECI) Specification.*

2.10.1 DC Characteristics

The PECI interface operates at a nominal voltage set by V_{TT}. The set of DC electrical specifications shown in Table 2-10 is used with devices normally operating from a V_{TT} interface supply. V_{TT} nominal levels will vary between processor families. All PECI devices will operate at the V_{TT} level determined by the processor installed in the system. For specific nominal V_{TT} levels, refer to Table 2-3.

Table 2-10. PECI DC Electrical Limits

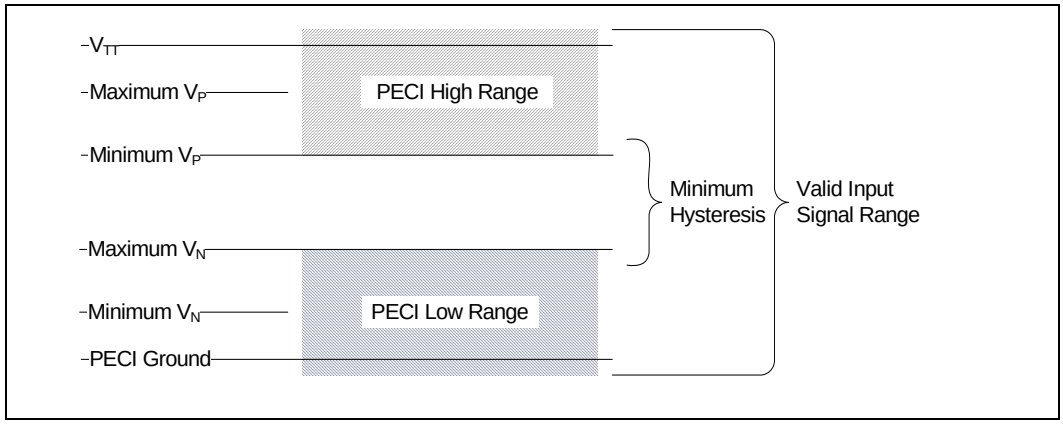
Symbol	Definition and Conditions	Min	Max	Units	Notes[1]
V_{in}	Input Voltage Range	-0.150	V_{TT}	V	
$V_{hysteresis}$	Hysteresis	0.1 * V_{TT}	N/A	V	
V_n	Negative-edge threshold voltage	0.275 * V_{TT}	0.500 * V_{TT}	V	
V_p	Positive-edge threshold voltage	0.550 * V_{TT}	0.725 * V_{TT}	V	
I_{source}	High level output source (V_{OH} = 0.75 * V_{TT})	-6.0	N/A	mA	
I_{sink}	Low level output sink (V_{OL} = 0.25 * V_{TT})	0.5	1.0	mA	
I_{leak+}	High impedance state leakage to V_{TT} (V_{leak} = V_{OL})	N/A	50	µA	2
I_{leak-}	High impedance leakage to GND (V_{leak} = V_{OH})	N/A	10	µA	2
C_{bus}	Bus capacitance per node	N/A	10	pF	3
V_{noise}	Signal noise immunity above 300 MHz	0.1 * V_{TT}	N/A	V_{p-p}	

NOTE:
1. V_{TT} supplies the PECI interface. PECI behavior does not affect V_{TT} min/max specifications.
2. The leakage specification applies to powered devices on the PECI bus.
3. One node is counted for each client and one node for the system host. Extended trace lengths might appear as additional nodes.

2.10.2 Input Device Hysteresis

The input buffers in both client and host models must use a Schmitt-triggered input design for improved noise immunity. Use Figure 2-1 as a guide for input buffer design.

Figure 2-1. Input Device Hysteresis



2.11 Mixing Processors

Intel supports and validates dual processor configurations only in which both processors operate with the same FSB frequency, core frequency, power segments, and have the same internal cache sizes. Mixing components operating at different internal clock frequencies is not supported and will not be validated by Intel. Combining processors from different power segments is also not supported.

Note: Processors within a system must operate at the same frequency per bits [12:8] of the CLOCK_FLEX_MAX MSR; however this does not apply to frequency transitions initiated due to thermal events, Extended HALT, Enhanced Intel SpeedStep Technology transitions, or assertion of the FORCEPR# signal (See Chapter 5).

Not all operating systems can support dual processors with mixed frequencies. Mixing processors of different steppings but the same model (as per CPUID instruction) is supported. Details regarding the CPUID instruction are provided in the *AP-485 Intel® Processor Identification and the CPUID Instruction* application note.

2.12 Absolute Maximum and Minimum Ratings

Table 2-11 specifies absolute maximum and minimum ratings only, which lie outside the functional limits of the processor. Only within specified operation limits, can functionality and long-term reliability be expected.

At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time then, when returned to conditions within the functional operating condition limits, it will either not function or its reliability will be severely degraded.

Although the processor contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

Table 2-11. Processor Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes[1, 2]
V_{CC}	Core voltage with respect to V_{SS}	-0.30	1.35	V	
V_{TT}	FSB termination voltage with respect to V_{SS}	-0.30	1.45	V	
T_{CASE}	Processor case temperature	See Chapter 5	See Chapter 5	°C	
$T_{STORAGE}$	Storage temperature	-40	85	°C	3, 4, 5

NOTES:
1. For functional operation, all processor electrical, signal quality, mechanical and thermal specifications must be satisfied.
2. Excessive overshoot or undershoot on any signal will likely result in permanent damage to the processor.
3. Storage temperature is applicable to storage conditions only. In this scenario, the processor must not receive a clock, and no lands can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. For functional operation, please refer to the processor case temperature specifications.
4. This rating applies to the processor and does not include any tray or packaging.
5. Failure to adhere to this specification can affect the long-term reliability of the processor.

2.13 Processor DC Specifications

The processor DC specifications in this section are defined at the processor die (pads) unless noted otherwise. See Chapter 4 for the processor land listings and signal definitions. Voltage and current specifications are detailed in Table 2-12. For platform planning refer to Table 2-13, which provides V_{CC} static and transient tolerances. This same information is presented graphically in Figure 2-3.

The FSB clock signal group is detailed in Table 2-19. BSEL[2:0] and VID[6:1] signals are specified in Table 2-14. The DC specifications for the AGTL+ signals are listed in Table 2-15. Legacy signals and Test Access Port (TAP) signals follow DC specifications similar to GTL+. The DC specifications for the PWRGOOD input and TAP signal group are listed in Table 2-15.

Table 2-12 through Table 2-17 list the DC specifications for the processor and are valid only while meeting specifications for case temperature (T_{CASE} as specified in Chapter 5, “Thermal Specifications”), clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Table 2-12. Voltage and Current Specifications

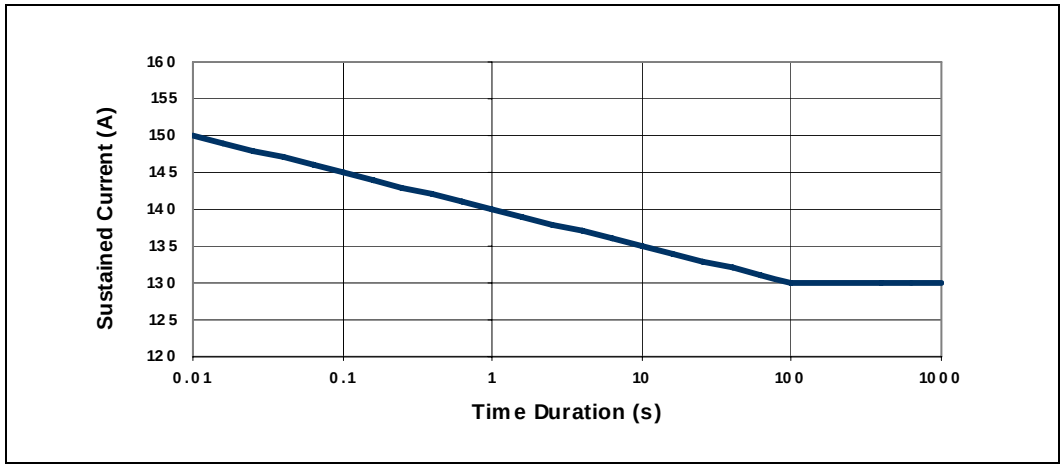
Symbol	Parameter		Min	Typ	Max	Unit	Notes [1, 10]
VID	VID range		0.850	—	1.3500	V	
V_{CC}	Processor Number: QX9775	V_{CC} for processor core 3.2 GHz	See Table 2-13 and Figure 2-3			V	2, 3, 4, 8, 18
V_{cc_boot}	Default VCC Voltage for initial power up		—	1.10	—	V	2
V_{VID_STEP}	VID step size during a transition		—	—	±12.5	mV	
V_{VID_SHIFT}	Total allowable DC load line shift from VID steps		—	—	450	mV	9
V_{TT}	FSB termination voltage (DC + AC specification)		1.045	1.10	1.155	V	7,12
V_{CCPLL}	PLL supply voltage (DC + AC specification)		1.455	1.500	1.605	V	11
I_{CC}	Processor Number: QX9775	I_{CC} processor core with multiple VID" 3.2 GHz	—	—	150	A	4,5,8,17, 18
I_{CC_RESET}	Processor Number: QX9775	I_{CC_RESET} core with multiple VID: 3.2 GHz	—	—	150	A	16,17
I_{TT}	I_{CC} for V_{TT} supply before V_{CC} stable I_{CC} for V_{TT} supply after V_{CC} stable		—	—	8 7	A	14
I_{CC_TDC}	Processor Number: QX9775	Thermal Design Current (TDC): 3.2 GHz	—	—	130	A	13,17,18
$I_{CC\_VTT\_OUT}$	DC current that may be drawn from V_{TT_OUT} per land		—	—	580	mA	15
I_{CC_GTLREF}	I_{CC} for GTLREF_DATA_MID, GTLREF_DATA_END, GTLREF_ADD_MID, and GTLREF_ADD_END		—	—	200	µA	6
I_{CC_VCCPLL}	I_{CC} for PLL supply		—	—	260	mA	11
I_{TCC}	I_{CC} during active thermal control circuit (TCC)		—	—	150	A	17

NOTES:

1. Unless otherwise noted, all specifications in this table are based on final silicon characterization data.
2. These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required. See Section 2.5 for more information.
3. The voltage specification requirements are measured across the VCC_DIE_SENSE and VSS_DIE_SENSE lands and across the VCC_DIE_SENSE2 and VSS_DIE_SENSE2 lands with an oscilloscope set to 100 MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
4. The processor must not be subjected to any static V_{CC} level that exceeds the V_{CC_MAX} associated with any particular current. Failure to adhere to this specification can shorten processor lifetime.
5. I_{CC_MAX} specification is based on maximum V_{CC} loadline. Refer to Figure 2-3 for details. The processor is capable of drawing I_{CC_MAX} for up to 10 ms. Refer to Figure 2-1 for further details on the average processor current draw over various time durations.
6. This specification represents the total current for.
7. V_{TT} must be provided via a separate voltage source and must not be connected to V_{CC}. This specification is measured at the land.

8. Minimum V_{CC} and maximum I_{CC} are specified at the maximum processor case temperature (TCASE) shown in Figure 5-1.
9. This specification refers to the total reduction of the load line due to VID transitions below the specified VID.
10. Individual processor VID values may be calibrated during manufacturing such that two devices at the same frequency may have different VID settings.
11. This specification applies to the VCCPLL land.
12. Baseboard bandwidth is limited to 20 MHz.
13. I_{CC_TDC} is the sustained (DC equivalent) current that the processor is capable of drawing indefinitely and should be used for the voltage regulator temperature assessment. The voltage regulator is responsible for monitoring its temperature and asserting the necessary signal to inform the processor of a thermal excursion. The processor is capable of drawing I_{CC_TDC} indefinitely. Refer to Figure 2-1 for further details on the average processor current draw over various time durations. This parameter is based on design characterization and is not tested.
14. This is the maximum total current drawn from the V_{TT} plane by only one processor with R_{TT} enabled. This specification does not include the current coming from on-board termination (R_{TT}), through the signal line. Refer to the Voltage Regulator Design Guidelines to determine the total I_{TT} drawn by the system. This parameter is based on design characterization and is not tested.
15. $I_{CC\_VTT\_OUT}$ is specified at 1.1 V.
16. I_{CC_RESET} is specified while PWRGOOD and RESET# are asserted.
17. The processor is intended for dual processor workstations only.

Figure 2-2. Processor Load Current versus Time



NOTES:
1. Processor or Voltage Regulator thermal protection circuitry should not trip for load currents greater than I_{CC_TDC}.
2. Not 100% tested. Specified by design characterization.

Table 2-13. Processor V_{CC} Static and Transient Tolerance

I_{CC} (A)	V_{CC_Max} (V)	V_{CC_Typ} (V)	V_{CC_Min} (V)	Notes
0	VID - 0.000	VID - 0.010	VID - 0.020	1,2,3
5	VID - 0.006	VID - 0.016	VID - 0.026	1,2,3
10	VID - 0.013	VID - 0.023	VID - 0.033	1,2,3
15	VID - 0.019	VID - 0.029	VID - 0.039	1,2,3
20	VID - 0.025	VID - 0.035	VID - 0.045	1,2,3
25	VID - 0.031	VID - 0.041	VID - 0.051	1,2,3
30	VID - 0.038	VID - 0.048	VID - 0.058	1,2,3
35	VID - 0.044	VID - 0.054	VID - 0.064	1,2,3
40	VID - 0.050	VID - 0.060	VID - 0.070	1,2,3
45	VID - 0.056	VID - 0.066	VID - 0.076	1,2,3
50	VID - 0.063	VID - 0.073	VID - 0.083	1,2,3
55	VID - 0.069	VID - 0.079	VID - 0.089	1,2,3
60	VID - 0.075	VID - 0.085	VID - 0.095	1,2,3
65	VID - 0.081	VID - 0.091	VID - 0.101	1,2,3
70	VID - 0.087	VID - 0.097	VID - 0.108	1,2,3
75	VID - 0.094	VID - 0.104	VID - 0.114	1,2,3
80	VID - 0.100	VID - 0.110	VID - 0.120	1,2,3
85	VID - 0.106	VID - 0.116	VID - 0.126	1,2,3
90	VID - 0.113	VID - 0.123	VID - 0.133	1,2,3
95	VID - 0.119	VID - 0.129	VID - 0.139	1,2,3
100	VID - 0.125	VID - 0.135	VID - 0.145	1,2,3
105	VID - 0.131	VID - 0.141	VID - 0.151	1,2,3
110	VID - 0.138	VID - 0.148	VID - 0.158	1,2,3
115	VID - 0.144	VID - 0.154	VID - 0.164	1,2,3
120	VID - 0.150	VID - 0.160	VID - 0.170	1,2,3
125	VID - 0.156	VID - 0.166	VID - 0.176	1,2,3
130	VID - 0.163	VID - 0.173	VID - 0.183	1,2,3
135	VID - 0.169	VID - 0.179	VID - 0.189	1,2,3
140	VID - 0.175	VID - 0.185	VID - 0.195	1,2,3
145	VID - 0.181	VID - 0.191	VID - 0.201	1,2,3
150	VID - 0.188	VID - 0.198	VID - 0.208	1,2,3

NOTES:

1. The V_{CC_MIN} and V_{CC_MAX} loadlines represent static and transient limits. See Section 2.13.1 for V_{CC} overshoot specifications.
2. This table is intended to aid in reading discrete points on Figure 2-3.
3. The loadlines specify voltage limits at the die measured at the VCC_DIE_SENSE and VSS_DIE_SENSE lands and across the VCC_DIE_SENSE2 and VSS_DIE_SENSE2 lands. Voltage regulation feedback for voltage regulator circuits must also be taken from processor VCC_DIE_SENSE and VSS_DIE_SENSE lands and VCC_DIE_SENSE2 and VSS_DIE_SENSE2 lands. Refer to the *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator Down (EVRD) 11.0 Design Guidelines* for socket load line guidelines and VR implementation.

Figure 2-3. Processor V_{CC} Static and Transient Tolerance Load Lines

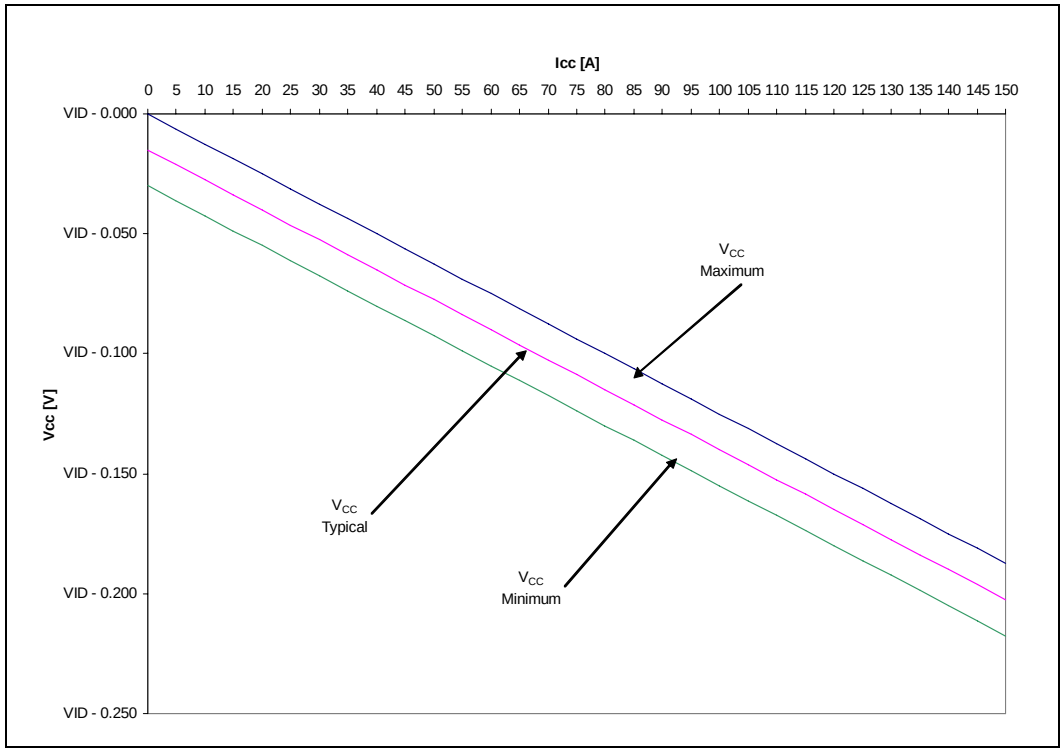


Table 2-14. AGTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{IL}	Input Low Voltage	-0.10	0	GTLREF–0.10	V	2,4,6
V_{IH}	Input High Voltage	GTLREF+0.10	V_{TT}	V_{TT}+0.10	V	3,6
V_{OH}	Output High Voltage	V_{TT}-0.10	N/A	V_{TT}	V	4,6
R_{ON}	Buffer On Resistance	8.25	10.25	12.25	Ω	5
I_{LI}	Input Leakage Current	N/A	N/A	± 100	µA	7

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{OH} may experience excursions above V_{TT}. However, input signal drivers must comply with the signal quality specifications.
5. This is the pull down driver resistance. Measured at 0.31*V_{TT}. R_{ON} (min) = 0.158*R_{TT}. R_{ON} (typ) = 0.167*R_{TT}.
   R_{ON} (max) = 0.175*R_{TT}.
6. GTLREF should be generated from V_{TT} with a 1% tolerance resistor divider. The V_{TT} referred to in these specifications is the instantaneous V_{TT}.
7. Specified when on-die R_{TT} and R_{ON} are turned off. V_{IN} between 0 and V_{TT}.

Table 2-15. CMOS Signal Input/Output Group and TAP Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{IL}	Input Low Voltage	-0.10	0.00	0.3 * V_{TT}	V	2,6
V_{IH}	Input High Voltage	0.7 * V_{TT}	V_{TT}	V_{TT} + 0.1	V	2
V_{OL}	Output Low Voltage	-0.10	0	0.1 * V_{TT}	V	2
V_{OH}	Output High Voltage	0.9 * V_{TT}	V_{TT}	V_{TT} + 0.1	V	2
I_{OL}	Output Low Current	1.70	N/A	4.70	mA	3
I_{OH}	Output High Current	1.70	N/A	4.70	mA	4
I_{LI}	Input Leakage Current	N/A	N/A	± 100	µA	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The V_{TT} referred to in these specifications refers to instantaneous V_{TT}.
3. Measured at 0.1*V_{TT}.
4. Measured at 0.9*V_{TT}.
5. For Vin between 0 V and V_{TT}. Measured when the driver is tristated.

Table 2-16. Open Drain Output Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{OL}	Output Low Voltage	0	N/A	0.20 * V_{TT}	V	
V_{OH}	Output High Voltage	0.95 * V_{TT}	V_{TT}	1.05 * V_{TT}	V	3
I_{OL}	Output Low Current	16	N/A	50	mA	2
I_{LO}	Leakage Current	N/A	N/A	± 200	µA	4

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Measured at 0.2*V_{TT}.
3. V_{OH} is determined by value of the external pullup resistor to V_{TT}.
4. For V_{IN} between 0 V and V_{OH}.

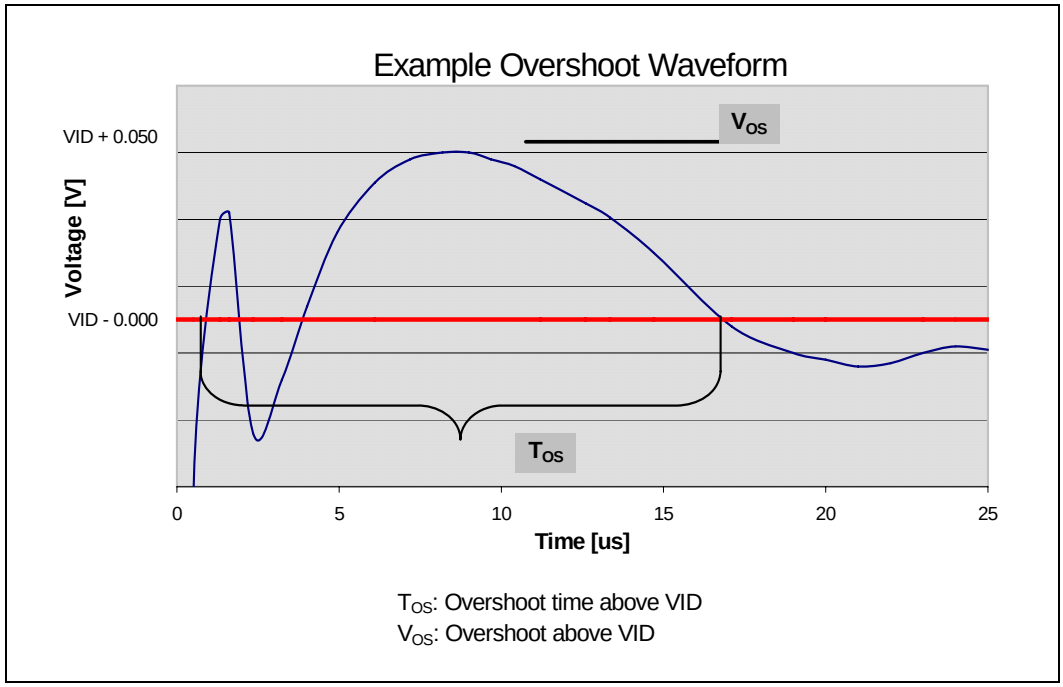
2.13.1 V_{CC} Overshoot Specification

The processor can tolerate short transient overshoot events where V_{CC} exceeds the VID voltage when transitioning from a high-to-low current load condition. This overshoot cannot exceed VID + V_{OS_MAX} (V_{OS_MAX} is the maximum allowable overshoot above VID). These specifications apply to the processor die voltage as measured across the VCC_DIE_SENSE and VSS_DIE_SENSE lands and across the VCC_DIE_SENSE2 and VSS_DIE_SENSE2 lands.

Table 2-17. V_{CC} Overshoot Specifications

Symbol	Parameter	Min	Max	Units	Figure	Notes
V_{OS_MAX}	Magnitude of V_{CC} overshoot above VID	—	50	mV	2-4	
T_{OS_MAX}	Time duration of V_{CC} overshoot above VID	—	25	µs	2-4	

Figure 2-4. V_{CC} Overshoot Example Waveform



NOTES:
1. V_{OS} is the measured overshoot voltage.
2. T_{OS} is the measured time duration above VID.

2.13.2 Die Voltage Validation

Core voltage (VCC) overshoot events at the processor must meet the specifications in Table 2-17 when measured across the VCC_DIE_SENSE and VSS_DIE_SENSE lands and across the VCC_DIE_SENSE2 and VSS_DIE_SENSE2 lands. Overshoot events that are < 10 ns in duration may be ignored. These measurements of processor die level overshoot should be taken with a 100 MHz bandwidth limited oscilloscope.

2.14 AGTL+ FSB Specifications

Routing topologies are dependent on the processors supported and the chipset used in the design. In most cases, termination resistors are not required as these are integrated into the processor silicon. See Table 2-8 for details on which signals do not include on-die termination. Refer to Table 2-18 for R_{TT} values.

Valid high and low levels are determined by the input buffers via comparing with a reference voltage called GTLREF_DATA_MID, GTLREF_DATA_END, GTLREF_ADD_MID, and GTLREF_ADD_END. GTLREF_DATA_MID and GTLREF_DATA_END is the reference voltage for the FSB 4X data signals, GTLREF_ADD_MID, and GTLREF_ADD_END is the reference voltage for the FSB 2X address signals and common clock signals. Table 2-18 lists the GTLREF_DATA_MID, GTLREF_DATA_END, GTLREF_ADD_MID, and GTLREF_ADD_END specifications.

The AGTL+ reference voltages (GTLREF_DATA_MID, GTLREF_DATA_END, GTLREF_ADD_MID, and GTLREF_ADD_END) must be generated on the baseboard using high precision voltage divider circuits.

Table 2-18. AGTL+ Bus Voltage Definitions

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
GTLREF_DATA_MID, GTLREF_DATA_END	Data Bus Reference Voltage	0.98 * 0.667 * V_{TT}	0.667 * V_{TT}	1.02*0.667 * V_{TT}	V	2, 3
GTLREF_ADD_MID, GTLREF_ADD_END	Address Bus Reference Voltage	0.98 * 0.667 * V_{TT}	0.667 * V_{TT}	1.02*0.667 * V_{TT}	V	2, 3
R_{TT}	Termination Resistance (pull up)	45	50	55	Ω	4
COMP	COMP Resistance	49.4	49.9	50.4	Ω	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The tolerances for this specification have been stated generically to enable system designer to calculate the minimum values across the range of V_{TT}.
3. GTLREF_DATA_MID, GTLREF_DATA_END, GTLREF_ADD_MID, and GTLREF_ADD_END is generated from V_{TT} on the baseboard by a voltage divider of 1% resistors. The minimum and maximum specifications account for this resistor tolerance. The V_{TT} referred to in these specifications is the instantaneous V_{TT}.
4. R_{TT} is the on-die termination resistance measured at V_{OL} of the AGTL+ output driver. Measured at 0.31*V_{TT}. R_{TT} is connected to V_{TT} on die.
5. COMP resistance must be provided on the system board with 1% resistors.

Table 2-19. FSB Differential BCLK Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Figure	Notes[1]
V_L	Input Low Voltage	-0.150	0.0	0.150	V	2-5	
V_H	Input High Voltage	0.660	0.710	0.850	V	2-5	
$V_{CROSS(abs)}$	Absolute Crossing Point	0.250	0.350	0.550	V	2-5, 2-6	2,9
$V_{CROSS(rel)}$	Relative Crossing Point	0.250 + 0.5 * (V_{Havg} – 0.700)	N/A	0.550 + 0.5 * (V_{Havg} – 0.700)	V	2-5, 2-6	3,8,9,11
Δ_{VCROSS}	Range of Crossing Points	N/A	N/A	0.140	V	2-5, 2-6	
V_{OS}	Overshoot	N/A	N/A	1.150	V	2-5	4
V_{US}	Undershoot	-0.300	N/A	N/A	V	2-5	5
V_{RBM}	Ringback Margin	0.200	N/A	N/A	V	2-5	6
V_{TR}	Threshold Region	V_{CROSS} - 0.100	N/A	V_{CROSS} + 0.100	V	2-5	7
I_{LI}	Input Leakage Current	N/A	N/A	± 100	µA		10
ERRefclk-diffRrise ERRefclk-diff-Fall	Differential Rising and falling edge rates	0.6		4	V/ns	2-7	12

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Crossing Voltage is defined as the instantaneous voltage value when the rising edge of BCLK0 is equal to the falling edge of BCLK1.
3. V_{Havg} is the statistical average of the V_H measured by the oscilloscope.
4. Overshoot is defined as the absolute value of the maximum voltage.
5. Undershoot is defined as the absolute value of the minimum voltage.
6. Ringback Margin is defined as the absolute voltage difference between the maximum Rising Edge Ringback and the maximum Falling Edge Ringback.
7. Threshold Region is defined as a region entered around the crossing point voltage in which the differential receiver switches. It includes input threshold hysteresis.
8. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
9. V_{Havg} can be measured directly using “Vtop” on Agilent and “High” on Tektronix oscilloscopes.
10. For V_{IN} between 0 V and V_H.
11. ΔV_{CROSS} is defined as the total variation of all crossing voltages as defined in note 3.
12. Measured from -200 mV to +200 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 2-7.

Figure 2-5. Differential Clock Waveform

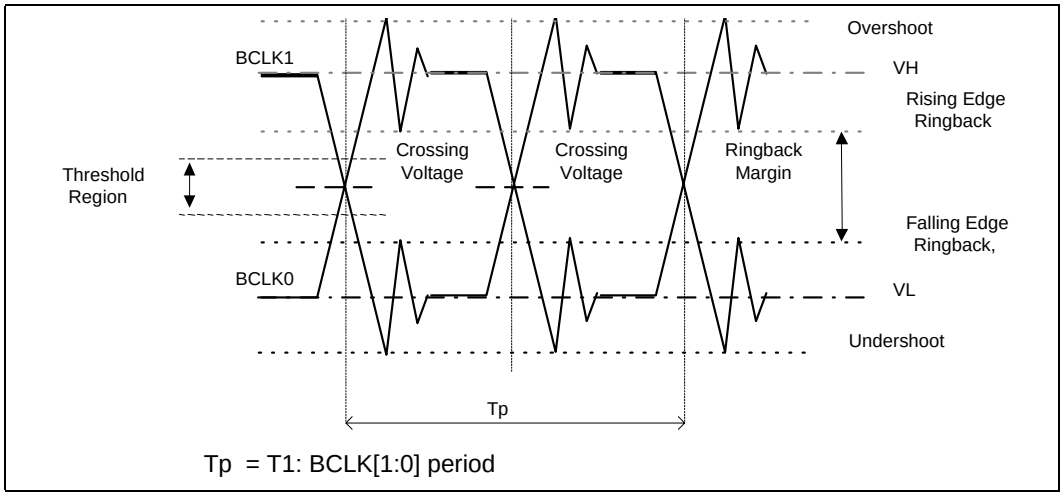


Figure 2-6. Differential Clock Crosspoint Specification

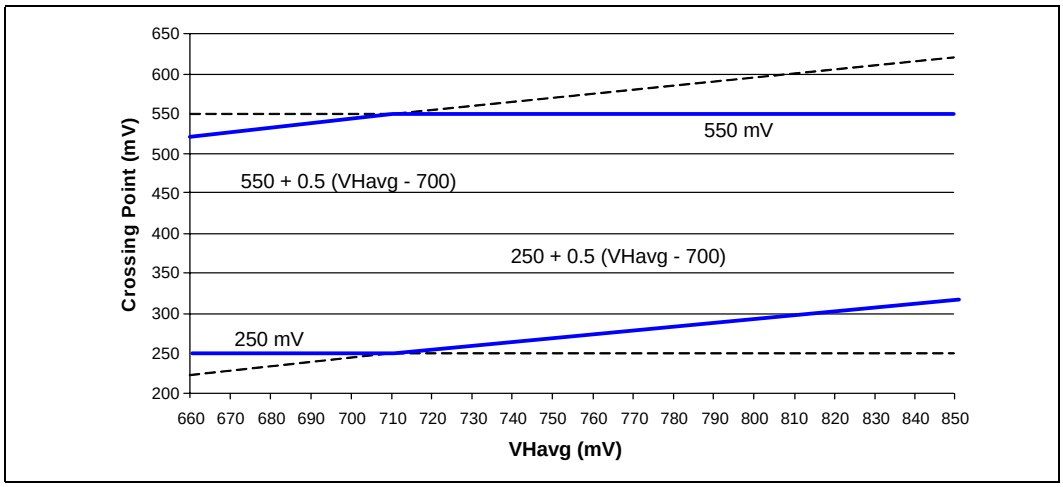
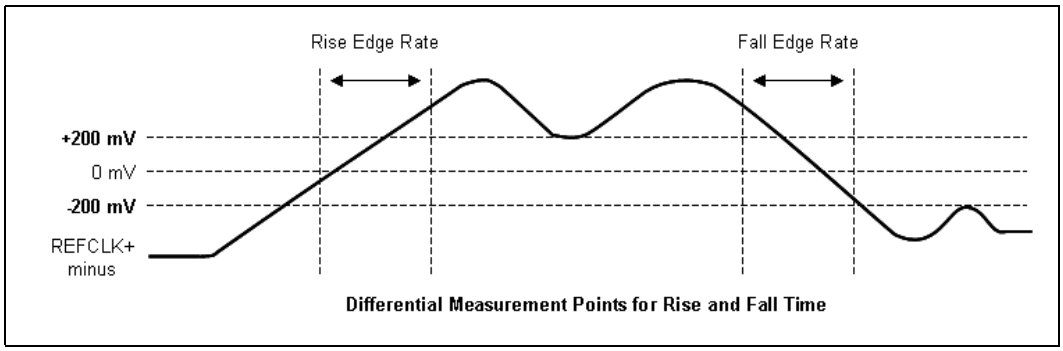


Figure 2-7. Differential Rising and Falling Edge Rates



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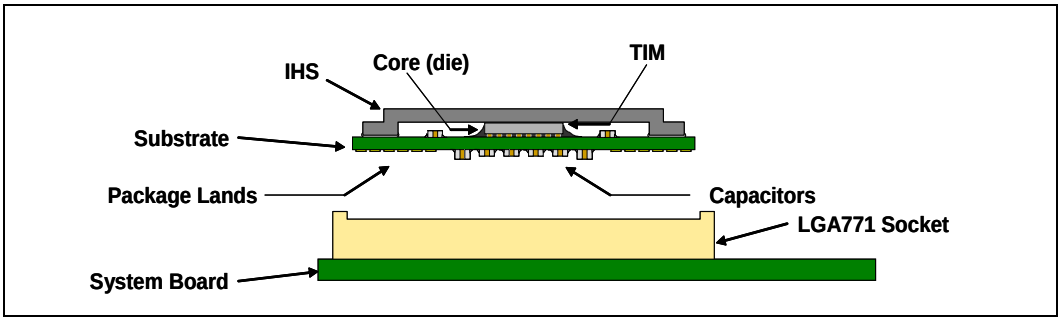
3 Mechanical Specifications

The processor is packaged in a Flip Chip Land Grid Array (FC-LGA) package that interfaces to the baseboard via a LGA771 socket. The package consists of a processor core mounted on a pinless substrate with 771 lands. An integrated heat spreader (IHS) is attached to the package substrate and core and serves as the interface for processor component thermal solutions such as a heatsink. Figure 3-1 shows a sketch of the processor package components and how they are assembled together. Refer to the *LGA771 Socket Design Guidelines* for complete details on the LGA771 socket.

The package components shown in Figure 3-1 include the following:

- Integrated Heat Spreader (IHS)
- Thermal Interface Material (TIM)
- Processor Core (die)
- Package Substrate
- Landside capacitors
- Package Lands

Figure 3-1. Processor Package Assembly Sketch



NOTE: This drawing is not to scale and is for reference only.

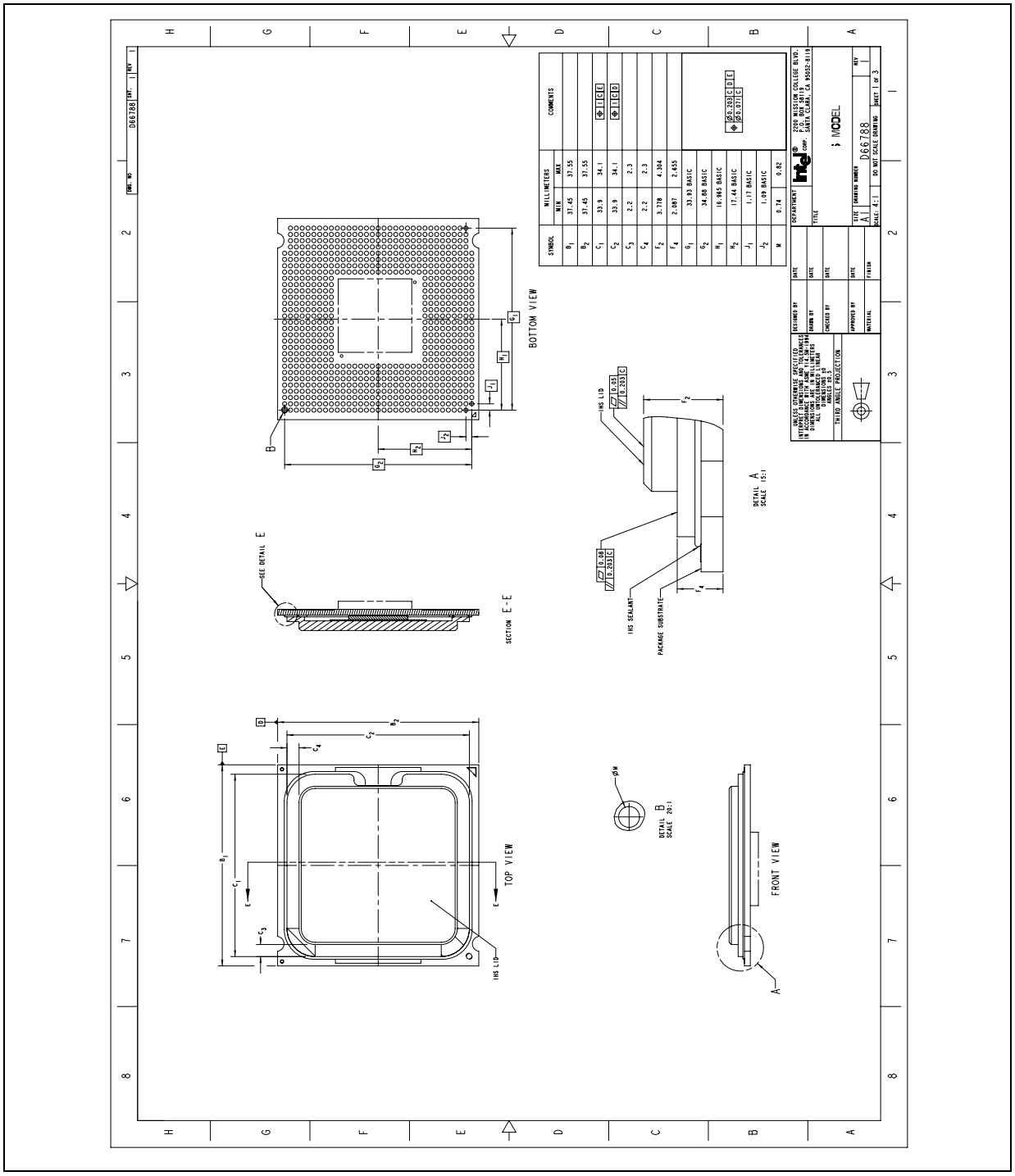
3.1 Package Mechanical Drawings

The package mechanical drawings are shown in Figure 3-2 through Figure 3-4. The drawings include dimensions necessary to design a thermal solution for the processor including:

- Package reference and tolerance dimensions (total height, length, width, and so forth)
- IHS parallelism and tilt
- Land dimensions
- Top-side and back-side component keepout dimensions
- Reference datums

Note: All drawing dimensions are in mm [in.].

Figure 3-2. Processor Package Drawing (Sheet 1 of 3)



NOTE: Guidelines on potential IHS flatness variation with socket load plate actuation and installation of the cooling solution is available in the processor Thermal and Mechanical Design Guidelines (See Section 1.2).

Figure 3-3. Processor Package Drawing (Sheet 2 of 3)

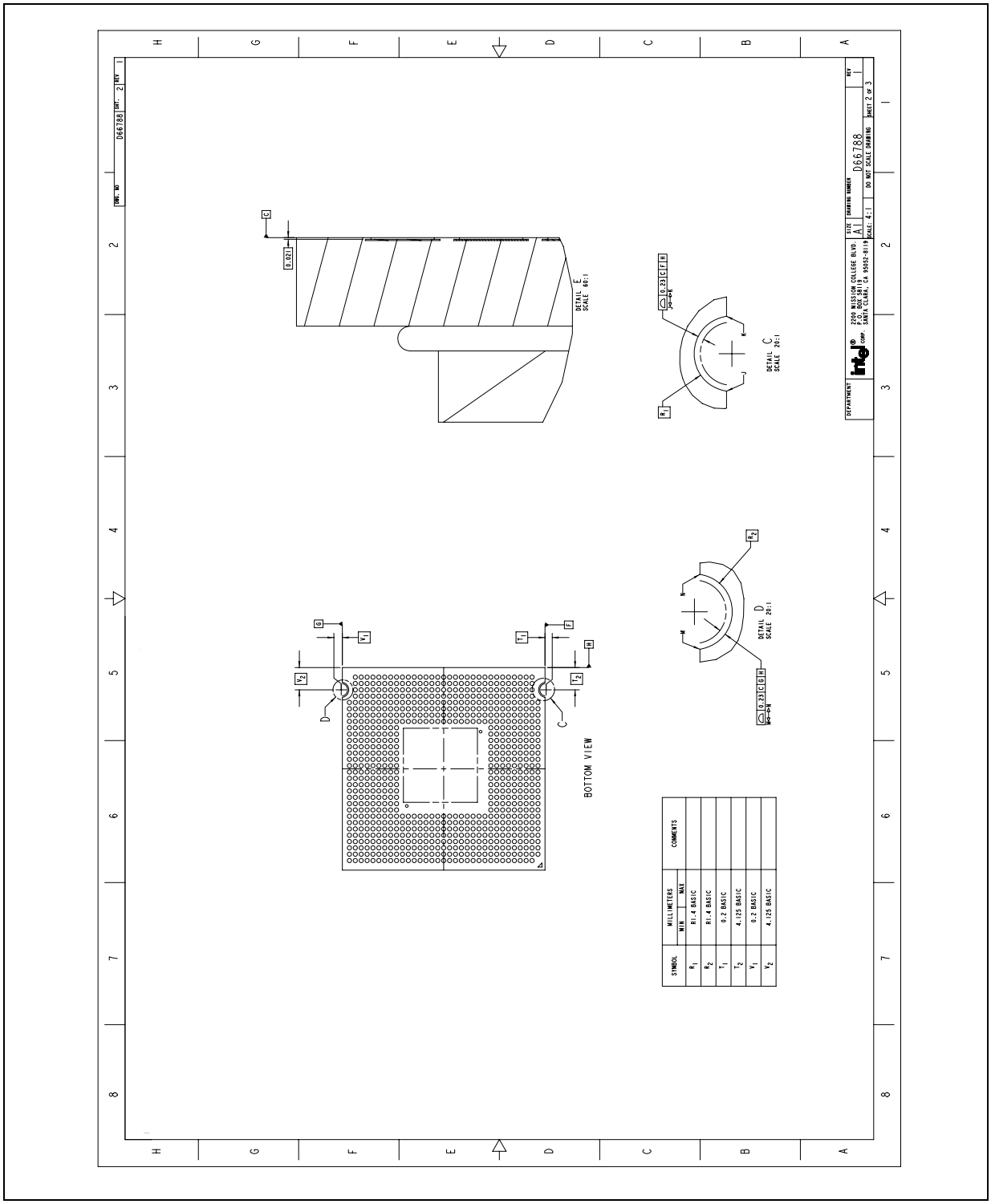
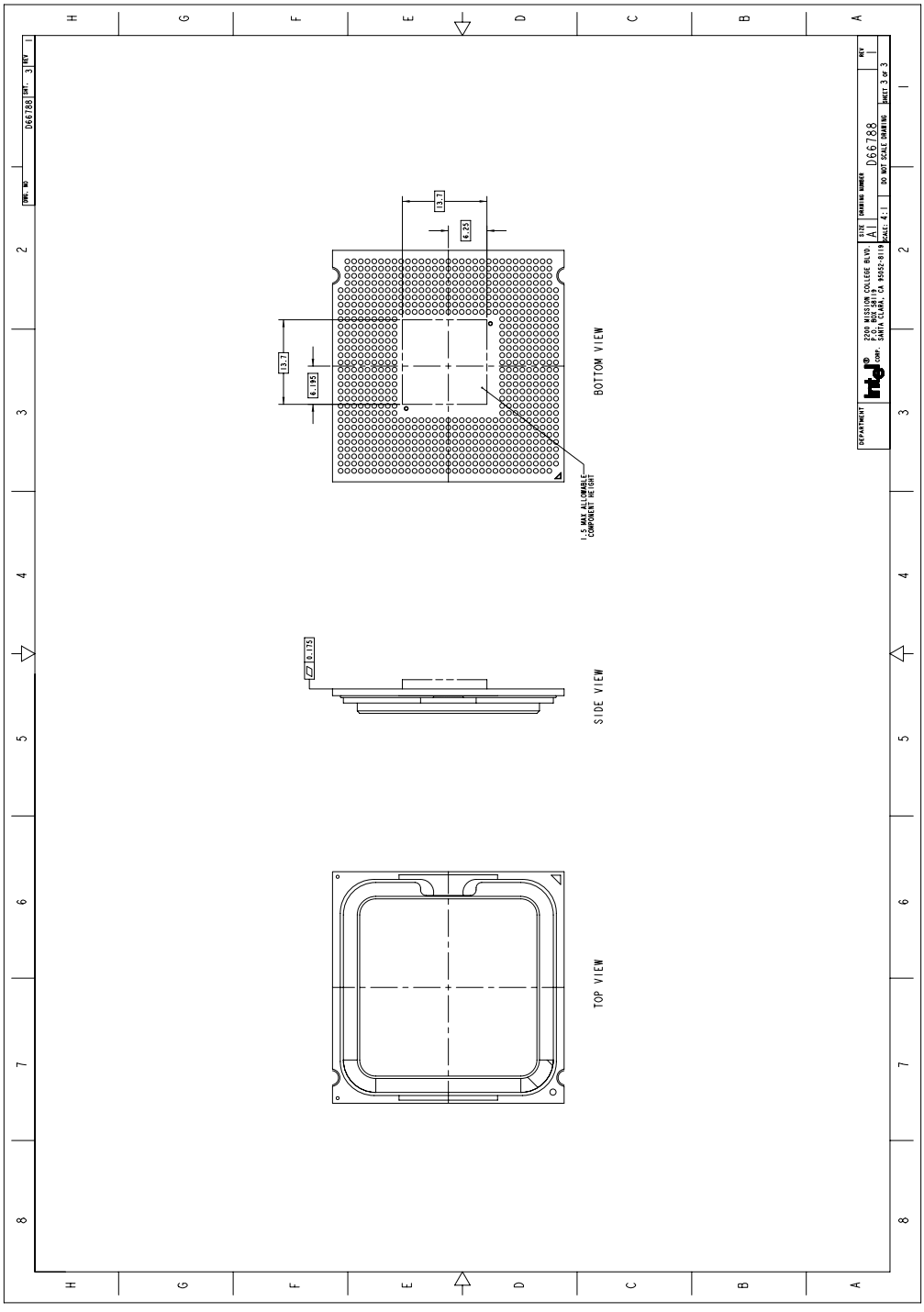


Figure 3-4. Processor Package Drawing (Sheet 3 of 3)



3.2 Processor Component Keepout Zones

The processor may contain components on the substrate that define component keepout zone requirements. Decoupling capacitors are typically mounted to either the topside or landside of the package substrate. See Figure 3-4 for keepout zones.

3.3 Package Loading Specifications

Table 3-1 provides dynamic and static load specifications for the processor package. These mechanical load limits should not be exceeded during heatsink assembly, mechanical stress testing or standard drop and shipping conditions. The heatsink attach solutions must not include continuous stress onto the processor with the exception of a uniform load to maintain the heatsink-to-processor thermal interface. Also, any mechanical system or component testing should not exceed these limits. The processor package substrate should not be used as a mechanical reference or load-bearing surface for thermal or mechanical solutions.

Table 3-1. Package Loading Specifications

Parameter	Board Thickness	Min	Max	Unit	Notes
Static Compressive Load	1.57 mm 0.062”	80 18	311 70	N lbf	1,2,3,8
	2.16 mm 0.085”	111 25	311 70	N lbf	
	2.54 mm 0.100”	133 30	311 70	N lbf	
Dynamic Compressive Load	NA	NA	311 N (max static compressive load) + 222 N dynamic loading 70 lbf (max static compressive load) + 50 lbf dynamic loading	N lbf	1,3,4,5,6
Transient Bend Limits	1.57 mm 0.062”	NA	750	me	1,3,7

NOTES:

1. These specifications apply to uniform compressive loading in a direction perpendicular to the IHS top surface.
2. This is the minimum and maximum static force that can be applied by the heatsink and retention solution to maintain the heatsink and processor interface.
3. These specifications are based on limited testing for design characterization. Loading limits are for the LGA771 socket.
4. Dynamic compressive load applies to all board thickness.
5. Dynamic loading is defined as an 11 ms duration average load superimposed on the static load requirement.
6. Test condition used a heatsink mass of 1 lbm with 50 g acceleration measured at heatsink mass. The dynamic portion of this specification in the product application can have flexibility in specific values, but the ultimate product of mass times acceleration should not exceed this dynamic load.
7. Transient bend is defined as the transient board deflection during manufacturing such as board assembly and system integration. It is a relatively slow bending event compared to shock and vibration tests.
8. Refer to the for information on heatsink clip load metrology.

3.4 Package Handling Guidelines

Table 3-2 includes a list of guidelines on a package handling in terms of recommended maximum loading on the processor IHS relative to a fixed substrate. These package handling loads may be experienced during heatsink removal.

Table 3-2. Package Handling Guidelines

Parameter	Maximum Recommended	Units	Notes
Shear	311 70	N lbf	1,4,5
Tensile	111 25	N lbf	2,4,5
Torque	3.95 35	N-m LBF-in	3,4,5

NOTES:
1. A shear load is defined as a load applied to the IHS in a direction parallel to the IHS top surface.
2. A tensile load is defined as a pulling load applied to the IHS in a direction normal to the IHS surface.
3. A torque load is defined as a twisting load applied to the IHS in an axis of rotation normal to the IHS top surface.
4. These guidelines are based on limited testing for design characterization and incidental applications (one time only).
5. Handling guidelines are for the package only and do not include the limits of the processor socket.

3.5 Package Insertion Specifications

The processor can be inserted and removed 15 times from an LGA771 socket, which meets the criteria outlined in the *LGA771 Socket Design Guidelines*.

3.6 Processor Mass Specifications

The typical mass of the processor is 21.5 grams [0.76D oz.]. This includes all components which make up the entire processor product.

3.7 Processor Materials

The processor is assembled from several components. The basic material properties are described in Table 3-3.

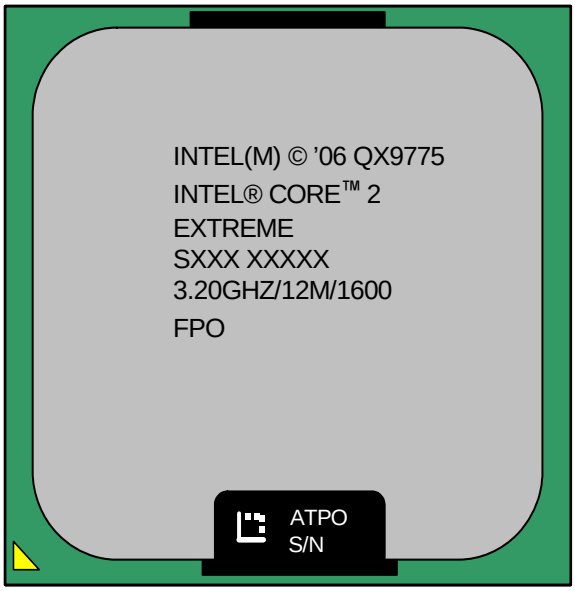
Table 3-3. Processor Materials

Component	Material
Integrated Heat Spreader (IHS)	Nickel over copper
Substrate	Fiber-reinforced resin
Substrate Lands	Gold over nickel

3.8 Processor Markings

Figure 3-5 shows the topside markings on the processor. This diagram aids in the identification of the processor.

Figure 3-5. Processor Top-side Markings (Example)



3.9 Processor Land Coordinates

Figure 3-6 and Figure 3-7 show the top and bottom view of the processor land coordinates, respectively. The coordinates are referred to throughout the document to identify processor lands.

Figure 3-6. Processor Land Coordinates, Top View

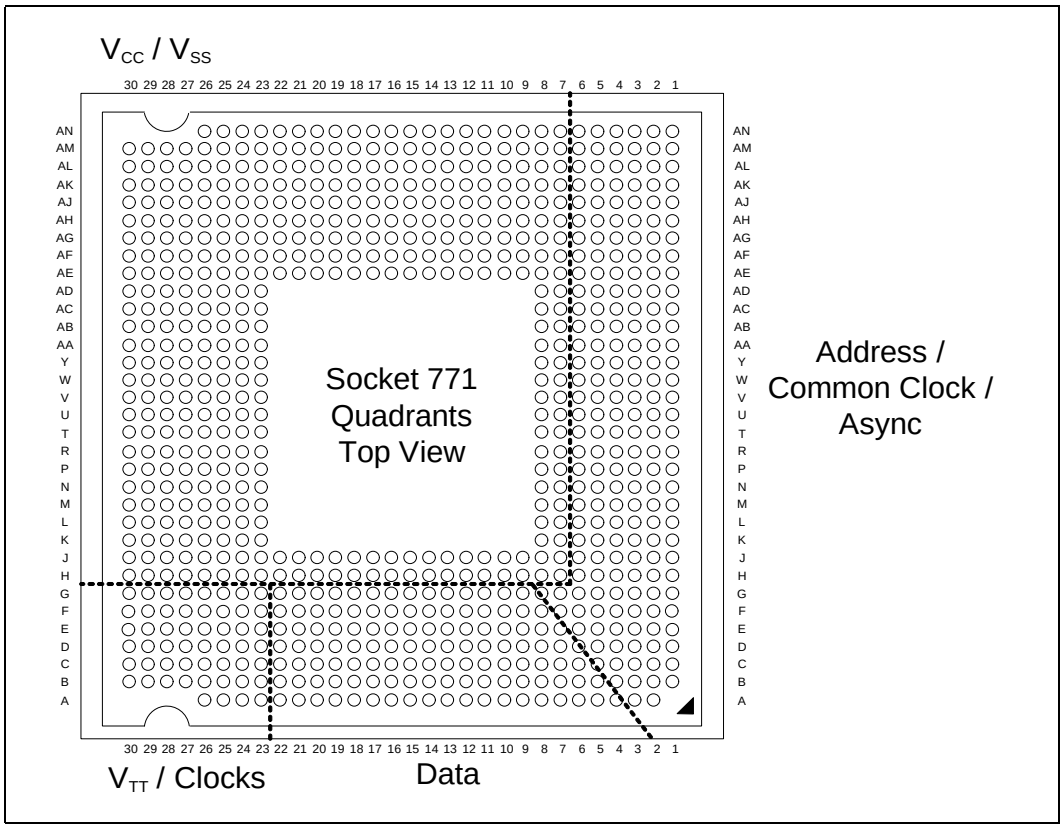
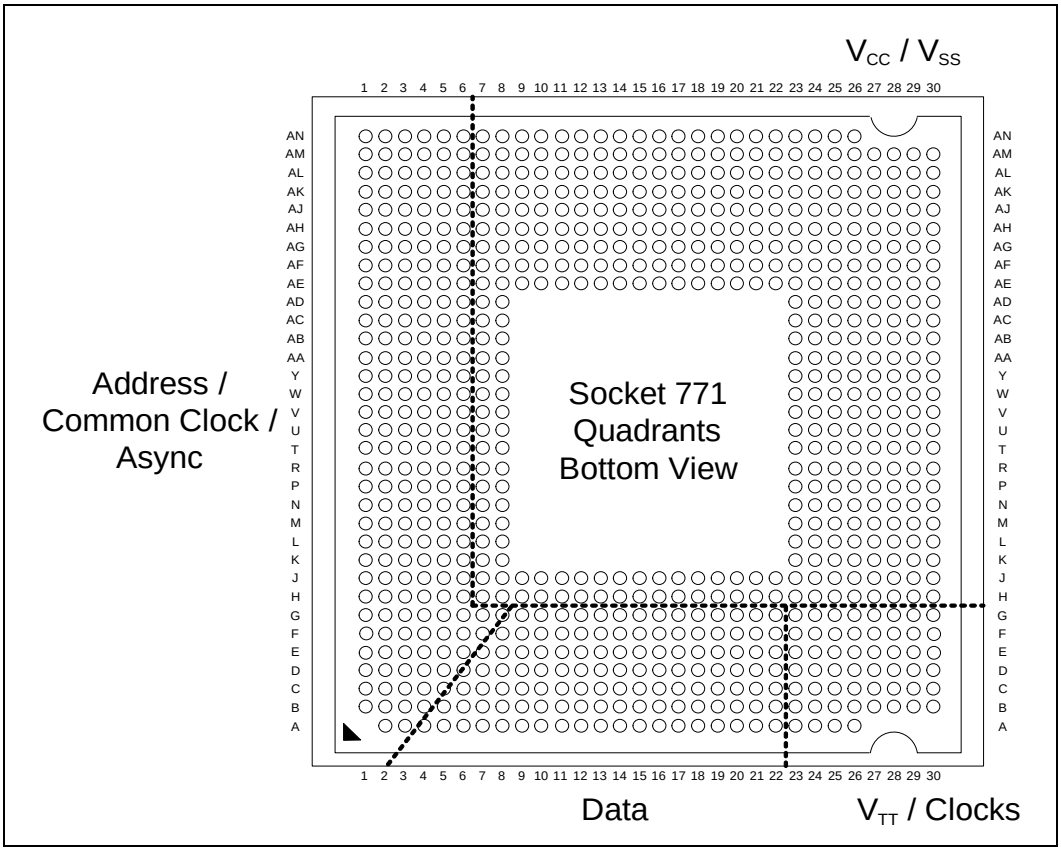


Figure 3-7. Processor Land Coordinates, Bottom View



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4 Land Listing and Signal Description

4.1 Land Listing

Table 4-1 is a listing of all processor lands ordered alphabetically by Land name. Table 4-2 is a listing of all processor lands ordered by land number.

Table 4-1. Land Listing by Land Name (Sheet 1 of 17)

Land Name	Land No.	Signal Buffer Type	Direction
A3#	M5	Source Sync	Input/Output
A4#	P6	Source Sync	Input/Output
A5#	L5	Source Sync	Input/Output
A6#	L4	Source Sync	Input/Output
A7#	M4	Source Sync	Input/Output
A8#	R4	Source Sync	Input/Output
A9#	T5	Source Sync	Input/Output
A10#	U6	Source Sync	Input/Output
A11#	T4	Source Sync	Input/Output
A12#	U5	Source Sync	Input/Output
A13#	U4	Source Sync	Input/Output
A14#	V5	Source Sync	Input/Output
A15#	V4	Source Sync	Input/Output
A16#	W5	Source Sync	Input/Output
A17#	AB6	Source Sync	Input/Output
A18#	W6	Source Sync	Input/Output
A19#	Y6	Source Sync	Input/Output
A20#	Y4	Source Sync	Input/Output
A20M#	K3	CMOS ASync	Input
A21#	AA4	Source Sync	Input/Output
A22#	AD6	Source Sync	Input/Output
A23#	AA5	Source Sync	Input/Output
A24#	AB5	Source Sync	Input/Output
A25#	AC5	Source Sync	Input/Output
A26#	AB4	Source Sync	Input/Output
A27#	AF5	Source Sync	Input/Output
A28#	AF4	Source Sync	Input/Output
A29#	AG6	Source Sync	Input/Output
A30#	AG4	Source Sync	Input/Output
A31#	AG5	Source Sync	Input/Output
A32#	AH4	Source Sync	Input/Output
A33#	AH5	Source Sync	Input/Output
A34#	AJ5	Source Sync	Input/Output
A35#	AJ6	Source Sync	Input/Output
A36#	N4	Source Sync	Input/Output
A37#	P5	Source Sync	Input/Output
ADS#	D2	Common Clk	Input/Output
ADSTB0#	R6	Source Sync	Input/Output
ADSTB1#	AD5	Source Sync	Input/Output
AP0#	U2	Common Clk	Input/Output
AP1#	U3	Common Clk	Input/Output
BCLK0	F28	Clk	Input
BCLK1	G28	Clk	Input
BINIT#	AD3	Common Clk	Input/Output
BNR#	C2	Common Clk	Input/Output
BPM0#	AJ2	Common Clk	Input/Output

Table 4-1. Land Listing by Land Name (Sheet 2 of 17)

Land Name	Land No.	Signal Buffer Type	Direction
BPM1#	AJ1	Common Clk	Output
BPM2#	AD2	Common Clk	Output
BPM3#	AG2	Common Clk	Input/Output
BPM4#	AF2	Common Clk	Output
BPM5#	AG3	Common Clk	Input/Output
BPMb0#	G1	Common Clk	Input/Output
BPMb1#	C9	Common Clk	Output
BPMb2#	G4	Common Clk	Output
BPMb3#	G3	Common Clk	Input/Output
BPRI#	G8	Common Clk	Input
BR0#	F3	Common Clk	Input/Output
BR1#	H5	Common Clk	Input
BSEL0	G29	CMOS ASync	Output
BSEL1	H30	CMOS ASync	Output
BSEL2	G30	CMOS Async	Output
COMP0	A13	Power/Other	Input
COMP1	T1	Power/Other	Input
COMP2	G2	Power/Other	Input
COMP3	R1	Power/Other	Input
D0#	B4	Source Sync	Input/Output
D1#	C5	Source Sync	Input/Output
D2#	A4	Source Sync	Input/Output
D3#	C6	Source Sync	Input/Output
D4#	A5	Source Sync	Input/Output
D5#	B6	Source Sync	Input/Output
D6#	B7	Source Sync	Input/Output
D7#	A7	Source Sync	Input/Output
D8#	A10	Source Sync	Input/Output
D9#	A11	Source Sync	Input/Output
D10#	B10	Source Sync	Input/Output
D11#	C11	Source Sync	Input/Output
D12#	D8	Source Sync	Input/Output
D13#	B12	Source Sync	Input/Output
D14#	C12	Source Sync	Input/Output
D15#	D11	Source Sync	Input/Output
D16#	G9	Source Sync	Input/Output
D17#	F8	Source Sync	Input/Output
D18#	F9	Source Sync	Input/Output
D19#	E9	Source Sync	Input/Output
D20#	D7	Source Sync	Input/Output
D21#	E10	Source Sync	Input/Output
D22#	D10	Source Sync	Input/Output
D23#	F11	Source Sync	Input/Output
D24#	F12	Source Sync	Input/Output
D25#	D13	Source Sync	Input/Output
D26#	E13	Source Sync	Input/Output

Table 4-1. Land Listing by Land Name (Sheet 3 of 17)

Land Name	Land No.	Signal Buffer Type	Direction
D27#	G13	Source Sync	Input/Output
D28#	F14	Source Sync	Input/Output
D29#	G14	Source Sync	Input/Output
D30#	F15	Source Sync	Input/Output
D31#	G15	Source Sync	Input/Output
D32#	G16	Source Sync	Input/Output
D33#	E15	Source Sync	Input/Output
D34#	E16	Source Sync	Input/Output
D35#	G18	Source Sync	Input/Output
D36#	G17	Source Sync	Input/Output
D37#	F17	Source Sync	Input/Output
D38#	F18	Source Sync	Input/Output
D39#	E18	Source Sync	Input/Output
D40#	E19	Source Sync	Input/Output
D41#	F20	Source Sync	Input/Output
D42#	E21	Source Sync	Input/Output
D43#	F21	Source Sync	Input/Output
D44#	G21	Source Sync	Input/Output
D45#	E22	Source Sync	Input/Output
D46#	D22	Source Sync	Input/Output
D47#	G22	Source Sync	Input/Output
D48#	D20	Source Sync	Input/Output
D49#	D17	Source Sync	Input/Output
D50#	A14	Source Sync	Input/Output
D51#	C15	Source Sync	Input/Output
D52#	C14	Source Sync	Input/Output
D53#	B15	Source Sync	Input/Output
D54#	C18	Source Sync	Input/Output
D55#	B16	Source Sync	Input/Output
D56#	A17	Source Sync	Input/Output
D57#	B18	Source Sync	Input/Output
D58#	C21	Source Sync	Input/Output
D59#	B21	Source Sync	Input/Output
D60#	B19	Source Sync	Input/Output
D61#	A19	Source Sync	Input/Output
D62#	A22	Source Sync	Input/Output
D63#	B22	Source Sync	Input/Output
DBI0#	A8	Source Sync	Input/Output
DBI1#	G11	Source Sync	Input/Output
DBI2#	D19	Source Sync	Input/Output
DBI3#	C20	Source Sync	Input/Output
DBR#	AC2	Power/Other	Output
DBSY#	B2	Common Clk	Input/Output
DEFER#	G7	Common Clk	Input
DP0#	J16	Common Clk	Input/Output
DP1#	H15	Common Clk	Input/Output

Table 4-1. Land Listing by Land Name (Sheet 4 of 17)

Land Name	Land No.	Signal Buffer Type	Direction
DP2#	H16	Common Clk	Input/Output
DP3#	J17	Common Clk	Input/Output
DRDY#	C1	Common Clk	Input/Output
DSTBN0#	C8	Source Sync	Input/Output
DSTBN1#	G12	Source Sync	Input/Output
DSTBN2#	G20	Source Sync	Input/Output
DSTBN3#	A16	Source Sync	Input/Output
DSTBP0#	B9	Source Sync	Input/Output
DSTBP1#	E12	Source Sync	Input/Output
DSTBP2#	G19	Source Sync	Input/Output
DSTBP3#	C17	Source Sync	Input/Output
FERR#/PBE#	R3	Open Drain	Output
FORCEPR#	AK6	CMOS ASync	Input
GTLREF_ADD_END	G10	Power/Other	Input
GTLREF_ADD_MID	F2	Power/Other	Input
GTLREF_DATA_END	H1	Power/Other	Input
GTLREF_DATA_MID	H2	Power/Other	Input
HIT#	D4	Common Clk	Input/Output
HITM#	E4	Common Clk	Input/Output
IERR#	AB2	Open Drain	Output
IGNNE#	N2	CMOS ASync	Input
INIT#	P3	CMOS ASync	Input
LINT0	K1	CMOS ASync	Input
LINT1	L1	CMOS ASync	Input
LL_ID0	V2	Power/Other	Output
LL_ID1	AA2	Power/Other	Output
LOCK#	C3	Common Clk	Input/Output
MCERR#	AB3	Common Clk	Input/Output
MS_ID0	W1	Power/Other	Output
MS_ID1	V1	Power/Other	Output
PECI	G5	Power/Other	Input/Output
PROCHOT#	AL2	Open Drain	Output
PWRGOOD	N1	CMOS ASync	Input
REQ0#	K4	Source Sync	Input/Output
REQ1#	J5	Source Sync	Input/Output
REQ2#	M6	Source Sync	Input/Output
REQ3#	K6	Source Sync	Input/Output
REQ4#	J6	Source Sync	Input/Output
RESERVED	AM6		
RESERVED	A20		
RESERVED	A23		
RESERVED	A24		
RESERVED	AC4		

Table 4-1. Land Listing by Land Name (Sheet 5 of 17)

Land Name	Land No.	Signal Buffer Type	Direction
RESERVED	AE4		
RESERVED	AE6		
RESERVED	AH2		
RESERVED	AH7		
RESERVED	AJ3		
RESERVED	AJ7		
RESERVED	AK3		
RESERVED	AM2		
RESERVED	AN5		
RESERVED	AN6		
RESERVED	B13		
RESERVED	B23		
RESERVED	C23		
RESERVED	D1		
RESERVED	D14		
RESERVED	D16		
RESERVED	E1		
RESERVED	E23		
RESERVED	E24		
RESERVED	E5		
RESERVED	E6		
RESERVED	E7		
RESERVED	E29		
RESERVED	F23		
RESERVED	F29		
RESERVED	F6		
RESERVED	G6		
RESERVED	J2		
RESERVED	J3		
RESERVED	N5		
RESERVED	T2		
RESERVED	Y1		
RESERVED	Y3		
RESERVED	AL1		
RESERVED	AK1		
RESERVED	G27		
RESERVED	G26		
RESERVED	G24		
RESERVED	F24		
RESERVED	F26		
RESERVED	F25		
RESERVED	G25		
RESERVED	W3		
RESET#	G23	Common Clk	Input
RS0#	B3	Common Clk	Input
RS1#	F5	Common Clk	Input

Table 4-1. Land Listing by Land Name (Sheet 6 of 17)

Land Name	Land No.	Signal Buffer Type	Direction
RS2#	A3	Common Clk	Input
RSP#	H4	Common Clk	Input
SKTOCC#	AE8	Power/Other	Output
SMI#	P2	CMOS ASync	Input
STPCLK#	M3	CMOS ASync	Input
TCK	AE1	TAP	Input
TDI	AD1	TAP	Input
TDO	AF1	TAP	Output
TESTHI10	P1	Power/Other	Input
TESTHI11	L2	Power/Other	Input
TESTHI12	AE3	Power/Other	Input
TESTIN1	W2	Power/Other	Input
TESTIN2	U1	Power/Other	Input
THERMTRIP#	M2	Open Drain	Output
TMS	AC1	TAP	Input
TRDY#	E3	Common Clk	Input
TRST#	AG1	TAP	Input
VCC	AA8	Power/Other	
VCC	AB8	Power/Other	
VCC	AC23	Power/Other	
VCC	AC24	Power/Other	
VCC	AC25	Power/Other	
VCC	AC26	Power/Other	
VCC	AC27	Power/Other	
VCC	AC28	Power/Other	
VCC	AC29	Power/Other	
VCC	AC30	Power/Other	
VCC	AC8	Power/Other	
VCC	AD23	Power/Other	
VCC	AD24	Power/Other	
VCC	AD25	Power/Other	
VCC	AD26	Power/Other	
VCC	AD27	Power/Other	
VCC	AD28	Power/Other	
VCC	AD29	Power/Other	
VCC	AD30	Power/Other	
VCC	AD8	Power/Other	
VCC	AE11	Power/Other	
VCC	AE12	Power/Other	
VCC	AE14	Power/Other	
VCC	AE15	Power/Other	
VCC	AE18	Power/Other	
VCC	AE19	Power/Other	
VCC	AE21	Power/Other	
VCC	AE22	Power/Other	
VCC	AE23	Power/Other	

Table 4-1. Land Listing by Land Name (Sheet 7 of 17)

Land Name	Land No.	Signal Buffer Type	Direction
VCC	AE9	Power/Other	
VCC	AF11	Power/Other	
VCC	AF12	Power/Other	
VCC	AF14	Power/Other	
VCC	AF15	Power/Other	
VCC	AF18	Power/Other	
VCC	AF19	Power/Other	
VCC	AF21	Power/Other	
VCC	AF22	Power/Other	
VCC	AF8	Power/Other	
VCC	AF9	Power/Other	
VCC	AG11	Power/Other	
VCC	AG12	Power/Other	
VCC	AG14	Power/Other	
VCC	AG15	Power/Other	
VCC	AG18	Power/Other	
VCC	AG19	Power/Other	
VCC	AG21	Power/Other	
VCC	AG22	Power/Other	
VCC	AG25	Power/Other	
VCC	AG26	Power/Other	
VCC	AG27	Power/Other	
VCC	AG28	Power/Other	
VCC	AG29	Power/Other	
VCC	AG30	Power/Other	
VCC	AG8	Power/Other	
VCC	AG9	Power/Other	
VCC	AH11	Power/Other	
VCC	AH12	Power/Other	
VCC	AH14	Power/Other	
VCC	AH15	Power/Other	
VCC	AH18	Power/Other	
VCC	AH19	Power/Other	
VCC	AH21	Power/Other	
VCC	AH22	Power/Other	
VCC	AH25	Power/Other	
VCC	AH26	Power/Other	
VCC	AH27	Power/Other	
VCC	AH28	Power/Other	
VCC	AH29	Power/Other	
VCC	AH30	Power/Other	
VCC	AH8	Power/Other	
VCC	AH9	Power/Other	
VCC	AJ11	Power/Other	
VCC	AJ12	Power/Other	
VCC	AJ14	Power/Other	

Table 4-1. Land Listing by Land Name (Sheet 8 of 17)

Land Name	Land No.	Signal Buffer Type	Direction
VCC	AJ15	Power/Other	
VCC	AJ18	Power/Other	
VCC	AJ19	Power/Other	
VCC	AJ21	Power/Other	
VCC	AJ22	Power/Other	
VCC	AJ25	Power/Other	
VCC	AJ26	Power/Other	
VCC	AJ8	Power/Other	
VCC	AJ9	Power/Other	
VCC	AK11	Power/Other	
VCC	AK12	Power/Other	
VCC	AK14	Power/Other	
VCC	AK15	Power/Other	
VCC	AK18	Power/Other	
VCC	AK19	Power/Other	
VCC	AK21	Power/Other	
VCC	AK22	Power/Other	
VCC	AK25	Power/Other	
VCC	AK26	Power/Other	
VCC	AK8	Power/Other	
VCC	AK9	Power/Other	
VCC	AL11	Power/Other	
VCC	AL12	Power/Other	
VCC	AL14	Power/Other	
VCC	AL15	Power/Other	
VCC	AL18	Power/Other	
VCC	AL19	Power/Other	
VCC	AL21	Power/Other	
VCC	AL22	Power/Other	
VCC	AL25	Power/Other	
VCC	AL26	Power/Other	
VCC	AL29	Power/Other	
VCC	AL30	Power/Other	
VCC	AL9	Power/Other	
VCC	AM11	Power/Other	
VCC	AM12	Power/Other	
VCC	AM14	Power/Other	
VCC	AM15	Power/Other	
VCC	AM18	Power/Other	
VCC	AM19	Power/Other	
VCC	AM21	Power/Other	
VCC	AM22	Power/Other	
VCC	AM25	Power/Other	
VCC	AM26	Power/Other	
VCC	AM29	Power/Other	
VCC	AM30	Power/Other	

Table 4-1. Land Listing by Land Name (Sheet 9 of 17)

Land Name	Land No.	Signal Buffer Type	Direction
VCC	AM8	Power/Other	
VCC	AM9	Power/Other	
VCC	AN11	Power/Other	
VCC	AN12	Power/Other	
VCC	AN14	Power/Other	
VCC	AN15	Power/Other	
VCC	AN18	Power/Other	
VCC	AN19	Power/Other	
VCC	AN21	Power/Other	
VCC	AN22	Power/Other	
VCC	AN25	Power/Other	
VCC	AN26	Power/Other	
VCC	AN8	Power/Other	
VCC	AN9	Power/Other	
VCC	J10	Power/Other	
VCC	J11	Power/Other	
VCC	J12	Power/Other	
VCC	J13	Power/Other	
VCC	J14	Power/Other	
VCC	J15	Power/Other	
VCC	J18	Power/Other	
VCC	J19	Power/Other	
VCC	J20	Power/Other	
VCC	J21	Power/Other	
VCC	J22	Power/Other	
VCC	J23	Power/Other	
VCC	J24	Power/Other	
VCC	J25	Power/Other	
VCC	J26	Power/Other	
VCC	J27	Power/Other	
VCC	J28	Power/Other	
VCC	J29	Power/Other	
VCC	J30	Power/Other	
VCC	J8	Power/Other	
VCC	J9	Power/Other	
VCC	K23	Power/Other	
VCC	K24	Power/Other	
VCC	K25	Power/Other	
VCC	K26	Power/Other	
VCC	K27	Power/Other	
VCC	K28	Power/Other	
VCC	K29	Power/Other	
VCC	K30	Power/Other	
VCC	K8	Power/Other	
VCC	L8	Power/Other	
VCC	M23	Power/Other	

Table 4-1. Land Listing by Land Name (Sheet 10 of 17)

Land Name	Land No.	Signal Buffer Type	Direction
VCC	M24	Power/Other	
VCC	M25	Power/Other	
VCC	M26	Power/Other	
VCC	M27	Power/Other	
VCC	M28	Power/Other	
VCC	M29	Power/Other	
VCC	M30	Power/Other	
VCC	M8	Power/Other	
VCC	N23	Power/Other	
VCC	N24	Power/Other	
VCC	N25	Power/Other	
VCC	N26	Power/Other	
VCC	N27	Power/Other	
VCC	N28	Power/Other	
VCC	N29	Power/Other	
VCC	N30	Power/Other	
VCC	N8	Power/Other	
VCC	P8	Power/Other	
VCC	R8	Power/Other	
VCC	T23	Power/Other	
VCC	T24	Power/Other	
VCC	T25	Power/Other	
VCC	T26	Power/Other	
VCC	T27	Power/Other	
VCC	T28	Power/Other	
VCC	T29	Power/Other	
VCC	T30	Power/Other	
VCC	T8	Power/Other	
VCC	U23	Power/Other	
VCC	U24	Power/Other	
VCC	U25	Power/Other	
VCC	U26	Power/Other	
VCC	U27	Power/Other	
VCC	U28	Power/Other	
VCC	U29	Power/Other	
VCC	U30	Power/Other	
VCC	U8	Power/Other	
VCC	V8	Power/Other	
VCC	W23	Power/Other	
VCC	W24	Power/Other	
VCC	W25	Power/Other	
VCC	W26	Power/Other	
VCC	W27	Power/Other	
VCC	W28	Power/Other	
VCC	W29	Power/Other	
VCC	W30	Power/Other	

Table 4-1. Land Listing by Land Name (Sheet 11 of 17)

Land Name	Land No.	Signal Buffer Type	Direction
VCC	W8	Power/Other	
VCC	Y23	Power/Other	
VCC	Y24	Power/Other	
VCC	Y25	Power/Other	
VCC	Y26	Power/Other	
VCC	Y27	Power/Other	
VCC	Y28	Power/Other	
VCC	Y29	Power/Other	
VCC	Y30	Power/Other	
VCC	Y8	Power/Other	
VCC_DIE_SENSE	AN3	Power/Other	Output
VCC_DIE_SENSE2	AL8	Power/Other	Output
VCCPLL	D23	Power/Other	Input
VID_SELECT	AN7	Power/Other	Output
VID1	AL5	CMOS Async	Output
VID2	AM3	CMOS Async	Output
VID3	AL6	CMOS Async	Output
VID4	AK4	CMOS Async	Output
VID5	AL4	CMOS Async	Output
VID6	AM5	CMOS Async	Output
VSS	A12	Power/Other	
VSS	A15	Power/Other	
VSS	A18	Power/Other	
VSS	A2	Power/Other	
VSS	A21	Power/Other	
VSS	A6	Power/Other	
VSS	A9	Power/Other	
VSS	AA23	Power/Other	
VSS	AA24	Power/Other	
VSS	AA25	Power/Other	
VSS	AA26	Power/Other	
VSS	AA27	Power/Other	
VSS	AA28	Power/Other	
VSS	AA29	Power/Other	
VSS	AA3	Power/Other	
VSS	AA30	Power/Other	
VSS	AA6	Power/Other	
VSS	AA7	Power/Other	
VSS	AB1	Power/Other	
VSS	AB23	Power/Other	
VSS	AB24	Power/Other	
VSS	AB25	Power/Other	
VSS	AB26	Power/Other	
VSS	AB27	Power/Other	
VSS	AB28	Power/Other	

Table 4-1. Land Listing by Land Name (Sheet 12 of 17)

Land Name	Land No.	Signal Buffer Type	Direction
VSS	AB29	Power/Other	
VSS	AB30	Power/Other	
VSS	AB7	Power/Other	
VSS	AC3	Power/Other	
VSS	AC6	Power/Other	
VSS	AC7	Power/Other	
VSS	AD4	Power/Other	
VSS	AD7	Power/Other	
VSS	AE10	Power/Other	
VSS	AE13	Power/Other	
VSS	AE16	Power/Other	
VSS	AE17	Power/Other	
VSS	AE2	Power/Other	
VSS	AE20	Power/Other	
VSS	AE24	Power/Other	
VSS	AE25	Power/Other	
VSS	AE26	Power/Other	
VSS	AE27	Power/Other	
VSS	AE28	Power/Other	
VSS	AE29	Power/Other	
VSS	AE30	Power/Other	
VSS	AE5	Power/Other	
VSS	AE7	Power/Other	
VSS	AF7	Power/Other	
VSS	AF10	Power/Other	
VSS	AF13	Power/Other	
VSS	AF16	Power/Other	
VSS	AF17	Power/Other	
VSS	AF20	Power/Other	
VSS	AF23	Power/Other	
VSS	AF24	Power/Other	
VSS	AF25	Power/Other	
VSS	AF26	Power/Other	
VSS	AF27	Power/Other	
VSS	AF28	Power/Other	
VSS	AF29	Power/Other	
VSS	AF3	Power/Other	
VSS	AF30	Power/Other	
VSS	AF6	Power/Other	
VSS	AG10	Power/Other	
VSS	AG13	Power/Other	
VSS	AG16	Power/Other	
VSS	AG17	Power/Other	
VSS	AG20	Power/Other	
VSS	AG23	Power/Other	
VSS	AG24	Power/Other	

Table 4-1. Land Listing by Land Name (Sheet 13 of 17)

Land Name	Land No.	Signal Buffer Type	Direction
VSS	AG7	Power/Other	
VSS	AH1	Power/Other	
VSS	AH10	Power/Other	
VSS	AH13	Power/Other	
VSS	AH16	Power/Other	
VSS	AH17	Power/Other	
VSS	AH20	Power/Other	
VSS	AH23	Power/Other	
VSS	AH24	Power/Other	
VSS	AH3	Power/Other	
VSS	AH6	Power/Other	
VSS	AJ10	Power/Other	
VSS	AJ13	Power/Other	
VSS	AJ16	Power/Other	
VSS	AJ17	Power/Other	
VSS	AJ20	Power/Other	
VSS	AJ23	Power/Other	
VSS	AJ24	Power/Other	
VSS	AJ27	Power/Other	
VSS	AJ28	Power/Other	
VSS	AJ29	Power/Other	
VSS	AJ30	Power/Other	
VSS	AJ4	Power/Other	
VSS	AK10	Power/Other	
VSS	AK13	Power/Other	
VSS	AK16	Power/Other	
VSS	AK17	Power/Other	
VSS	AK2	Power/Other	
VSS	AK20	Power/Other	
VSS	AK23	Power/Other	
VSS	AK24	Power/Other	
VSS	AK27	Power/Other	
VSS	AK28	Power/Other	
VSS	AK29	Power/Other	
VSS	AK30	Power/Other	
VSS	AK5	Power/Other	
VSS	AK7	Power/Other	
VSS	AL10	Power/Other	
VSS	AL13	Power/Other	
VSS	AL16	Power/Other	
VSS	AL17	Power/Other	
VSS	AL20	Power/Other	
VSS	AL23	Power/Other	
VSS	AL24	Power/Other	
VSS	AL27	Power/Other	
VSS	AL28	Power/Other	

Table 4-1. Land Listing by Land Name (Sheet 14 of 17)

Land Name	Land No.	Signal Buffer Type	Direction
VSS	AL3	Power/Other	
VSS	AM1	Power/Other	
VSS	AM10	Power/Other	
VSS	AM13	Power/Other	
VSS	AM16	Power/Other	
VSS	AM17	Power/Other	
VSS	AM20	Power/Other	
VSS	AM23	Power/Other	
VSS	AM24	Power/Other	
VSS	AM27	Power/Other	
VSS	AM28	Power/Other	
VSS	AM4	Power/Other	
VSS	AM7	Power/Other	
VSS	AN1	Power/Other	
VSS	AN10	Power/Other	
VSS	AN13	Power/Other	
VSS	AN16	Power/Other	
VSS	AN17	Power/Other	
VSS	AN2	Power/Other	
VSS	AN20	Power/Other	
VSS	AN23	Power/Other	
VSS	AN24	Power/Other	
VSS	B1	Power/Other	
VSS	B11	Power/Other	
VSS	B14	Power/Other	
VSS	B17	Power/Other	
VSS	B20	Power/Other	
VSS	B24	Power/Other	
VSS	B5	Power/Other	
VSS	B8	Power/Other	
VSS	C10	Power/Other	
VSS	C13	Power/Other	
VSS	C16	Power/Other	
VSS	C19	Power/Other	
VSS	C22	Power/Other	
VSS	C24	Power/Other	
VSS	C4	Power/Other	
VSS	C7	Power/Other	
VSS	D12	Power/Other	
VSS	D15	Power/Other	
VSS	D18	Power/Other	
VSS	D21	Power/Other	
VSS	D24	Power/Other	
VSS	D3	Power/Other	
VSS	D5	Power/Other	
VSS	D6	Power/Other	

Table 4-1. Land Listing by Land Name (Sheet 15 of 17)

Land Name	Land No.	Signal Buffer Type	Direction
VSS	D9	Power/Other	
VSS	E11	Power/Other	
VSS	E14	Power/Other	
VSS	E17	Power/Other	
VSS	E2	Power/Other	
VSS	E20	Power/Other	
VSS	E25	Power/Other	
VSS	E26	Power/Other	
VSS	E27	Power/Other	
VSS	E28	Power/Other	
VSS	E8	Power/Other	
VSS	F1	Power/Other	
VSS	F10	Power/Other	
VSS	F13	Power/Other	
VSS	F16	Power/Other	
VSS	F19	Power/Other	
VSS	F22	Power/Other	
VSS	F4	Power/Other	
VSS	F7	Power/Other	
VSS	H10	Power/Other	
VSS	H11	Power/Other	
VSS	H12	Power/Other	
VSS	H13	Power/Other	
VSS	H14	Power/Other	
VSS	H17	Power/Other	
VSS	H18	Power/Other	
VSS	H19	Power/Other	
VSS	H20	Power/Other	
VSS	H21	Power/Other	
VSS	H22	Power/Other	
VSS	H23	Power/Other	
VSS	H24	Power/Other	
VSS	H25	Power/Other	
VSS	H26	Power/Other	
VSS	H27	Power/Other	
VSS	H28	Power/Other	
VSS	H29	Power/Other	
VSS	H3	Power/Other	
VSS	H6	Power/Other	
VSS	H7	Power/Other	
VSS	H8	Power/Other	
VSS	H9	Power/Other	
VSS	J4	Power/Other	
VSS	J7	Power/Other	
VSS	K2	Power/Other	
VSS	K5	Power/Other	

Table 4-1. Land Listing by Land Name (Sheet 16 of 17)

Land Name	Land No.	Signal Buffer Type	Direction
VSS	K7	Power/Other	
VSS	L23	Power/Other	
VSS	L24	Power/Other	
VSS	L25	Power/Other	
VSS	L26	Power/Other	
VSS	L27	Power/Other	
VSS	L28	Power/Other	
VSS	L29	Power/Other	
VSS	L3	Power/Other	
VSS	L30	Power/Other	
VSS	L6	Power/Other	
VSS	L7	Power/Other	
VSS	M1	Power/Other	
VSS	M7	Power/Other	
VSS	N3	Power/Other	
VSS	N6	Power/Other	
VSS	N7	Power/Other	
VSS	P23	Power/Other	
VSS	P24	Power/Other	
VSS	P25	Power/Other	
VSS	P26	Power/Other	
VSS	P27	Power/Other	
VSS	P28	Power/Other	
VSS	P29	Power/Other	
VSS	P30	Power/Other	
VSS	P4	Power/Other	
VSS	P7	Power/Other	
VSS	R2	Power/Other	
VSS	R23	Power/Other	
VSS	R24	Power/Other	
VSS	R25	Power/Other	
VSS	R26	Power/Other	
VSS	R27	Power/Other	
VSS	R28	Power/Other	
VSS	R29	Power/Other	
VSS	R30	Power/Other	
VSS	R5	Power/Other	
VSS	R7	Power/Other	
VSS	T3	Power/Other	
VSS	T6	Power/Other	
VSS	T7	Power/Other	
VSS	U7	Power/Other	
VSS	V23	Power/Other	
VSS	V24	Power/Other	
VSS	V25	Power/Other	
VSS	V26	Power/Other	

Table 4-1. Land Listing by Land Name (Sheet 17 of 17)

Land Name	Land No.	Signal Buffer Type	Direction
VSS	V27	Power/Other	
VSS	V28	Power/Other	
VSS	V29	Power/Other	
VSS	V3	Power/Other	
VSS	V30	Power/Other	
VSS	V6	Power/Other	
VSS	V7	Power/Other	
VSS	W4	Power/Other	
VSS	W7	Power/Other	
VSS	Y2	Power/Other	
VSS	Y5	Power/Other	
VSS	Y7	Power/Other	
VSS_DIE_SENSE	AN4	Power/Other	Output
VSS_DIE_SENSE2	AL7	Power/Other	Output
VTT	A25	Power/Other	
VTT	A26	Power/Other	
VTT	B25	Power/Other	
VTT	B26	Power/Other	
VTT	B27	Power/Other	
VTT	B28	Power/Other	
VTT	B29	Power/Other	
VTT	B30	Power/Other	
VTT	C25	Power/Other	
VTT	C26	Power/Other	
VTT	C27	Power/Other	
VTT	C28	Power/Other	
VTT	C29	Power/Other	
VTT	C30	Power/Other	
VTT	D25	Power/Other	
VTT	D26	Power/Other	
VTT	D27	Power/Other	
VTT	D28	Power/Other	
VTT	D29	Power/Other	
VTT	D30	Power/Other	
VTT	E30	Power/Other	
VTT	F30	Power/Other	
VTT_OUT	AA1	Power/Other	Output
VTT_OUT	J1	Power/Other	Output
VTT_SEL	F27	Power/Other	Output

Table 4-2. Land Listing by Land Number (Sheet 1 of 17)

Pin No.	Pin Name	Signal Buffer Type	Direction
A2	VSS	Power/Other	
A3	RS2#	Common Clk	Input
A4	D02#	Source Sync	Input/Output
A5	D04#	Source Sync	Input/Output
A6	VSS	Power/Other	
A7	D07#	Source Sync	Input/Output
A8	DBI0#	Source Sync	Input/Output
A9	VSS	Power/Other	
A10	D08#	Source Sync	Input/Output
A11	D09#	Source Sync	Input/Output
A12	VSS	Power/Other	
A13	COMP0	Power/Other	Input
A14	D50#	Source Sync	Input/Output
A15	VSS	Power/Other	
A16	DSTBN3#	Source Sync	Input/Output
A17	D56#	Source Sync	Input/Output
A18	VSS	Power/Other	
A19	D61#	Source Sync	Input/Output
A20	RESERVED		
A21	VSS	Power/Other	
A22	D62#	Source Sync	Input/Output
A23	RESERVED		
A24	RESERVED		
A25	VTT	Power/Other	
A26	VTT	Power/Other	
B1	VSS	Power/Other	
B2	DBSY#	Common Clk	Input/Output
B3	RS0#	Common Clk	Input
B4	D00#	Source Sync	Input/Output
B5	VSS	Power/Other	
B6	D05#	Source Sync	Input/Output
B7	D06#	Source Sync	Input/Output
B8	VSS	Power/Other	
B9	DSTBP0#	Source Sync	Input/Output
B10	D10#	Source Sync	Input/Output
B11	VSS	Power/Other	
B12	D13#	Source Sync	Input/Output
B13	RESERVED		
B14	VSS	Power/Other	
B15	D53#	Source Sync	Input/Output
B16	D55#	Source Sync	Input/Output
B17	VSS	Power/Other	
B18	D57#	Source Sync	Input/Output
B19	D60#	Source Sync	Input/Output
B20	VSS	Power/Other	
B21	D59#	Source Sync	Input/Output

Table 4-2. Land Listing by Land Number (Sheet 2 of 17)

Pin No.	Pin Name	Signal Buffer Type	Direction
B22	D63#	Source Sync	Input/Output
B23	RESERVED		
B24	VSS	Power/Other	
B25	VTT	Power/Other	
B26	VTT	Power/Other	
B27	VTT	Power/Other	
B28	VTT	Power/Other	
B29	VTT	Power/Other	
B30	VTT	Power/Other	
C1	DRDY#	Common Clk	Input/Output
C2	BNR#	Common Clk	Input/Output
C3	LOCK#	Common Clk	Input/Output
C4	VSS	Power/Other	
C5	D01#	Source Sync	Input/Output
C6	D03#	Source Sync	Input/Output
C7	VSS	Power/Other	
C8	DSTBN0#	Source Sync	Input/Output
C9	BPMb1	Common Clk	Output
C10	VSS	Power/Other	
C11	D11#	Source Sync	Input/Output
C12	D14#	Source Sync	Input/Output
C13	VSS	Power/Other	
C14	D52#	Source Sync	Input/Output
C15	D51#	Source Sync	Input/Output
C16	VSS	Power/Other	
C17	DSTBP3#	Source Sync	Input/Output
C18	D54#	Source Sync	Input/Output
C19	VSS	Power/Other	
C20	DBI3#	Source Sync	Input/Output
C21	D58#	Source Sync	Input/Output
C22	VSS	Power/Other	
C23	RESERVED		
C24	VSS	Power/Other	
C25	VTT	Power/Other	
C26	VTT	Power/Other	
C27	VTT	Power/Other	
C28	VTT	Power/Other	
C29	VTT	Power/Other	
C30	VTT	Power/Other	
D1	RESERVED		
D2	ADS#	Common Clk	Input/Output
D3	VSS	Power/Other	
D4	HIT#	Common Clk	Input/Output
D5	VSS	Power/Other	
D6	VSS	Power/Other	
D7	D20#	Source Sync	Input/Output

Table 4-2. Land Listing by Land Number (Sheet 3 of 17)

Pin No.	Pin Name	Signal Buffer Type	Direction
D8	D12#	Source Sync	Input/Output
D9	VSS	Power/Other	
D10	D22#	Source Sync	Input/Output
D11	D15#	Source Sync	Input/Output
D12	VSS	Power/Other	
D13	D25#	Source Sync	Input/Output
D14	RESERVED		
D15	VSS	Power/Other	
D16	RESERVED		
D17	D49#	Source Sync	Input/Output
D18	VSS	Power/Other	
D19	DBI2#	Source Sync	Input/Output
D20	D48#	Source Sync	Input/Output
D21	VSS	Power/Other	
D22	D46#	Source Sync	Input/Output
D23	VCCPLL	Power/Other	Input
D24	VSS	Power/Other	
D25	VTT	Power/Other	
D26	VTT	Power/Other	
D27	VTT	Power/Other	
D28	VTT	Power/Other	
D29	VTT	Power/Other	
D30	VTT	Power/Other	
E1	RESERVED	Power/Other	
E2	VSS	Power/Other	
E3	TRDY#	Common Clk	Input
E4	HITM#	Common Clk	Input/Output
E5	RESERVED		
E6	RESERVED		
E7	RESERVED		
E8	VSS	Power/Other	
E9	D19#	Source Sync	Input/Output
E10	D21#	Source Sync	Input/Output
E11	VSS	Power/Other	
E12	DSTBP1#	Source Sync	Input/Output
E13	D26#	Source Sync	Input/Output
E14	VSS	Power/Other	
E15	D33#	Source Sync	Input/Output
E16	D34#	Source Sync	Input/Output
E17	VSS	Power/Other	
E18	D39#	Source Sync	Input/Output
E19	D40#	Source Sync	Input/Output
E20	VSS	Power/Other	
E21	D42#	Source Sync	Input/Output
E22	D45#	Source Sync	Input/Output
E23	RESERVED		

Table 4-2. Land Listing by Land Number (Sheet 4 of 17)

Pin No.	Pin Name	Signal Buffer Type	Direction
E24	RESERVED		
E25	VSS	Power/Other	
E26	VSS	Power/Other	
E27	VSS	Power/Other	
E28	VSS	Power/Other	
E29	RESERVED		
E30	VTT	Power/Other	
F1	VSS	Power/Other	
F2	GTLREF_ADD_MID	Power/Other	Input
F4	VSS	Power/Other	
F5	RS1#	Common Clk	Input
F6	RESERVED		
F7	VSS	Power/Other	
F8	D17#	Source Sync	Input/Output
F9	D18#	Source Sync	Input/Output
F10	VSS	Power/Other	
F11	D23#	Source Sync	Input/Output
F12	D24#	Source Sync	Input/Output
F13	VSS	Power/Other	
F14	D28#	Source Sync	Input/Output
F15	D30#	Source Sync	Input/Output
F16	VSS	Power/Other	
F17	D37#	Source Sync	Input/Output
F18	D38#	Source Sync	Input/Output
F19	VSS	Power/Other	
F20	D41#	Source Sync	Input/Output
F21	D43#	Source Sync	Input/Output
F22	VSS	Power/Other	
F23	RESERVED		
F24	RESERVED		
F25	RESERVED		
F26	RESERVED		
F27	VTT_SEL	Power/Other	Output
F28	BCLK0	Clk	Input
F29	RESERVED		
F3	BR0#	Common Clk	Input/Output
F30	VTT	Power/Other	
G1	BPMb0#	Common Clk	Input/Output
G2	COMP2	Power/Other	Input
G3	BPMb3#	Common Clk	Input/Output
G4	BPMb2#	Common Clk	Output
G5	PECI	Power/Other	Input/Output
G6	RESERVED		
G7	DEFER#	Common Clk	Input
G8	BPRI#	Common Clk	Input

Table 4-2. Land Listing by Land Number (Sheet 5 of 17)

Pin No.	Pin Name	Signal Buffer Type	Direction
G9	D16#	Source Sync	Input/Output
G10	GTLREF_ADD_END	Power/Other	Input
G11	DBI1#	Source Sync	Input/Output
G12	DSTBN1#	Source Sync	Input/Output
G13	D27#	Source Sync	Input/Output
G14	D29#	Source Sync	Input/Output
G15	D31#	Source Sync	Input/Output
G16	D32#	Source Sync	Input/Output
G17	D36#	Source Sync	Input/Output
G18	D35#	Source Sync	Input/Output
G19	DSTBP2#	Source Sync	Input/Output
G20	DSTBN2#	Source Sync	Input/Output
G21	D44#	Source Sync	Input/Output
G22	D47#	Source Sync	Input/Output
G23	RESET#	Common Clk	Input
G24	RESERVED		
G25	RESERVED		
G26	RESERVED		
G27	RESERVED		
G28	BCLK1	Clk	Input
G29	BSEL0	CMOS Async	Output
G30	BSEL2	CMOS Async	Output
H1	GTLREF_DATA_END	Power/Other	Input
H2	GTLREF_DATA_MID	Power/Other	Input
H3	VSS	Power/Other	
H4	RSP#	Common Clk	Input
H5	BR1#	Common Clk	Input
H6	VSS	Power/Other	
H7	VSS	Power/Other	
H8	VSS	Power/Other	
H9	VSS	Power/Other	
H10	VSS	Power/Other	
H11	VSS	Power/Other	
H12	VSS	Power/Other	
H13	VSS	Power/Other	
H14	VSS	Power/Other	
H15	DP1#	Common Clk	Input/Output
H16	DP2#	Common Clk	Input/Output
H17	VSS	Power/Other	
H18	VSS	Power/Other	
H19	VSS	Power/Other	
H20	VSS	Power/Other	
H21	VSS	Power/Other	
H22	VSS	Power/Other	

Table 4-2. Land Listing by Land Number (Sheet 6 of 17)

Pin No.	Pin Name	Signal Buffer Type	Direction
H23	VSS	Power/Other	
H24	VSS	Power/Other	
H25	VSS	Power/Other	
H26	VSS	Power/Other	
H27	VSS	Power/Other	
H28	VSS	Power/Other	
H29	VSS	Power/Other	
H30	BSEL1	CMOS Async	Output
J1	VTT_OUT	Power/Other	Output
J2	RESERVED		
J3	RESERVED		
J4	VSS	Power/Other	
J5	REQ1#	Source Sync	Input/Output
J6	REQ4#	Source Sync	Input/Output
J7	VSS	Power/Other	
J8	VCC	Power/Other	
J9	VCC	Power/Other	
J10	VCC	Power/Other	
J11	VCC	Power/Other	
J12	VCC	Power/Other	
J13	VCC	Power/Other	
J14	VCC	Power/Other	
J15	VCC	Power/Other	
J16	DP0#	Common Clk	Input/Output
J17	DP3#	Common Clk	Input/Output
J18	VCC	Power/Other	
J19	VCC	Power/Other	
J20	VCC	Power/Other	
J21	VCC	Power/Other	
J22	VCC	Power/Other	
J23	VCC	Power/Other	
J24	VCC	Power/Other	
J25	VCC	Power/Other	
J26	VCC	Power/Other	
J27	VCC	Power/Other	
J28	VCC	Power/Other	
J29	VCC	Power/Other	
J30	VCC	Power/Other	
K1	LINT0	CMOS Async	Input
K2	VSS	Power/Other	
K3	A20M#	CMOS Async	Input
K4	REQ0#	Source Sync	Input/Output
K5	VSS	Power/Other	
K6	REQ3#	Source Sync	Input/Output
K7	VSS	Power/Other	
K8	VCC	Power/Other	

Table 4-2. Land Listing by Land Number (Sheet 7 of 17)

Pin No.	Pin Name	Signal Buffer Type	Direction
K23	VCC	Power/Other	
K24	VCC	Power/Other	
K25	VCC	Power/Other	
K26	VCC	Power/Other	
K27	VCC	Power/Other	
K28	VCC	Power/Other	
K29	VCC	Power/Other	
K30	VCC	Power/Other	
L1	LINT1	CMOS Async	Input
L2	TESTHI11	Power/Other	Input
L3	VSS	Power/Other	
L4	A06#	Source Sync	Input/Output
L5	A05#	Source Sync	Input/Output
L6	VSS	Power/Other	
L7	VSS	Power/Other	
L8	VCC	Power/Other	
L23	VSS	Power/Other	
L24	VSS	Power/Other	
L25	VSS	Power/Other	
L26	VSS	Power/Other	
L27	VSS	Power/Other	
L28	VSS	Power/Other	
L29	VSS	Power/Other	
L30	VSS	Power/Other	
M1	VSS	Power/Other	
M2	THERMTRIP#	Open Drain	Output
M3	STPCLK#	CMOS Async	Input
M4	A07#	Source Sync	Input/Output
M5	A03#	Source Sync	Input/Output
M6	REQ2#	Source Sync	Input/Output
M7	VSS	Power/Other	
M8	VCC	Power/Other	
M23	VCC	Power/Other	
M24	VCC	Power/Other	
M25	VCC	Power/Other	
M26	VCC	Power/Other	
M27	VCC	Power/Other	
M28	VCC	Power/Other	
M29	VCC	Power/Other	
M30	VCC	Power/Other	
N1	PWRGOOD	Power/Other	Input
N2	IGNNE#	CMOS Async	Input
N3	VSS	Power/Other	
N4	A36#	Source Sync	Input/Output
N5	RESERVED		
N6	VSS	Power/Other	

Table 4-2. Land Listing by Land Number (Sheet 8 of 17)

Pin No.	Pin Name	Signal Buffer Type	Direction
N7	VSS	Power/Other	
N8	VCC	Power/Other	
N23	VCC	Power/Other	
N24	VCC	Power/Other	
N25	VCC	Power/Other	
N26	VCC	Power/Other	
N27	VCC	Power/Other	
N28	VCC	Power/Other	
N29	VCC	Power/Other	
N30	VCC	Power/Other	
P1	TESTHI10	Power/Other	Input
P2	SMI#	CMOS Async	Input
P3	INIT#	CMOS Async	Input
P4	VSS	Power/Other	
P5	A37#	Source Sync	Input/Output
P6	A04#	Source Sync	Input/Output
P7	VSS	Power/Other	
P8	VCC	Power/Other	
P23	VSS	Power/Other	
P24	VSS	Power/Other	
P25	VSS	Power/Other	
P26	VSS	Power/Other	
P27	VSS	Power/Other	
P28	VSS	Power/Other	
P29	VSS	Power/Other	
P30	VSS	Power/Other	
R1	COMP3	Power/Other	Input
R2	VSS	Power/Other	
R3	FERR#/PBE#	Open Drain	Output
R4	A08#	Source Sync	Input/Output
R5	VSS	Power/Other	
R6	ADSTB0#	Source Sync	Input/Output
R7	VSS	Power/Other	
R8	VCC	Power/Other	
R23	VSS	Power/Other	
R24	VSS	Power/Other	
R25	VSS	Power/Other	
R26	VSS	Power/Other	
R27	VSS	Power/Other	
R28	VSS	Power/Other	
R29	VSS	Power/Other	
R30	VSS	Power/Other	
T1	COMP1	Power/Other	Input
T2	RESERVED		
T3	VSS	Power/Other	
T4	A11#	Source Sync	Input/Output

Table 4-2. Land Listing by Land Number (Sheet 9 of 17)

Pin No.	Pin Name	Signal Buffer Type	Direction
T5	A09#	Source Sync	Input/Output
T6	VSS	Power/Other	
T7	VSS	Power/Other	
T8	VCC	Power/Other	
T23	VCC	Power/Other	
T24	VCC	Power/Other	
T25	VCC	Power/Other	
T26	VCC	Power/Other	
T27	VCC	Power/Other	
T28	VCC	Power/Other	
T29	VCC	Power/Other	
T30	VCC	Power/Other	
U1	TESTIN2	Power/Other	Input
U2	AP0#	Common Clk	Input/Output
U3	AP1#	Common Clk	Input/Output
U4	A13#	Source Sync	Input/Output
U5	A12#	Source Sync	Input/Output
U6	A10#	Source Sync	Input/Output
U7	VSS	Power/Other	
U8	VCC	Power/Other	
U23	VCC	Power/Other	
U24	VCC	Power/Other	
U25	VCC	Power/Other	
U26	VCC	Power/Other	
U27	VCC	Power/Other	
U28	VCC	Power/Other	
U29	VCC	Power/Other	
U30	VCC	Power/Other	
V1	MS_ID1	Power/Other	Output
V2	LL_ID0	Power/Other	Output
V3	VSS	Power/Other	
V4	A15#	Source Sync	Input/Output
V5	A14#	Source Sync	Input/Output
V6	VSS	Power/Other	
V7	VSS	Power/Other	
V8	VCC	Power/Other	
V23	VSS	Power/Other	
V24	VSS	Power/Other	
V25	VSS	Power/Other	
V26	VSS	Power/Other	
V27	VSS	Power/Other	
V28	VSS	Power/Other	
V29	VSS	Power/Other	
V30	VSS	Power/Other	
W1	MS_ID0	Power/Other	Output
W2	TESTIN1	Power/Other	Input

Table 4-2. Land Listing by Land Number (Sheet 10 of

Pin No.	Pin Name	Signal Buffer Type	Direction
W3	RESERVED		
W4	VSS	Power/Other	
W5	A16#	Source Sync	Input/Output
W6	A18#	Source Sync	Input/Output
W7	VSS	Power/Other	
W8	VCC	Power/Other	
W23	VCC	Power/Other	
W24	VCC	Power/Other	
W25	VCC	Power/Other	
W26	VCC	Power/Other	
W27	VCC	Power/Other	
W28	VCC	Power/Other	
W29	VCC	Power/Other	
W30	VCC	Power/Other	
Y1	RESERVED		
Y2	VSS	Power/Other	
Y3	RESERVED		
Y23	VCC	Power/Other	
Y4	A20#	Source Sync	Input/Output
Y5	VSS	Power/Other	
Y6	A19#	Source Sync	Input/Output
Y7	VSS	Power/Other	
Y8	VCC	Power/Other	
Y24	VCC	Power/Other	
Y25	VCC	Power/Other	
Y26	VCC	Power/Other	
Y27	VCC	Power/Other	
Y28	VCC	Power/Other	
Y29	VCC	Power/Other	
Y30	VCC	Power/Other	
AA1	VTT_OUT	Power/Other	Output
AA2	LL_ID1	Power/Other	Output
AA3	VSS	Power/Other	
AA4	A21#	Source Sync	Input/Output
AA5	A23#	Source Sync	Input/Output
AA6	VSS	Power/Other	
AA7	VSS	Power/Other	
AA8	VCC	Power/Other	
AA23	VSS	Power/Other	
AA24	VSS	Power/Other	
AA25	VSS	Power/Other	
AA26	VSS	Power/Other	
AA27	VSS	Power/Other	
AA28	VSS	Power/Other	
AA29	VSS	Power/Other	
AA30	VSS	Power/Other	

Table 4-2. Land Listing by Land Number (Sheet 11 of

Pin No.	Pin Name	Signal Buffer Type	Direction
AB1	VSS	Power/Other	
AB2	IERR#	Open Drain	Output
AB3	MCERR#	Common Clk	Input/Output
AB4	A26#	Source Sync	Input/Output
AB5	A24#	Source Sync	Input/Output
AB6	A17#	Source Sync	Input/Output
AB7	VSS	Power/Other	
AB8	VCC	Power/Other	
AB23	VSS	Power/Other	
AB24	VSS	Power/Other	
AB25	VSS	Power/Other	
AB26	VSS	Power/Other	
AB27	VSS	Power/Other	
AB28	VSS	Power/Other	
AB29	VSS	Power/Other	
AB30	VSS	Power/Other	
AC1	TMS	TAP	Input
AC2	DBR#	Power/Other	Output
AC3	VSS	Power/Other	
AC4	RESERVED		
AC5	A25#	Source Sync	Input/Output
AC6	VSS	Power/Other	
AC7	VSS	Power/Other	
AC8	VCC	Power/Other	
AC23	VCC	Power/Other	
AC24	VCC	Power/Other	
AC25	VCC	Power/Other	
AC26	VCC	Power/Other	
AC27	VCC	Power/Other	
AC28	VCC	Power/Other	
AC29	VCC	Power/Other	
AC30	VCC	Power/Other	
AD1	TDI	TAP	Input
AD2	BPM2#	Common Clk	Output
AD3	BINIT#	Common Clk	Input/Output
AD4	VSS	Power/Other	
AD5	ADSTB1#	Source Sync	Input/Output
AD6	A22#	Source Sync	Input/Output
AD7	VSS	Power/Other	
AD8	VCC	Power/Other	
AD23	VCC	Power/Other	
AD24	VCC	Power/Other	
AD25	VCC	Power/Other	
AD26	VCC	Power/Other	
AD27	VCC	Power/Other	
AD28	VCC	Power/Other	

Table 4-2. Land Listing by Land Number (Sheet 12 of

Pin No.	Pin Name	Signal Buffer Type	Direction
AD29	VCC	Power/Other	
AD30	VCC	Power/Other	
AE1	TCK	TAP	Input
AE2	VSS	Power/Other	
AE3	TESTHI12	Power/Other	Input
AE4	RESERVED		
AE5	VSS	Power/Other	
AE6	RESERVED		
AE7	VSS	Power/Other	
AE8	SKTOCC#	Power/Other	Output
AE9	VCC	Power/Other	
AE10	VSS	Power/Other	
AE11	VCC	Power/Other	
AE12	VCC	Power/Other	
AE13	VSS	Power/Other	
AE14	VCC	Power/Other	
AE15	VCC	Power/Other	
AE16	VSS	Power/Other	
AE17	VSS	Power/Other	
AE18	VCC	Power/Other	
AE19	VCC	Power/Other	
AE20	VSS	Power/Other	
AE21	VCC	Power/Other	
AE22	VCC	Power/Other	
AE23	VCC	Power/Other	
AE24	VSS	Power/Other	
AE25	VSS	Power/Other	
AE26	VSS	Power/Other	
AE27	VSS	Power/Other	
AE28	VSS	Power/Other	
AE29	VSS	Power/Other	
AE30	VSS	Power/Other	
AF1	TDO	TAP	Output
AF2	BPM4#	Common Clk	Output
AF3	VSS	Power/Other	
AF4	A28#	Source Sync	Input/Output
AF5	A27#	Source Sync	Input/Output
AF6	VSS	Power/Other	
AF7	VSS	Power/Other	
AF8	VCC	Power/Other	
AF9	VCC	Power/Other	
AF10	VSS	Power/Other	
AF11	VCC	Power/Other	
AF12	VCC	Power/Other	
AF13	VSS	Power/Other	
AF14	VCC	Power/Other	

Table 4-2. Land Listing by Land Number (Sheet 13 of

Pin No.	Pin Name	Signal Buffer Type	Direction
AF15	VCC	Power/Other	
AF16	VSS	Power/Other	
AF17	VSS	Power/Other	
AF18	VCC	Power/Other	
AF19	VCC	Power/Other	
AF20	VSS	Power/Other	
AF21	VCC	Power/Other	
AF22	VCC	Power/Other	
AF23	VSS	Power/Other	
AF24	VSS	Power/Other	
AF25	VSS	Power/Other	
AF26	VSS	Power/Other	
AF27	VSS	Power/Other	
AF28	VSS	Power/Other	
AF29	VSS	Power/Other	
AF30	VSS	Power/Other	
AG1	TRST#	TAP	Input
AG2	BPM3#	Common Clk	Input/Output
AG3	BPM5#	Common Clk	Input/Output
AG4	A30#	Source Sync	Input/Output
AG5	A31#	Source Sync	Input/Output
AG6	A29#	Source Sync	Input/Output
AG7	VSS	Power/Other	
AG8	VCC	Power/Other	
AG9	VCC	Power/Other	
AG10	VSS	Power/Other	
AG11	VCC	Power/Other	
AG12	VCC	Power/Other	
AG13	VSS	Power/Other	
AG14	VCC	Power/Other	
AG15	VCC	Power/Other	
AG16	VSS	Power/Other	
AG17	VSS	Power/Other	
AG18	VCC	Power/Other	
AG19	VCC	Power/Other	
AG20	VSS	Power/Other	
AG21	VCC	Power/Other	
AG22	VCC	Power/Other	
AG23	VSS	Power/Other	
AG24	VSS	Power/Other	
AG25	VCC	Power/Other	
AG26	VCC	Power/Other	
AG27	VCC	Power/Other	
AG28	VCC	Power/Other	
AG29	VCC	Power/Other	
AG30	VCC	Power/Other	

Table 4-2. Land Listing by Land Number (Sheet 14 of

Pin No.	Pin Name	Signal Buffer Type	Direction
AH1	VSS	Power/Other	
AH2	RESERVED		
AH3	VSS	Power/Other	
AH4	A32#	Source Sync	Input/Output
AH5	A33#	Source Sync	Input/Output
AH6	VSS	Power/Other	
AH7	RESERVED		
AH8	VCC	Power/Other	
AH9	VCC	Power/Other	
AH10	VSS	Power/Other	
AH11	VCC	Power/Other	
AH12	VCC	Power/Other	
AH13	VSS	Power/Other	
AH14	VCC	Power/Other	
AH15	VCC	Power/Other	
AH16	VSS	Power/Other	
AH17	VSS	Power/Other	
AH18	VCC	Power/Other	
AH19	VCC	Power/Other	
AH20	VSS	Power/Other	
AH21	VCC	Power/Other	
AH22	VCC	Power/Other	
AH23	VSS	Power/Other	
AH24	VSS	Power/Other	
AH25	VCC	Power/Other	
AH26	VCC	Power/Other	
AH27	VCC	Power/Other	
AH28	VCC	Power/Other	
AH29	VCC	Power/Other	
AH30	VCC	Power/Other	
AJ1	BPM1#	Common Clk	Output
AJ2	BPM0#	Common Clk	Input/Output
AJ3	RESERVED		
AJ4	VSS	Power/Other	
AJ5	A34#	Source Sync	Input/Output
AJ6	A35#	Source Sync	Input/Output
AJ7	RESERVED		
AJ8	VCC	Power/Other	
AJ9	VCC	Power/Other	
AJ10	VSS	Power/Other	
AJ11	VCC	Power/Other	
AJ12	VCC	Power/Other	
AJ13	VSS	Power/Other	
AJ14	VCC	Power/Other	
AJ15	VCC	Power/Other	
AJ16	VSS	Power/Other	

Table 4-2. Land Listing by Land Number (Sheet 15 of

Pin No.	Pin Name	Signal Buffer Type	Direction
AJ17	VSS	Power/Other	
AJ18	VCC	Power/Other	
AJ19	VCC	Power/Other	
AJ20	VSS	Power/Other	
AJ21	VCC	Power/Other	
AJ22	VCC	Power/Other	
AJ23	VSS	Power/Other	
AJ24	VSS	Power/Other	
AJ25	VCC	Power/Other	
AJ26	VCC	Power/Other	
AJ27	VSS	Power/Other	
AJ28	VSS	Power/Other	
AJ29	VSS	Power/Other	
AJ30	VSS	Power/Other	
AK1	RESERVED		
AK2	VSS	Power/Other	
AK3	RESERVED		
AK4	VID4	CMOS Async	Output
AK5	VSS	Power/Other	
AK6	FORCEPR#	CMOS Async	Input
AK7	VSS	Power/Other	
AK8	VCC	Power/Other	
AK9	VCC	Power/Other	
AK10	VSS	Power/Other	
AK11	VCC	Power/Other	
AK12	VCC	Power/Other	
AK13	VSS	Power/Other	
AK14	VCC	Power/Other	
AK15	VCC	Power/Other	
AK16	VSS	Power/Other	
AK17	VSS	Power/Other	
AK18	VCC	Power/Other	
AK19	VCC	Power/Other	
AK20	VSS	Power/Other	
AK21	VCC	Power/Other	
AK22	VCC	Power/Other	
AK23	VSS	Power/Other	
AK24	VSS	Power/Other	
AK25	VCC	Power/Other	
AK26	VCC	Power/Other	
AK27	VSS	Power/Other	
AK28	VSS	Power/Other	
AK29	VSS	Power/Other	
AK30	VSS	Power/Other	
AL1	RESERVED		
AL2	PROCHOT#	Open Drain	Output

Table 4-2. Land Listing by Land Number (Sheet 16 of

Pin No.	Pin Name	Signal Buffer Type	Direction
AL3	VSS	Power/Other	
AL4	VID5	CMOS Async	Output
AL5	VID1	CMOS Async	Output
AL6	VID3	CMOS Async	Output
AL7	VSS_DIE_ SENSE2	Power/Other	
AL8	VCC_DIE_ SENSE2	Power/Other	
AL9	VCC	Power/Other	
AL10	VSS	Power/Other	
AL11	VCC	Power/Other	
AL12	VCC	Power/Other	
AL13	VSS	Power/Other	
AL14	VCC	Power/Other	
AL15	VCC	Power/Other	
AL16	VSS	Power/Other	
AL17	VSS	Power/Other	
AL18	VCC	Power/Other	
AL19	VCC	Power/Other	
AL20	VSS	Power/Other	
AL21	VCC	Power/Other	
AL22	VCC	Power/Other	
AL23	VSS	Power/Other	
AL24	VSS	Power/Other	
AL25	VCC	Power/Other	
AL26	VCC	Power/Other	
AL27	VSS	Power/Other	
AL28	VSS	Power/Other	
AL29	VCC	Power/Other	
AL30	VCC	Power/Other	
AM1	VSS	Power/Other	
AM2	RESERVED		
AM3	VID2	CMOS Async	Output
AM4	VSS	Power/Other	
AM5	VID6	CMOS Async	Output
AM6	RESERVED		
AM7	VSS	Power/Other	
AM8	VCC	Power/Other	
AM9	VCC	Power/Other	
AM10	VSS	Power/Other	
AM11	VCC	Power/Other	
AM12	VCC	Power/Other	
AM13	VSS	Power/Other	
AM14	VCC	Power/Other	
AM15	VCC	Power/Other	
AM16	VSS	Power/Other	
AM17	VSS	Power/Other	

Table 4-2. Land Listing by Land Number (Sheet 17 of

Pin No.	Pin Name	Signal Buffer Type	Direction
AM18	VCC	Power/Other	
AM19	VCC	Power/Other	
AM20	VSS	Power/Other	
AM21	VCC	Power/Other	
AM22	VCC	Power/Other	
AM23	VSS	Power/Other	
AM24	VSS	Power/Other	
AM25	VCC	Power/Other	
AM26	VCC	Power/Other	
AM27	VSS	Power/Other	
AM28	VSS	Power/Other	
AM29	VCC	Power/Other	
AM30	VCC	Power/Other	
AN1	VSS	Power/Other	
AN2	VSS	Power/Other	
AN3	VCC_DIE_ SENSE	Power/Other	Output
AN4	VSS_DIE_ SENSE	Power/Other	Output
AN5	RESERVED		
AN6	RESERVED		
AN7	VID_SELECT	Power/Other	Output
AN8	VCC	Power/Other	
AN9	VCC	Power/Other	
AN10	VSS	Power/Other	
AN11	VCC	Power/Other	
AN12	VCC	Power/Other	
AN13	VSS	Power/Other	
AN14	VCC	Power/Other	
AN15	VCC	Power/Other	
AN16	VSS	Power/Other	
AN17	VSS	Power/Other	
AN18	VCC	Power/Other	
AN19	VCC	Power/Other	
AN20	VSS	Power/Other	
AN21	VCC	Power/Other	
AN22	VCC	Power/Other	
AN23	VSS	Power/Other	
AN24	VSS	Power/Other	
AN25	VCC	Power/Other	
AN26	VCC	Power/Other	

4.2 Signal Definitions

Table 4-1. Signal Definitions (Sheet 1 of 11)

Name	Type	Description	Notes
A[37:3]#	I/O	A[37:3]# (Address) define a 2^{38}-byte physical memory address space. In sub-phase 1 of the address phase, these signals transmit the address of a transaction. In sub-phase 2, these signals transmit transaction type information. These signals must connect the appropriate pins of all agents on the FSB. A[37:3]# are protected by parity signals AP[1:0]#. A[37:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. On the active-to-inactive transition of RESET#, the processors sample a subset of the A[37:3]# lands to determine their power-on configuration. See Section 6.1.	3
A20M#	I	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1 MB boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O write bus transaction.	2
ADS#	I/O	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[37:3]# lands. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction. This signal must be connected to the appropriate pins on all processor FSB agents.	3
ADSTB[1:0]#	I/O	Address strobes are used to latch A[37:3]# and REQ[4:0]# on their rising and falling edge. Strobes are associated with signals as shown below. **Signals** / **Associated Strobes** REQ[4:0]#, A[16:3]#, A[37:36]# — ADSTB0# A[35:17]# — ADSTB1#	3

Table 4-1. Signal Definitions (Sheet 2 of 11)

Name	Type	Description	Notes
AP[1:0]#	I/O	AP[1:0]# (Address Parity) are driven by the request initiator along with ADS#, A[37:3]#, and the transaction type on the REQ[4:0]# signals. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# must be connected to the appropriate pins of all processor FSB agents. The following table defines the coverage model of these signals. **Request Signals / Subphase 1 / Subphase 2** A[37:24]# / AP0# / AP1# A[23:3]# / AP1# / AP0# REQ[4:0]# / AP1# / AP0#	3
BCLK[1:0]	I	The differential bus clock pair BCLK[1:0] (Bus Clock) determines the FSB frequency. All processor FSB agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of BCLK0 crossing V_{CROSS}.	3
BINIT#	I/O	BINIT# (Bus Initialization) may be observed and driven by all processor FSB agents and if used, must connect the appropriate pins of all such agents. If the BINIT# driver is enabled during power on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future operation. If BINIT# observation is enabled during power-on configuration (see Section 6.1) and BINIT# is sampled asserted, symmetric agents reset their bus LOCK# activity and bus request arbitration state machines. The bus agents do not reset their I/O Queue (IOQ) and transaction tracking state machines upon observation of BINIT# assertion. Once the BINIT# assertion has been observed, the bus agents will re-arbitrate for the FSB and attempt completion of their bus queue and IOQ entries. If BINIT# observation is disabled during power-on configuration, a priority agent may handle an assertion of BINIT# as appropriate to the error handling architecture of the system.	3
BNR#	I/O	BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions. Since multiple agents might need to request a bus stall at the same time, BNR# is a wired-OR signal which must connect the appropriate pins of all processor FSB agents. In order to avoid wired-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.	3

Table 4-1. Signal Definitions (Sheet 3 of 11)

Name	Type	Description	Notes
BPM5# BPM4# BPM3# BPM[2:1]# BPM0#	I/O O I/O O I/O	BPM[5:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[5:0]# should connect the appropriate pins of all FSB agents. BPM4# provides PRDY# (Probe Ready) functionality for the TAP port. PRDY# is a processor output used by debug tools to determine processor debug readiness. BPM5# provides PREQ# (Probe Request) functionality for the TAP port. PREQ# is used by debug tools to request debug operation of the processors. BPM[5:4]# must be bussed to all bus agents.	2
BPMb3# BPMb[2:1]# BPMb0#	I/O O I/O	BPMb[3:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPMb[3:0]# should connect the appropriate pins of all FSB agents.	
BPRI#	I	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor FSB. It must connect the appropriate pins of all processor FSB agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.	3
BR[1:0]#	I/O	The BR[1:0]# signals are sampled on the active-to-inactive transition of RESET#. The signal which the agent samples asserted determines its agent ID. BR0# drives the BREQ0# signal in the system and is used by the processor to request the bus. These signals do not have on-die termination and must be terminated.	3
BSEL[2:0]	O	The BCLK[1:0] frequency select signals BSEL[2:0] are used to select the processor input clock frequency. Table 2-2 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processors, chipset, and clock synthesizer. All FSB agents must operate at the same frequency.	
COMP[3:0]	I	COMP[3:0] must be terminated to VSS on the baseboard using precision resistors. These inputs configure the AGTL+ drivers of the processor.	

Table 4-1. Signal Definitions (Sheet 4 of 11)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th><th>Notes</th></tr>
<tr><td>D[63:0]#</td><td>I/O</td><td>D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor FSB agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer.
D[63:0]# are quad-pumped signals, and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to strobes and DBI#.
<table><tr><th>Data Group</th><th>DSTBN# / DSTBP#</th><th>DBI#</th></tr><tr><td>D[15:0]#</td><td>0</td><td>0</td></tr><tr><td>D[31:16]#</td><td>1</td><td>1</td></tr><tr><td>D[47:32]#</td><td>2</td><td>2</td></tr><tr><td>D[63:48]#</td><td>3</td><td>3</td></tr></table>Furthermore, the DBI# signals determine the polarity of the data signals. Each group of 16 data signals corresponds to one DBI# signal. When the DBI# signal is active, the corresponding data group is inverted and therefore sampled active high.</td><td>3</td></tr>
<tr><td>DBI[3:0]#</td><td>I/O</td><td>DBI[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DBI[3:0]# signals are activated when the data on the data bus is inverted. If more than half the data bits, within, within a 16-bit group, would have been asserted electronically low, the bus agent may invert the data bus signals for that particular sub-phase for that 16-bit group.
DBI[3:0] Assignment to Data Bus
<table><tr><th>Bus Signal</th><th>Data Bus Signals</th></tr><tr><td>DBI0#</td><td>D[15:0]#</td></tr><tr><td>DBI1#</td><td>D[31:16]#</td></tr><tr><td>DBI2#</td><td>D[47:32]#</td></tr><tr><td>DBI3#</td><td>D[63:48]#</td></tr></table></td><td>3</td></tr>
<tr><td>DBR#</td><td>O</td><td>DBR# is used only in systems where no debug port connector is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port connector is implemented in the system, DBR# is a no-connect on the processor package. DBR# is not a processor signal.</td><td></td></tr>
</table>

Table 4-1. Signal Definitions (Sheet 5 of 11)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th><th>Notes</th></tr>
<tr><td>DBSY#</td><td>I/O</td><td>DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor FSB to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on all processor FSB agents.</td><td>3</td></tr>
<tr><td>DEFER#</td><td>I</td><td>DEFER# is asserted by an agent to indicate that a transaction cannot be ensured in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or I/O agent. This signal must connect the appropriate pins of all processor FSB agents.</td><td>3</td></tr>
<tr><td>DP[3:0]#</td><td>I/O</td><td>DP[3:0]# (Data Parity) provide parity protection for the D[63:0]# signals. They are driven by the agent responsible for driving D[63:0]#, and must connect the appropriate pins of all processor FSB agents.</td><td>3</td></tr>
<tr><td>DRDY#</td><td>I/O</td><td>DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of all processor FSB agents.</td><td>3</td></tr>
<tr><td>DSTBN[3:0]#</td><td>I/O</td><td>Data strobe used to latch in D[63:0]#.
<table><tr><th>Signals</th><th>Associated Strobes</th></tr><tr><td>D[15:0]#, DBI0#</td><td>DSTBN0#</td></tr><tr><td>D[31:16]#, DBI1#</td><td>DSTBN1#</td></tr><tr><td>D[47:32]#, DBI2#</td><td>DSTBN2#</td></tr><tr><td>D[63:48]#, DBI3#</td><td>DSTBN3#</td></tr></table></td><td>3</td></tr>
<tr><td>DSTBP[3:0]#</td><td>I/O</td><td>Data strobe used to latch in D[63:0]#.
<table><tr><th>Signals</th><th>Associated Strobes</th></tr><tr><td>D[15:0]#, DBI0#</td><td>DSTBP0#</td></tr><tr><td>D[31:16]#, DBI1#</td><td>DSTBP1#</td></tr><tr><td>D[47:32]#, DBI2#</td><td>DSTBP2#</td></tr><tr><td>D[63:48]#, DBI3#</td><td>DSTBP3#</td></tr></table></td><td>3</td></tr>
</table>

Table 4-1. Signal Definitions (Sheet 6 of 11)

Name	Type	Description	Notes
FERR#/PBE#	O	FERR#/PBE# (floating-point error/pending break event) is a multiplexed signal and its meaning is qualified by STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating-point error and will be asserted when the processor detects an unmasked floating-point error. When STPCLK# is not asserted, FERR#/PBE# is similar to the ERROR# signal on the Intel® 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. For additional information on the pending break event functionality, including the identification of support of the feature and enable/disable information, refer to Vol. 3 of the *Intel® 64 and IA-32 Architectures Software Developer's Manual* and the *Intel Processor Identification and the CPUID Instruction* application note.	2
FORCEPR#	I	The FORCEPR# (force power reduction) input can be used by the platform to cause the processor to activate the Thermal Control Circuit (TCC).	
GTLREF_ADD_MID GTLREF_ADD_END	I	GTLREF_ADD determines the signal reference level for AGTL+ address and common clock input lands. GTLREF_ADD is used by the AGTL+ receivers to determine if a signal is a logical 0 or a logical 1. Refer to Table 2-18 for additional details.	
GTLREF_DATA_MID GTLREF_DATA_END	I	GTLREF_DATA determines the signal reference level for AGTL+ data input lands. GTLREF_DATA is used by the AGTL+ receivers to determine if a signal is a logical 0 or a logical 1. Refer to Table 2-18 for additional details.	
HIT# HITM#	I/O I/O	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Any FSB agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.	3
IERR#	O	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor FSB. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#. This signal does not have on-die termination.	2

Table 4-1. Signal Definitions (Sheet 7 of 11)

Name	Type	Description	Notes
IGNNE#	I	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O write bus transaction.	2
INIT#	I	INIT# (Initialization), when asserted, resets integer registers inside all processors without affecting their internal caches or floating-point registers. Each processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all processor FSB agents.	2
LINT[1:0]	I	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all FSB agents. When the APIC functionality is disabled, the LINT0/INTR signal becomes INTR, a maskable interrupt request signal, and LINT1/NMI becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium® processor. Both signals are asynchronous. These signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.	2
LL_ID[1:0]	O	The LL_ID[1:0] signals are used to select the correct loadline slope for the processor. These signals are not connected to the processor die.	
LOCK#	I/O	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all processor FSB agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor FSB, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor FSB throughout the bus locked operation and ensure the atomicity of lock.	3

Table 4-1. Signal Definitions (Sheet 8 of 11)

Name	Type	Description	Notes
MCERR#	I/O	MCERR# (Machine Check Error) is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all processor FSB agents. MCERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options: • Enabled or disabled. • Asserted, if configured, for internal errors along with IERR#. • Asserted, if configured, by the request initiator of a bus transaction after it observes an error. • Asserted by any bus agent when it observes an error in a bus transaction. For more details regarding machine check architecture, refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manual*, Volume 3.	
MS_ID[1:0]	O	These signals are provided to indicate the Market Segment for the processor and may be used for future processor compatibility or for keying. These signals are not connected to the processor die. Both the bits 0 and 1 are logic 1 and are no connects on the package.	
PROCHOT#	O	PROCHOT# (Processor Hot) will go active when the processor's temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the Thermal Control Circuit (TCC) has been activated, if enabled. The TCC will remain active until shortly after the processor deasserts PROCHOT#. See Section 5.2.3 for more details.	
PWRGOOD	I	PWRGOOD (Power Good) is an input. The processor requires this signal to be a clean indication that all processor clocks and power supplies are stable and within their specifications. "Clean" implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.	2
REQ[4:0]#	I/O	REQ[4:0]# (Request Command) must connect the appropriate pins of all processor FSB agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[1:0]#. Refer to the AP[1:0]# signal description for details on parity checking of these signals.	3

Table 4-1. Signal Definitions (Sheet 9 of 11)

Name	Type	Description	Notes
RESET#	I	Asserting the RESET# signal resets all processors to known states and invalidates their internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least 1 ms after VCC and BCLK have reached their proper specifications. On observing active RESET#, all FSB agents will deassert their outputs within two clocks. RESET# must not be kept asserted for more than 10 ms while PWRGOOD is asserted. A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the Section 6.1. This signal does not have on-die termination and must be terminated on the system board.	3
RS[2:0]#	I	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor FSB agents.	3
RSP#	I	RSP# (Response Parity) is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect to the appropriate pins of all processor FSB agents. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. While RS[2:0]# = 000, RSP# is also high, since this indicates it is not being driven by any agent ensuring correct parity.	3
SKTOCC#	O	SKTOCC# (Socket occupied) will be pulled to ground by the processor to indicate that the processor is present. There is no connection to the processor silicon for this signal.	
SMI#	I	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, processors save the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tri-state its outputs. See Section 6.1.	2
STPCLK#	I	STPCLK# (Stop Clock), when asserted, causes processors to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the FSB and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.	2

Table 4-1. Signal Definitions (Sheet 10 of 11)

Name	Type	Description	Notes
TCK	I	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).	
TDI	I	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.	
TDO	O	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.	
TESTHI[12:10]	I	TESTHI[12:10] must be connected to a V_{TT} power source through a resistor for proper processor operation. Refer to Section 2.6 for TESTHI grouping restrictions.	
TESTIN1 TESTIN2	I I	TESTIN1 must be connected to a VTT power source through a resistor as well as to the TESTIN2 land of the same socket for proper processor operation. TESTIN2 must be connected to a VTT power source through a resistor as well as to the TESTIN1 land of the same socket for proper processor operation.	
THERMTRIP#	O	Assertion of THERMTRIP# (Thermal Trip) indicates the processor junction temperature has reached a temperature beyond which permanent silicon damage may occur. Measurement of the temperature is accomplished through an internal thermal sensor. Upon assertion of THERMTRIP#, the processor will shut off its internal clocks (thus halting program execution) in an attempt to reduce the processor junction temperature. To protect the processor its core voltage (V_{CC}) must be removed following the assertion of THERMTRIP#. Intel also recommends the removal of V_{TT} when THERMTRIP# is asserted. Driving of the THERMTRIP# signals is enabled within 10 µs of the assertion of PWRGOOD and is disabled on de-assertion of PWRGOOD. Once activated, THERMTRIP# remains latched until PWRGOOD is de-asserted. While the de-assertion of the PWRGOOD signal will de-assert THERMTRIP#, if the processor's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted within 10 µs of the assertion of PWRGOOD.	1
TMS	I	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.	
TRDY#	I	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all FSB agents.	
TRST#	I	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.	
VCCPLL	I	The processor implements an on-die PLL filter solution. The VCCPLL input is used as a PLL supply voltage.	

Table 4-1. Signal Definitions (Sheet 11 of 11)

Name	Type	Description	Notes
VCC_DIE_SENSE VCC_DIE_SENSE2	O	VCC_DIE_SENSE and VCC_DIE_SENSE2 provides an isolated, low impedance connection to the processor core power and ground. This signal should be connected to the voltage regulator feedback signal, which insures the output voltage (that is, processor voltage) remains within specification.	
VID[6:1]	O	VID[6:1] (Voltage ID) pins are used to support automatic selection of power supply voltages (V_{CC}). These are CMOS signals that are driven by the processor and must be pulled up through a resistor. Conversely, the voltage regulator output must be disabled prior to the voltage supply for these pins becomes invalid. The VID pins are needed to support processor voltage specification variations. See Table 2-4 for definitions of these pins. The VR must supply the voltage that is requested by these pins, or disable itself.	
VID_SELECT	O	VID_SELECT is an output from the processor which selects the appropriate VID table for the Voltage Regulator. This signal is not connected to the processor die. This signal is a no-connect on the processor package.	
VSS_DIE_SENSE VSS_DIE_SENSE2	O	VSS_DIE_SENSE and VSS_DIE_SENSE2 provides an isolated, low impedance connection to the processor core power and ground. This signal should be connected to the voltage regulator feedback signal, which insures the output voltage (that is, processor voltage) remains within specification.	
VTT	P	The FSB termination voltage input pins. Refer to Table 2-12 for further details.	
VTT_OUT	O	The VTT_OUT signals are included in order to provide a local V_{TT} for some signals that require termination to V_{TT} on the motherboard.	
VTT_SEL	O	The VTT_SEL signal is used to select the correct V_{TT} voltage level for the processor. VTT_SEL is connected to VSS on the processor package.	

NOTES:
1. For this processor land, the maximum number of symmetric agents is one. Maximum number of priority agents is zero.
2. For this processor land, the maximum number of symmetric agents is two. Maximum number of priority agents is zero.
3. For this processor land, the maximum number of symmetric agents is two. Maximum number of priority agents is one.

§

5 Thermal Specifications

5.1 Package Thermal Specifications

The processor requires a thermal solution to maintain temperatures within its operating limits. Any attempt to operate the processor outside these operating limits may result in permanent damage to the processor and potentially other components within the system. As processor technology changes, thermal management becomes increasingly crucial when building computer systems. Maintaining the proper thermal environment is key to reliable, long-term system operation.

A complete solution includes both component and system level thermal management features. Component level thermal solutions can include active or passive heatsinks attached to the processor integrated heat spreader (IHS). Typical system level thermal solutions may consist of system fans combined with ducting and venting.

This section provides data necessary for developing a complete thermal solution. For more information on designing a component level thermal solution, refer to the appropriate processor Thermal and Mechanical Design Guidelines (see Section 1.2).

5.1.1 Thermal Specifications

To allow the optimal operation and long-term reliability of Intel processor-based systems, the processor must remain within the minimum and maximum case temperature (TCASE) specifications as defined by the applicable thermal profile Table 5-1 and Figure 5-1. Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system. For more details on thermal solution design, refer to the appropriate processor Thermal and Mechanical Design Guidelines (see Section 1.2).

The processor implements a methodology for managing processor temperatures which is intended to support acoustic noise reduction through fan speed control and to assure processor reliability. Selection of the appropriate fan speed is based on the relative temperature data reported by the processor's Platform Environment Control Interface (PECI) bus as described in Section 5.3. If the value reported via PECI is less than $T_{CONTROL}$, then the case temperature is permitted to exceed the Thermal Profile. If the value reported via PECI is greater than or equal to $T_{CONTROL}$, then the processor case temperature must remain at or below the temperature as specified by the thermal. The temperature reported over PECI is always a negative value and represents a delta below the onset of thermal control circuit (TCC) activation, as indicated by PROCHOT# (see Section 5.2, Processor Thermal Features). Systems that implement fan speed control must be designed to use this data. Systems that do not alter the fan speed only need to ensure the case temperature meets the thermal profile specifications.

The processor supports a single Thermal Profile (see Figure 5-1, Table 5-1). With this Thermal Profile, it is expected that the Thermal Control Circuit (TCC) would only be activated for very brief periods of time when running the most power-intensive applications. Refer to the appropriate processor Thermal and Mechanical Design Guidelines (see Section 1.2) for details on system thermal solution design, thermal profiles and environmental considerations.

Analysis indicates that real applications are unlikely to cause the processor to consume maximum power dissipation for sustained time periods. Intel recommends that complete thermal solution designs target the Thermal Design Power (TDP) indicated in Table 5-1 for the processor, instead of the maximum processor power consumption. The Thermal Monitor feature is intended to help protect the processor in the event that an application exceeds the TDP recommendation for a sustained time period. For more

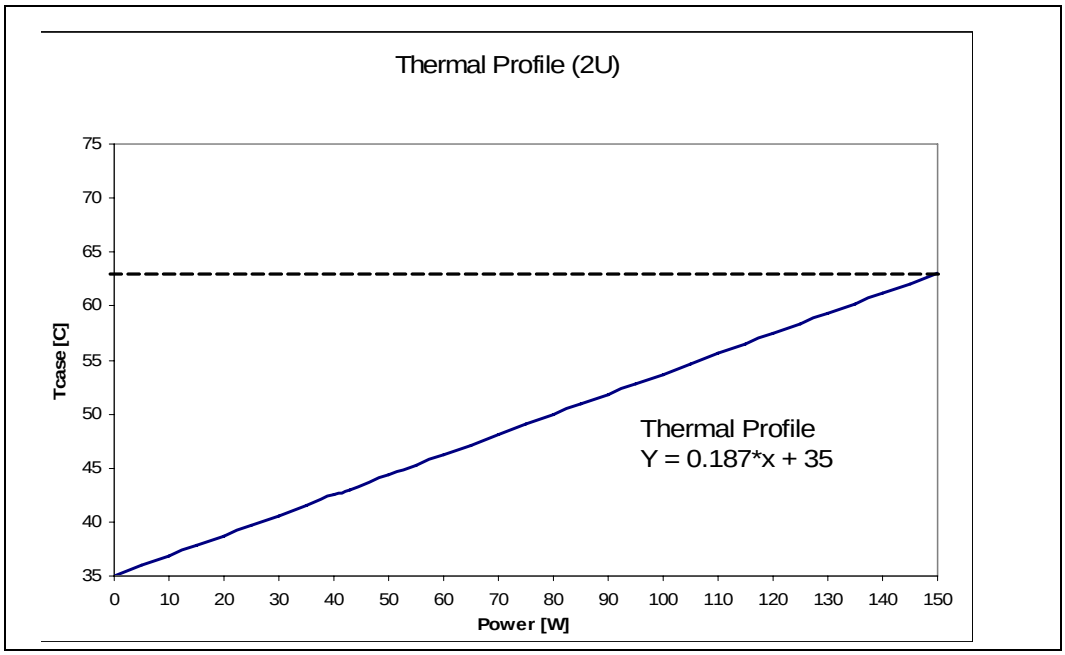
details on this feature, refer to Section 5.2. **Thermal Monitor 1 and Thermal Monitor 2 feature must be enabled for the processor to remain within its specifications.**

Table 5-1. Processor Thermal Specifications

Core Frequency	Maximum Power (W)	Thermal Design Power (W)	Minimum T_{CASE} (°C)	Maximum T_{CASE} (°C)	Notes
QX9775	155	150	5	See Figure 5-1; Table 5-2	1,2,3,4,5

NOTES:
1. These values are specified at V_{CC_MAX} for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} at specified I_{CC}. Refer to the loadline specifications in Section 2.13.
2. Thermal Design Power (TDP) should be used for the processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum T_{CASE}.
3. These specifications are based on silicon characterization.
4. Power specifications are defined at all VIDs found in Table 2-3. The processor may be shipped under multiple VIDs for each frequency.
5. The processor s intended for dual processor workstations only.

Figure 5-1. Processor Thermal Profile



NOTES:
1. Refer to Table 5-2 for discrete points that constitute the thermal profile.
2. Implementation of the processor Thermal Profile should result in virtually no TCC activation. Furthermore, utilization of thermal solutions that do not meet the processor Thermal Profile will result in increased probability of TCC activation and may incur measurable performance loss. Refer to the appropriate processor Thermal and Mechanical Design Guidelines (see Section 1.2) for system and environmental implementation details.

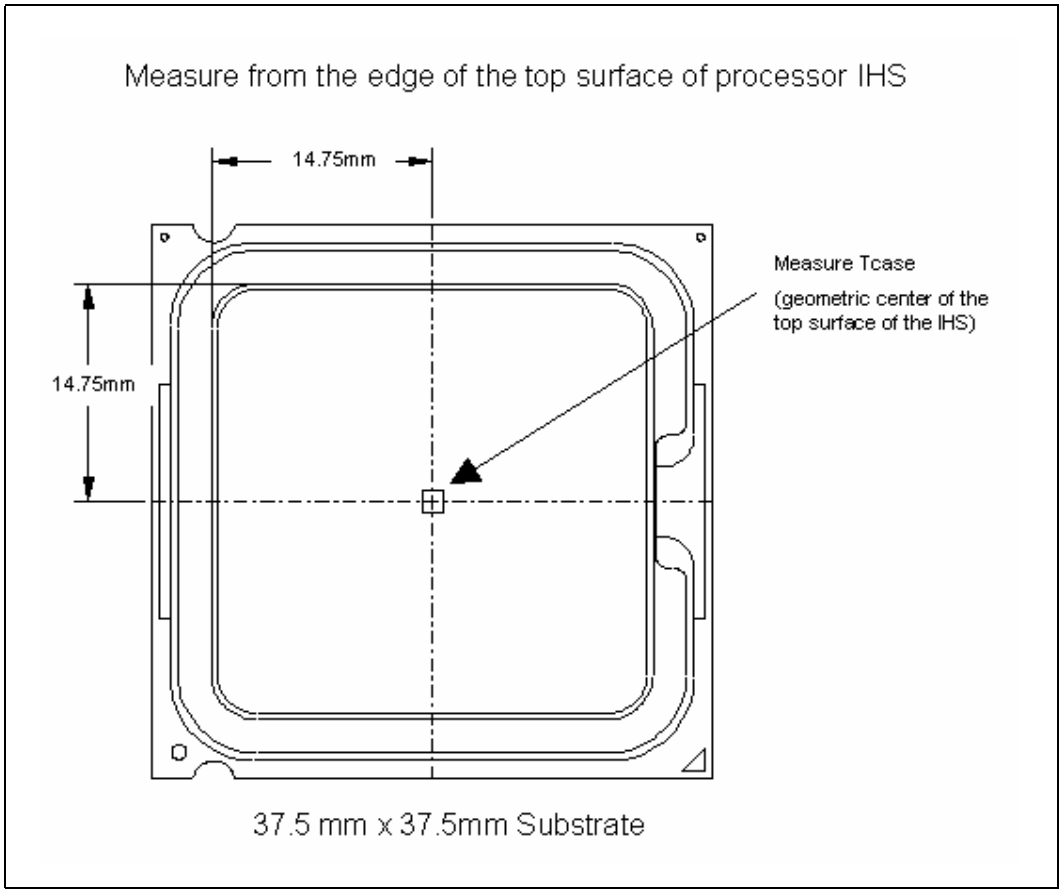
Table 5-2. Processor Thermal Profile Table

Power (W)	T_{CASE_MAX} (°C)	Power (W)	T_{CASE_MAX} (°C)
0	35.0	80	50.0
5	35.9	85	50.9
10	36.9	90	51.8
15	37.8	95	52.8
20	38.7	100	53.7
25	39.7	105	54.6
30	40.6	110	55.6
35	41.5	115	56.5
40	42.5	120	57.4
45	43.0	125	58.4
50	44.4	130	59.3
55	45.3	135	60.2
60	46.2	140	61.2
65	47.2	145	62.1
70	48.1	150	63.0
75	49.0		

5.1.2 Thermal Metrology

The minimum and maximum case temperatures (T_{CASE}) are specified in Table 5-2 is measured at the geometric top center of the processor integrated heat spreader (IHS). Figure 5-2 illustrates the location where T_{CASE} temperature measurements should be made. For detailed guidelines on temperature measurement methodology, refer to the appropriate processor Thermal and Mechanical Design Guidelines (see Section 1.2).

Figure 5-2. Case Temperature (T_{CASE}) Measurement Location



NOTE: Figure is not to scale and is for reference only.

5.2 Processor Thermal Features

5.2.1 Intel® Thermal Monitor Features

The processor provides two thermal monitor features — Thermal Monitor (TM1) and Enhanced Thermal Monitor (TM2). The Thermal Monitor and Enhanced Thermal Monitor must both be enabled in BIOS for the processor to be operating within specifications. When both are enabled, TM2 will be activated first and TM1 will be added if TM2 is not effective.

5.2.1.1 Thermal Monitor (TM1)

The Thermal Monitor (TM1) feature helps control the processor temperature by activating the Thermal Control Circuit (TCC) when the processor silicon reaches its maximum operating temperature. The TCC reduces processor power consumption as needed by modulating (starting and stopping) the internal processor core clocks. The temperature at which Thermal Monitor activates the thermal control circuit is not user configurable and is not software visible. Bus traffic is snooped in the normal manner, and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

When the TM1 is enabled, and a high temperature situation exists (that is, TCC is active), the clocks will be modulated by alternately turning the clocks off and on at a duty cycle specific to the processor (typically 30 – 50%). Cycle times are processor speed dependent and will decrease as processor core frequencies increase. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the TCC goes inactive and clock modulation ceases.

With thermal solutions designed to the processor Thermal Profile, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable. Refer to the appropriate processor Thermal and Mechanical Design Guidelines (see Section 1.2).

The duty cycle for the TCC, when activated by the TM1, is factory configured and cannot be modified. The TM1 does not require any additional hardware, software drivers, or interrupt handling routines.

5.2.1.2 Enhanced Thermal Monitor (TM2)

The processor adds supports for an Enhanced Thermal Monitor capability known as Thermal Monitor 2 (TM2). This mechanism provides an efficient means for limiting the processor temperature by reducing the power consumption within the processor. TM2 requires support for dynamic VID transitions in the platform.

When Thermal Monitor 2 is enabled, and a high temperature situation is detected, the Thermal Control Circuit (TCC) will be activated for both processor cores. The TCC causes the processor to adjust its operating frequency (via the bus multiplier) and input voltage (via the VID signals). This combination of reduced frequency and VID results in a reduction to the processor power consumption.

A processor enabled for Thermal Monitor 2 includes two operating points, each consisting of a specific operating frequency and voltage, which is identical for both processor cores. The first operating point represents the normal operating condition for the processor. Under this condition, the core-frequency-to-system-bus multiplier used by the processor is that contained in the CLOCK_FLEX_MAX MSR and the VID that is specified in Table 2-3.

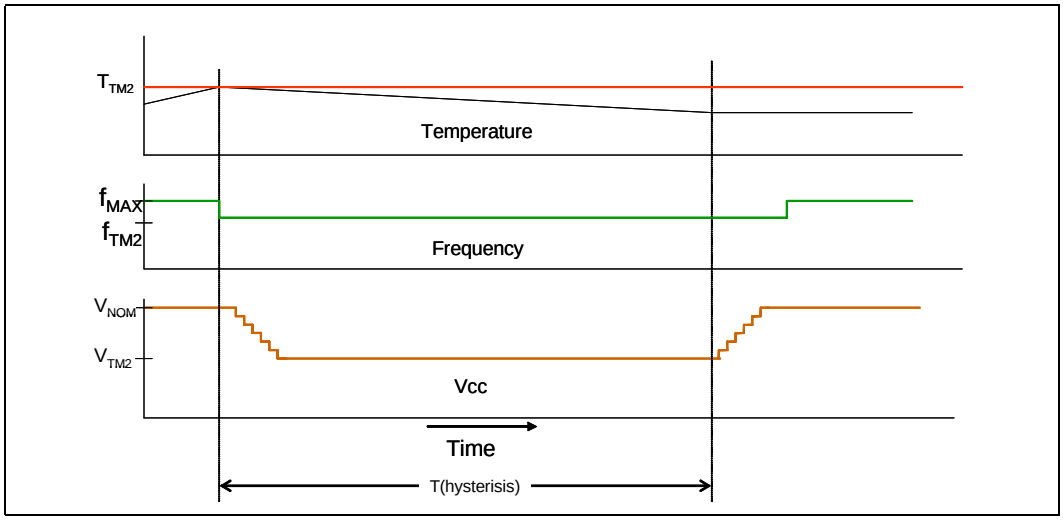
The second operating point consists of both a lower operating frequency and voltage. The lowest operating frequency is determined by the lowest supported bus ratio (1/6 for the processor. When the TCC is activated, the processor automatically transitions to the new frequency. This transition occurs rapidly, on the order of 5 µs. During the frequency transition, the processor is unable to service any bus requests, and consequently, all bus traffic is blocked. Edge-triggered interrupts will be latched and kept pending until the processor resumes operation at the new frequency.

Once the new operating frequency is engaged, the processor will transition to the new core operating voltage by issuing a new VID code to the voltage regulator. The voltage regulator must support dynamic VID steps in order to support Thermal Monitor 2. During the voltage change, it will be necessary to transition through multiple VID codes to reach the target operating voltage. Each step will be one VID table entry (see Table 2-3). The processor continues to execute instructions during the voltage transition. Operation at the lower voltage reduces the power consumption of the processor.

A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the operating frequency and

voltage transition back to the normal system operating point. Transition of the VID code will occur first, in order to insure proper operation once the processor reaches its normal operating frequency. Refer to Figure 5-3 for an illustration of this ordering.

Figure 5-3. Thermal Monitor 2 Frequency and Voltage Ordering



The PROCHOT# signal is asserted when a high temperature situation is detected, regardless of whether Thermal Monitor 1 or Thermal Monitor 2 is enabled.

5.2.2 On-Demand Mode

The processor provides an auxiliary mechanism that allows system software to force the processor to reduce its power consumption. This mechanism is referred to as "On-Demand" mode and is distinct from the Thermal Monitor 1 and Thermal Monitor 2 features. On-Demand mode is intended as a means to reduce system level power consumption. Systems using the processor must not rely on software usage of this mechanism to limit the processor temperature. If bit 4 of the IA32_CLOCK_MODULATION MSR is set to a '1', the processor will immediately reduce its power consumption via modulation (starting and stopping) of the internal core clock, independent of the processor temperature. When using On-Demand mode, the duty cycle of the clock modulation is programmable via bits 3:1 of the same IA32_CLOCK_MODULATION MSR. In On-Demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off to 87.5% on/12.5% off in 12.5% increments. On-Demand mode may be used in conjunction with the Thermal Monitor; however, if the system tries to enable On-Demand mode at the same time the TCC is engaged, the factory configured duty cycle of the TCC will override the duty cycle selected by the On-Demand mode.

5.2.3 PROCHOT# Signal

An external signal, PROCHOT# (processor hot) is asserted when the processor die temperature of any processor cores reaches its factory configured trip point. If Thermal Monitor is enabled (note that Thermal Monitor must be enabled for the processor to be operating within specification), the TCC will be active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT#. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manual* for specific register and programming details.

PROCHOT# is designed to assert at or a few degrees higher than maximum T_{CASE} when dissipating TDP power, and cannot be interpreted as an indication of processor case temperature. This temperature delta accounts for processor package, lifetime and manufacturing variations and attempts to ensure the Thermal Control Circuit is not activated below maximum T_{CASE} when dissipating TDP power. There is no defined or fixed correlation between the PROCHOT# trip temperature, or the case temperature. Thermal solutions must be designed to the processor specifications and cannot be adjusted based on experimental measurements of T_{CASE}, or PROCHOT#.

5.2.4 FORCEPR# Signal

The FORCEPR# (force power reduction) input can be used by the platform to cause the processor to activate the TCC. If the Thermal Monitor is enabled, the TCC will be activated upon the assertion of the FORCEPR# signal. Assertion of the FORCEPR# signal will activate TCC for all processor cores. The TCC will remain active until the system deasserts FORCEPR#. FORCEPR# is an asynchronous input. FORCEPR# can be used to thermally protect other system components. To use the VR as an example, when FORCEPR# is asserted, the TCC circuit in the processor will activate, reducing the current consumption of the processor and the corresponding temperature of the VR.

It should be noted that assertion of FORCEPR# does not automatically assert PROCHOT#. As mentioned previously, the PROCHOT# signal is asserted when a high temperature situation is detected. A minimum pulse width of 500 µs is recommended when FORCEPR# is asserted by the system. Sustained activation of the FORCEPR# signal may cause noticeable platform performance degradation.

5.2.5 THERMTRIP# Signal

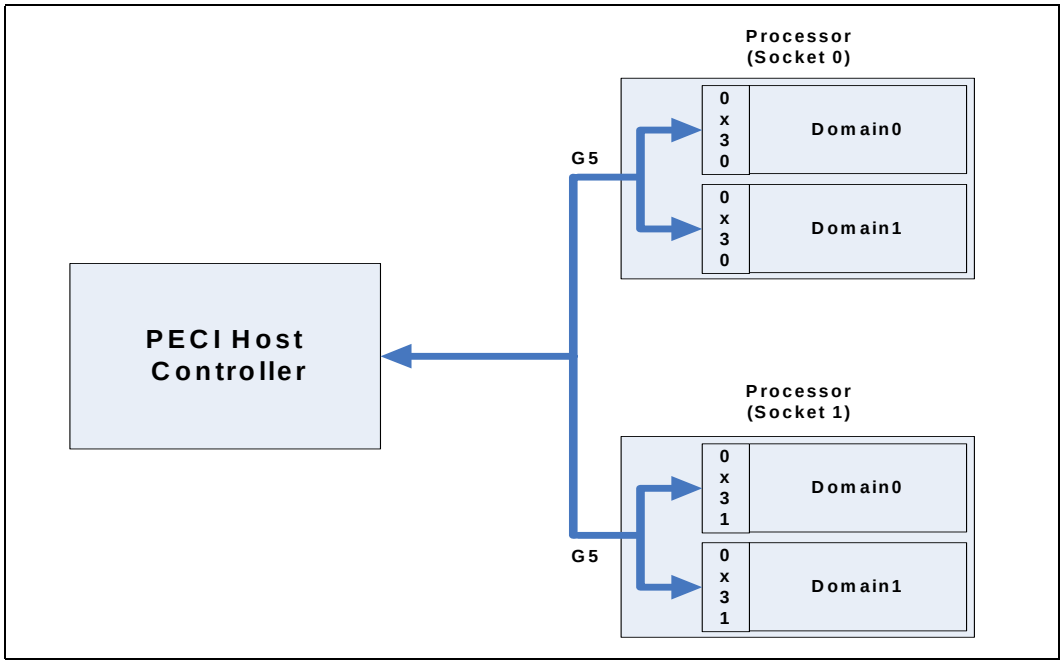
Regardless of whether or not Thermal Monitor 1 or Thermal Monitor 2 is enabled, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached an elevated temperature (refer to the THERMTRIP# definition in Section 4.2). At this point, the FSB signal THERMTRIP# will go active and stay active as described in Section 4.2. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. Intel also recommends the removal of V_{TT}.

5.3 Platform Environment Control Interface (PECI)

5.3.1 Introduction

PECI offers an interface for thermal monitoring of Intel processor and chipset components. It uses a single wire, thus alleviating routing congestion issues. Figure 5-4 shows an example of the PECI topology in a system with the Intel® Core™2 Extreme processor QX9775. PECI uses CRC checking on the host side to ensure reliable transfers between the host and client devices. Also, data transfer speeds across the PECI interface are negotiable within a wide range (2 Kbps to 2 Mbps). The PECI interface on the processor is disabled by default and must be enabled through BIOS.

Figure 5-4. Processor PECI Topology

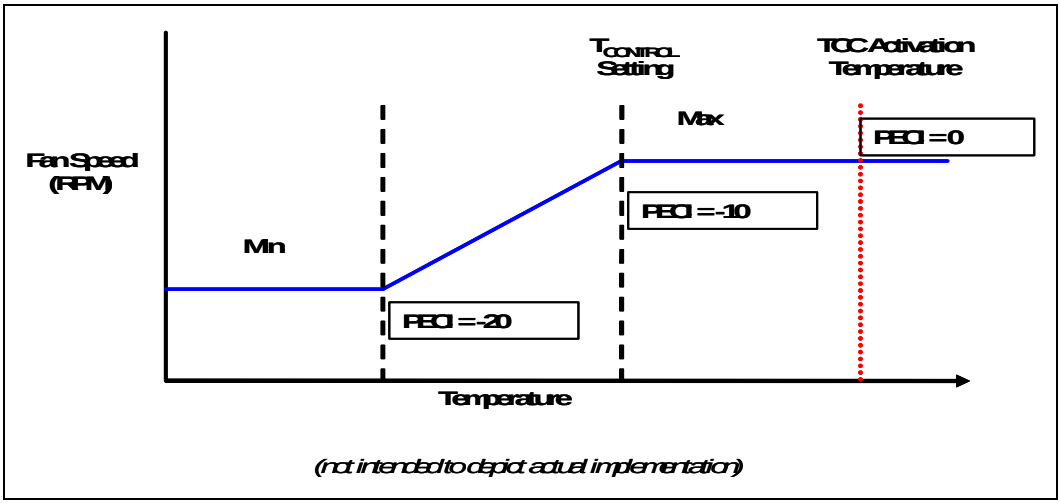


5.3.1.1 $T_{CONTROL}$ and TCC Activation on PECI-based Systems

Fan speed control solutions based on PECI utilize a $T_{CONTROL}$ value stored in the processor IA32_TEMPERATURE_TARGET MSR. The $T_{CONTROL}$ MSR uses the same offset temperature format as PECI though it contains no sign bit. Thermal management devices should infer the $T_{CONTROL}$ value as negative. Thermal management algorithms should use the relative temperature value delivered over PECI in conjunction with the $T_{CONTROL}$ MSR value to control or optimize fan speeds. Figure 5-5 shows a conceptual fan control diagram using PECI temperatures.

The relative temperature value reported over PECI represents the data below the onset of thermal control circuit (TCC) activation as needed by PROCHOT# assertions. As the temperature approaches TCC activation, the PECI value approaches zero. TCC activates at a PECI count of zero.

Figure 5-5. Conceptual Fan Control Diagram of PECI-based Platforms



5.3.1.2 Processor Thermal Data Sample Rate and Filtering

The Digital Thermal Sensor (DTS) provides an improved capability to monitor device hot spots, which inherently leads to more varying temperature readings over short time intervals. The DTS sample interval range can be modified, and a data filtering algorithm can be activated to help moderate this. The DTS sample interval range is 82 us (default) to 20 ms (max). This value can be set in BIOS.

To reduce the sample rate requirements on PECI and improve thermal data stability vs. time the processor DTS also implements an averaging algorithm that filters the incoming data. This is an alpha-beta filter with coefficients of 0.5, and is expressed mathematically as: Current_filtered_temp = (Previous_filtered_temp / 2) + (new_sensor_temp / 2). This filtering algorithm is fixed and cannot be changed. It is on by default and can be turned off in BIOS.

Host controllers should use the min/max sample times to determine the appropriate sample rate based on the controller's fan control algorithm and targeted response rate. The key items to take into account when settling on a fan control algorithm are the DTS sample rate, whether the temperature filter is enabled, how often the PECI host will poll the processor for temperature data, and the rate at which fan speed is changed. Depending on the designer's specific requirements the DTS sample rate and alpha-beta filter may have no effect on the fan control algorithm.

5.3.2 PECI Specifications

5.3.2.1 PECI Device Address

The PECI device address for socket 0 is 30h and socket 1 is 31h. Note that each address also supports two domains (Domain0 and Domain1). For more information on PECI domains, please refer to the *Platform Environment Control Interface (PECI) Specification*.

5.3.2.2 PECI Command Support

PECI command support is covered in detail in *Platform Environment Control Interface Specification.* Refer to this document for details on supported PECI command function and codes.

5.3.2.3 PECI Fault Handling Requirements

PECI is largely a fault tolerant interface, including noise immunity and error checking improvements over other comparable industry standard interfaces. The PECI client is as reliable as the device that it is embedded in, and thus given operating conditions that fall under the specification, the PECI will always respond to requests and the protocol itself can be relied upon to detect any transmission failures. There are, however, certain scenarios where PECI is known to be unresponsive.

Prior to a power on RESET# and during RESET# assertion, PECI is not assured to provide reliable thermal data. System designs should implement a default power-on condition that ensures proper processor operation during the time frame when reliable data is not available via PECI.

To protect platforms from potential operational or safety issues due to an abnormal condition on PECI, the Host controller should take action to protect the system from possible damage. It is recommended that the PECI host controller take appropriate action to protect the client processor device if valid temperature readings have not been obtained in response to three consecutive gettemp()s or for a one second time interval. The host controller may also implement an alert to software in the event of a critical or continuous fault condition.

5.3.2.4 PECI GetTemp0()and GetTemp1() Error Code Support

The error codes supported for the processor GetTemp0() and GetTemp1() commands are listed in Table 5-3.

Table 5-3. GetTemp0() GetTemp1()Error Codes

Error Code	Description
8000h	General sensor error
8002h	Sensor is operational, but has detected a temperature below its operational range (underflow).

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6 Features

6.1 Power-On Configuration Options

Several configuration options can be configured by hardware. The processor samples its hardware configuration at reset, on the active-to-inactive transition of RESET#. For specifics on these options, refer to Table 6-1.

The sampled information configures the processor for subsequent operation. These configuration options cannot be changed except by another reset. All external resets reconfigure the processor, for configuration purposes, the processor does not distinguish between a “warm” reset (PWRGOOD signal remains asserted) and a “power-on” reset.

Table 6-1. Power-On Configuration Option Lands

Configuration Option	Land Name	Notes
Output tri state	SMI#	1,2
Execute BIST (Built-In Self Test)	A3#	1,2
Disable MCERR# observation	A9#	1,2
Disable BINIT# observation	A10#	1,2
Symmetric agent arbitration ID	BR[1:0]#	1,2

NOTES:

1. Asserting this signal during RESET# will select the corresponding option.
2. Address lands not identified in this table as configuration options should not be asserted during RESET#.

Disabling of any of the cores within the processor must be handled by configuring the EXT_CONFIG Model Specific Register (MSR). This MSR will allow for the disabling of a single core per die within the package.

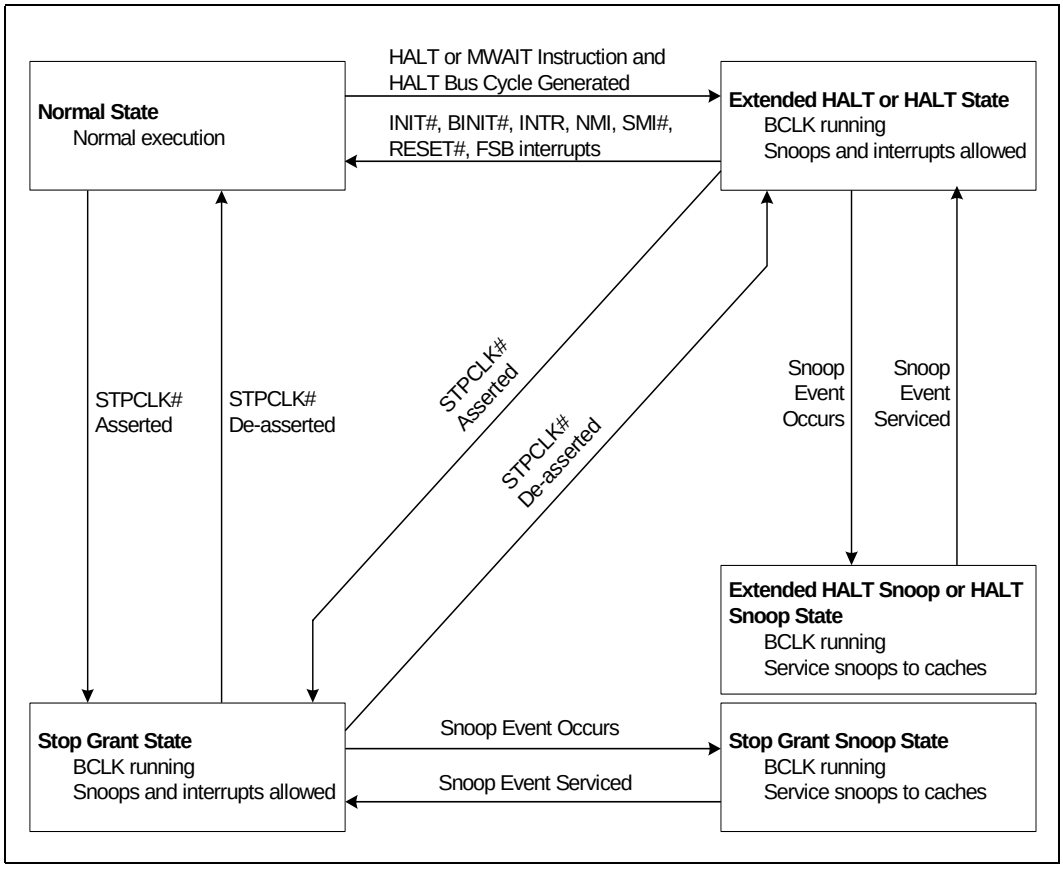
6.2 Clock Control and Low Power States

The processor supports the Extended HALT state (also referred to as C1E) in addition to the HALT state and Stop-Grant state to reduce power consumption by stopping the clock to internal sections of the processor, depending on each particular state. See Figure 6-1 for a visual representation of the processor low power states. The Extended HALT state is a lower power state than the HALT state or Stop Grant state.

The Extended HALT state must be enabled via the BIOS for the processor to remain within its specifications. For processors that are already running at the lowest bus to core frequency ratio for its nominal operating point, the processor will transition to the HALT state instead of the Extended HALT state.

The Stop Grant state requires chipset and BIOS support on multiprocessor systems. In a multiprocessor system, all the STPCLK# signals are bussed together, thus all processors are affected in unison. When the STPCLK# signal is asserted, the processor enters the Stop Grant state, issuing a Stop Grant Special Bus Cycle (SBC) for each processor die. The chipset needs to account for a variable number of processors asserting the Stop Grant SBC on the bus before allowing the processor to be transitioned into one of the lower processor power states.

Figure 6-1. Stop Clock State Machine



6.2.1 Normal State

This is the normal operating state for the processor.

6.2.2 HALT or Extended HALT State

The Extended HALT state (C1E) is enabled via the BIOS. **The Extended HALT state must be enabled for the processor to remain within its specifications.** The Extended HALT state requires support for dynamic VID transitions in the platform.

6.2.2.1 HALT State

HALT is a low power state entered when the processor have executed the HALT or MWAIT instruction. When one of the processor cores execute the HALT or MWAIT instruction, that processor core is halted; however, the other processor continues normal operation. The processor will transition to the Normal state upon the occurrence of SMI#, BINIT#, INIT#, LINT[1:0] (NMI, INTR), or an interrupt delivered over the front side bus. RESET# will cause the processor to immediately initialize itself.

The return from a System Management Interrupt (SMI) handler can be to either Normal Mode or the HALT state. See the *Intel® 64 and IA-32 Architecture Software Developer's Manual*.

The system can generate a STPCLK# while the processor is in the HALT state. When the system deasserts STPCLK#, the processor will return execution to the HALT state.

While in HALT state, the processor will process front side bus snoops and interrupts.

6.2.2.2 Extended HALT State

Extended HALT state is a low power state entered when all processor cores have executed the HALT or MWAIT instructions and Extended HALT state has been enabled via the BIOS. When one of the processor cores executes the HALT instruction, that processor core is halted; however, the other processor core continues normal operation. The Extended HALT state is a lower power state than the HALT state or Stop Grant state. The Extended HALT state must be enabled for the processor to remain within its specifications.

The processor will automatically transition to a lower core frequency and voltage operating point before entering the Extended HALT state. Note that the processor FSB frequency is not altered; only the internal core frequency is changed. When entering the low power state, the processor will first switch to the lower bus to core frequency ratio and then transition to the lower voltage (VID).

While in the Extended HALT state, the processor will process bus snoops.

Table 6-2. Extended HALT Maximum Power

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$P_{EXTENDED\_HALT}$	Extended HALT State Power	—	—	16	W	1,2

NOTE:
1. The specification is at Tcase = 40 °C and nominal Vcc. The VID setting represents the maximum expected VID when running in HALT state.
2. Processors running in the lowest bus ratio supported as shown in Table 2-1, will enter the HALT State when the processor has executed the HALT or MWAIT instruction since the processor is already operating in the lowest core frequency and voltage operating point.

The processor exits the Extended HALT state when a break event occurs. When the processor exits the Extended HALT state, it will first transition the VID to the original value and then change the bus to core frequency ratio back to the original value.

6.2.3 Stop-Grant State

When the STPCLK# pin is asserted, the Stop-Grant state of the processor is entered no later than 20 bus clocks after the response phase of the processor issued Stop Grant Acknowledge special bus cycle. By default, the processor will issue two Stop Grant Acknowledge special bus cycles, one for each die. Once the STPCLK# pin has been asserted, it may only be deasserted once the processor is in the Stop Grant state. All processor cores will enter the Stop-Grant state once the STPCLK# pin is asserted. Additionally, all processor cores must be in the Stop Grant state before the de-assertion of STPCLK#.

Since the AGTL+ signal pins receive power from the front side bus, these pins should not be driven (allowing the level to return to V_{TT}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the front side bus should be driven to the inactive state.

BINIT# will not be serviced while the processor is in Stop-Grant state. The event will be latched and can be serviced by software upon exit from the Stop Grant state.

RESET# will cause the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. A transition back to the Normal state will occur with the de-assertion of the STPCLK# signal.

A transition to the Grant Snoop state will occur when the processor detects a snoop on the front side bus (see Section 6.2.4.1).

While in the Stop-Grant state, SMI#, INIT#, BINIT# and LINT[1:0] will be latched by the processor, and only serviced when the processor returns to the Normal state. Only one occurrence of each event will be recognized upon return to the Normal state.

While in Stop-Grant state, the processor will process snoops on the front side bus and it will latch interrupts delivered on the front side bus.

The PBE# signal can be driven when the processor is in Stop-Grant state. PBE# will be asserted if there is any pending interrupt latched within the processor. Pending interrupts that are blocked by the EFLAGS.IF bit being clear will still cause assertion of PBE#. Assertion of PBE# indicates to system logic that it should return the processor to the Normal state.

6.2.4 Extended HALT Snoop or HALT Snoop State, Stop Grant Snoop State

The Extended HALT Snoop state is used in conjunction with the Extended HALT state. If the Extended HALT state is not enabled in the BIOS, the default Snoop state entered will be the HALT Snoop state. Refer to the sections below for details on HALT Snoop state, Stop Grant Snoop state, and Extended HALT Snoop state.

6.2.4.1 HALT Snoop State, Stop Grant Snoop State

The processor will respond to snoop or interrupt transactions on the front side bus while in Stop-Grant state or in HALT state. During a snoop or interrupt transaction, the processor enters the HALT/Grant Snoop state. The processor will stay in this state until the snoop on the front side bus has been serviced (whether by the processor or another agent on the front side bus) or the interrupt has been latched. After the snoop is serviced or the interrupt is latched, the processor will return to the Stop-Grant state or HALT state, as appropriate.

6.2.4.2 Extended HALT Snoop State

The Extended HALT Snoop state is the default Snoop state when the Extended HALT state is enabled via the BIOS. The processor will remain in the lower bus to core frequency ratio and VID operating point of the Extended HALT state.

While in the Extended HALT Snoop state, snoops and interrupt transactions are handled the same way as in the HALT Snoop state. After the snoop is serviced or the interrupt is latched, the processor will return to the Extended HALT state.

6.3 Enhanced Intel SpeedStep® Technology

The processor supports Enhanced Intel SpeedStep® Technology. This technology enables the processor to switch between multiple frequency and voltage points, which results in platform power savings. Enhanced Intel SpeedStep Technology requires support for dynamic VID transitions in the platform. Switching between voltage/frequency states is software controlled. For more configuration details also refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manual*.

Enhanced Intel SpeedStep Technology creates processor performance states (P-states) or voltage/frequency operating points which are lower power capability states within the Normal state (see Figure 6-1 for the Stop Clock State Machine for supported P-states). Enhanced Intel SpeedStep Technology enables real-time dynamic switching between frequency and voltage points. It alters the performance of the processor by changing the bus to core frequency ratio and voltage. This allows the processor to run at different core frequencies and voltages to best serve the performance and power requirements of the processor and system. The processor has hardware logic that coordinates the requested voltage (VID) between the processor cores. The highest voltage that is requested for either of the processor cores is selected for that processor package. Note that the front side bus is not altered; only the internal core frequency is changed. In order to run at reduced power consumption, the voltage is altered in step with the bus ratio.

The following are key features of Enhanced Intel SpeedStep Technology:

- Multiple voltage/frequency operating points provide optimal performance at reduced power consumption.
- Voltage/frequency selection is software controlled by writing to the processor MSR's (Model Specific Registers); thus, eliminating chipset dependency.
  - If the target frequency is higher than the current frequency, V_{CC} is incremented in steps (+12.5 mV) by placing a new value on the VID signals and the processor shifts to the new frequency. Note that the top frequency for the processor can not be exceeded.
  - If the target frequency is lower than the current frequency, the processor shifts to the new frequency and V_{CC} is then decremented in steps (-12.5 mV) by changing the target VID through the VID signals.

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