Green-Mode PWM Controller with Integrated Protections

Rev. 01a

General Description

The LD7552B are low cost, low startup current, current mode PWM controllers with green-mode power- saving operation. The integrated functions include the leading-edge blanking of the current sensing, internal slope compensation. They provide the users a superior AC/DC power application of higher efficiency, low external component counts, and lower cost solution.

Furthermore, LD7552B feature more protections like OLP (Over Load Protection) and OVP (Over Voltage Protection) to eliminate the external protection circuits. It is designed for the switching adaptor with 30W~60W output, offered in both SOP-8 and DIP-8 package.

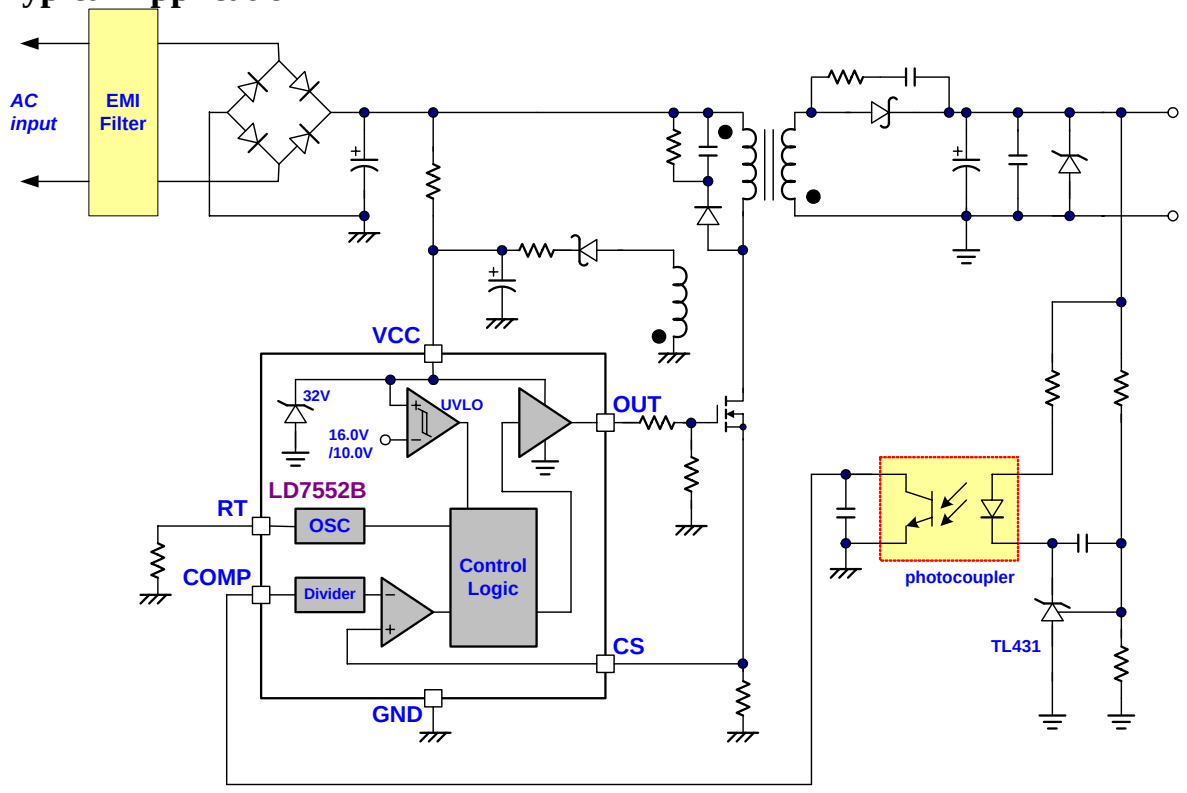
Features

- High-Voltage CMOS Process with Excellent ESD protection
- Very Low Startup Current (<20μA)
- Current Mode Control
- Non-audible-noise Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- Programmable Switching Frequency
- Internal Slope Compensation
- OVP (Over Voltage Protection) on Vcc Pin
- OLP (Over Load Protection)
- 500mA Driving Capability

Applications

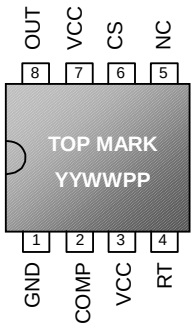
- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply
- 384X Replacement

Typical Application



Pin Configuration

SOP-8 & DIP-8 (TOP VIEW)



YY: Year code (D: 2004, E: 2005…..)
WW: week code
PP: production code

Ordering Information

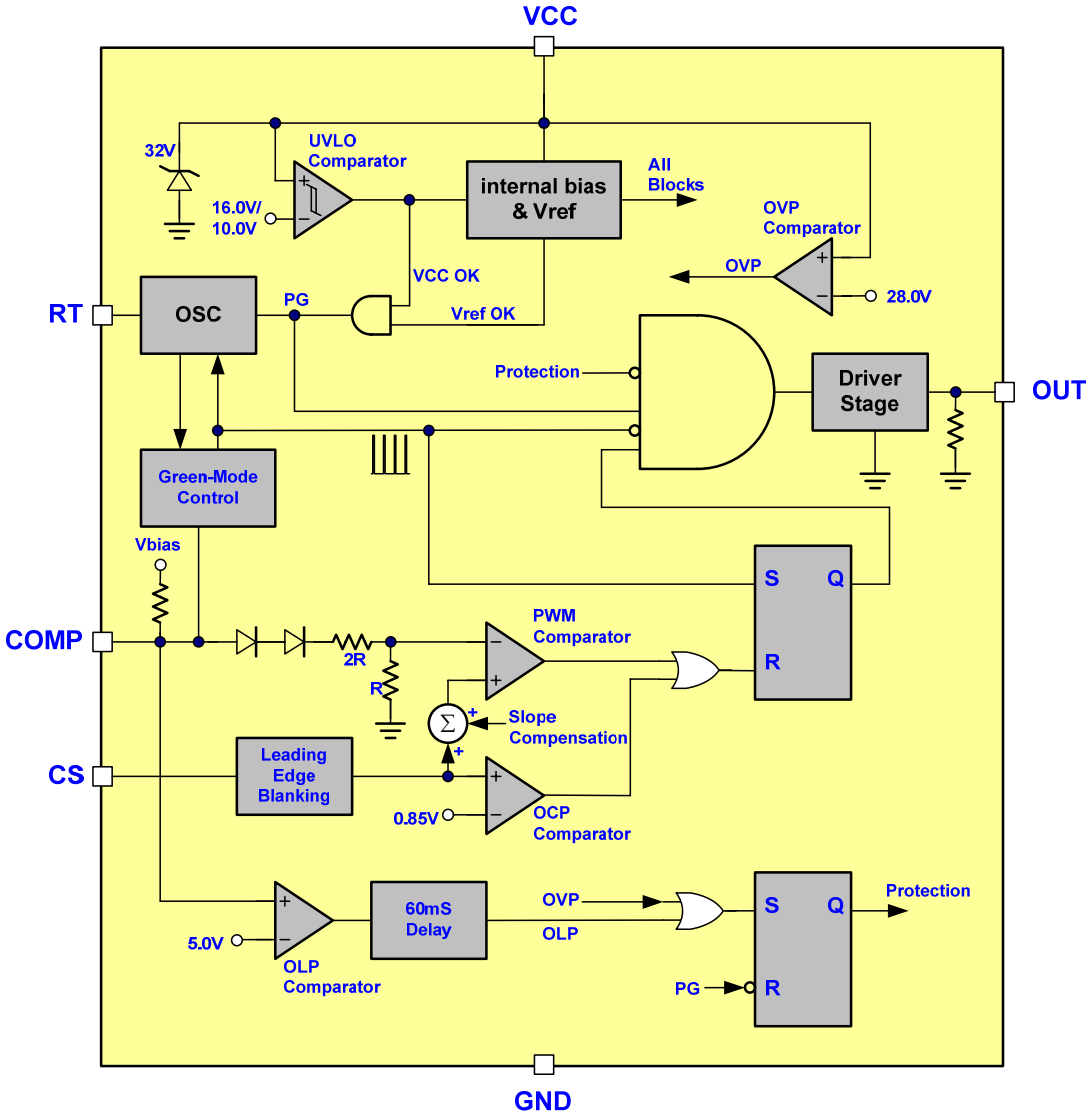
Part number	Package		TOP MARK	Shipping
LD7552B PS	SOP-8	PB Free	LD7552BPS	2500 /tape & reel
LD7552B GS	SOP-8	Green Package	LD7552BGS	2500 /tape & reel
LD7552B PN	DIP-8	PB Free	LD7552BPN	3600 /tube /carton

The LD7552B is ROHS Compliant/ Green Package.

Pin Descriptions

PIN	NAME	FUNCTION
1	GND	Ground
2	COMP	Voltage feedback pin (same as the COMP pin in UC384X), By connecting a photo-coupler to close the control loop and achieve the regulation.
3	VCC	Supply voltage pin
4	RT	This pin is to program the switching frequency. By connecting a resistor to ground to set the switching frequency.
5	NC	Unconnected pin
6	CS	Current sense pin, connect to sense the MOSFET current
7	VCC	Supply voltage pin
8	OUT	Gate drive output to drive the external MOSFET

Block Diagram



* *Note: OLP delay is 60mS when the switching frequency is set as 65KHz.*

The OLP delay time is proportional to the period of switching cycle.

That is, $T_{OLP\_delay} \propto T_s = \frac{1}{f_s}$.

Absolute Maximum Ratings

Supply Voltage VCC	30V
COMP, RT, CS	-0.3 ~7V
Junction Temperature	150°C
Operating Ambient Temperature	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-8)	160°C/W
Package Thermal Resistance (DIP-8)	100°C/W
Power Dissipation (SOP-8, at Ambient Temperature = 85°C)	400mW
Power Dissipation (DIP-8, at Ambient Temperature = 85°C)	650mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model	3KV
ESD Voltage Protection, Machine Model	300V
Gate Output Current	500mA

Caution:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (Vcc Pin)					
Startup Current			8	20	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V		2.0	3.0	mA
	V_{COMP}=3V		2.5		mA
	Protection tripped (OLP, OVP)		0.5		mA
UVLO (Off)		9.0	10.0	11.0	V
UVLO (On)		15.0	16.0	17.0	V
OVP Level		26.5	28.0	29.5	V
Voltage Feedback (Comp Pin)					
Short Circuit Current	V_{COMP}=0V		1.5	2.2	mA
Open Loop Voltage	COMP pin open		6.0		V
Green Mode Threshold VCOMP			2.35		V
Current Sensing (CS Pin)					
Maximum Input Voltage, Vcs(off)		0.80	0.85	0.90	V
Leading Edge Blanking Time			350		nS
Input impedance		1			MΩ
Delay to Output			100		nS
Oscillator (RT pin)					
Frequency	RT=100KΩ	60	65	70	KHz
Green Mode Frequency	Fs=65KHz		20		KHz
Temp. Stability	(-40°C ~105°C)		5		%
Voltage Stability	(VCC=11V-25V)			1	%
Gate Drive Output (OUT Pin)					
Output Low Level	VCC=15V, Io=20mA			1	V
Output High Level	VCC=15V, Io=20mA	9			V
Rising Time	Load Capacitance=1000pF		50	160	nS
Falling Time	Load Capacitance=1000pF		30	60	nS
OLP (Over Load Protection)					
OLP Trip Level	V_{COMP}(OLP)		5.0		V
OLP Delay Time (note)	Fs=65KHz		60		mS

Note: The OLP delay time is proportional to the period of switching cycle. So that, the lower RT value will set the higher switching frequency and the shorter OLP delay time.

Typical Performance Characteristics

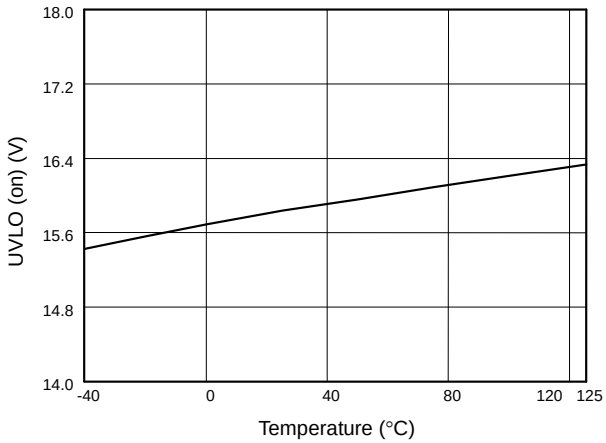


Fig. 1 UVLO (on) vs. Temperature

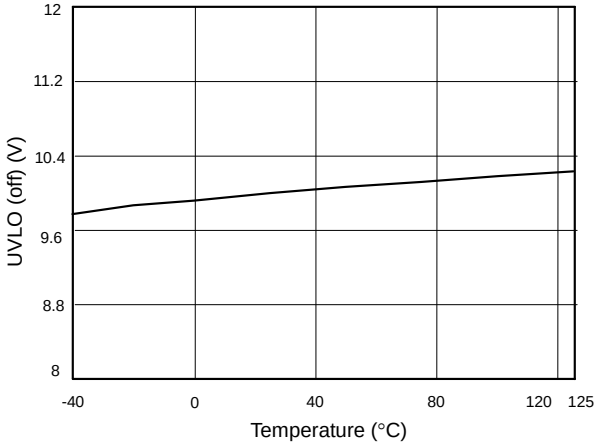


Fig. 2 UVLO (off) vs. Temperature

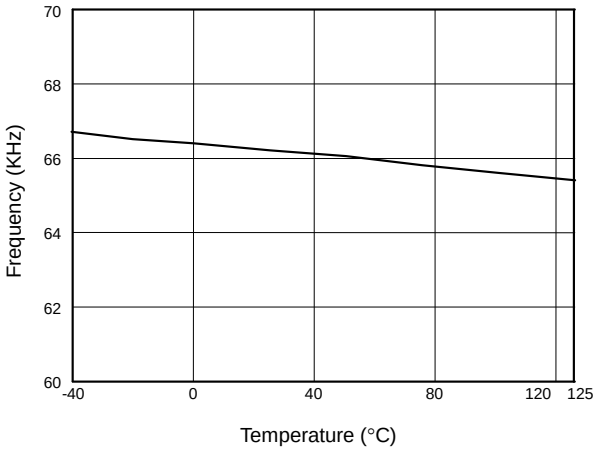


Fig. 3 Frequency vs. Temperature

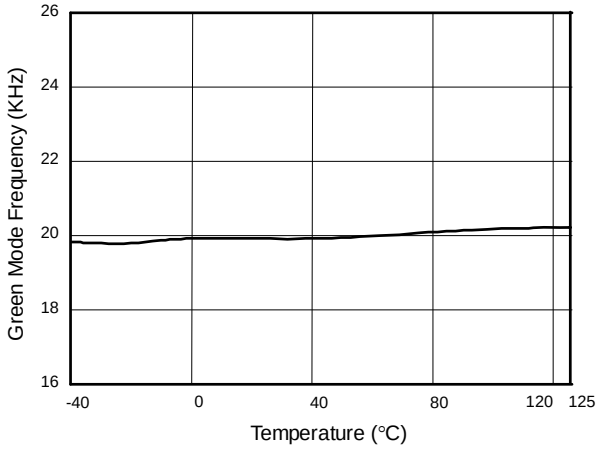


Fig. 4 Green Mode Frequency vs. Temperature

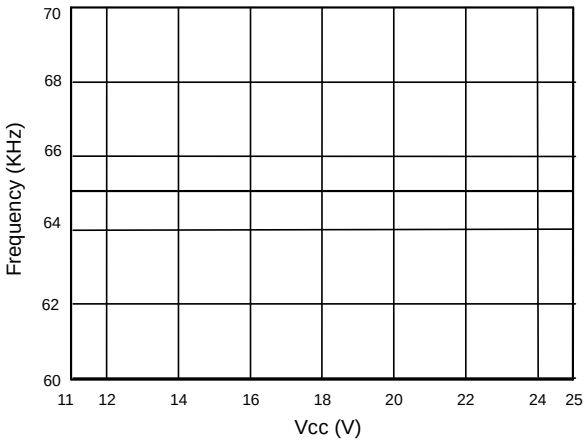


Fig. 5 Frequency vs. Vcc

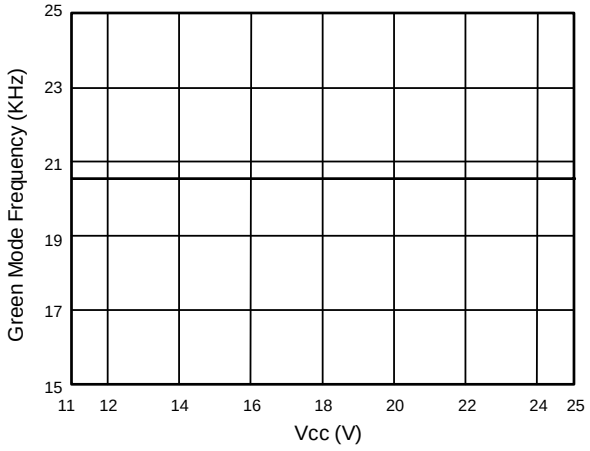


Fig. 6 Green Mode Frequency vs. Vcc

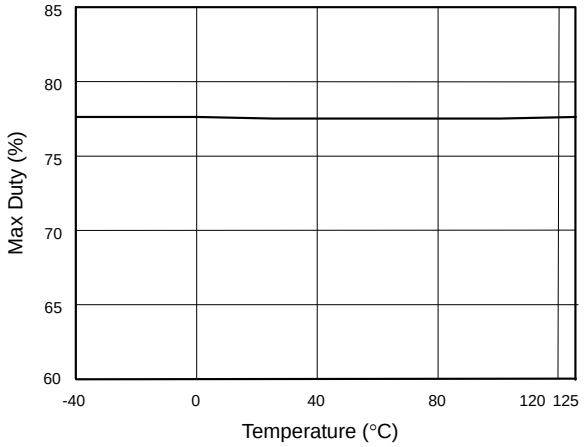


Fig. 7 Max Duty vs. Temperature

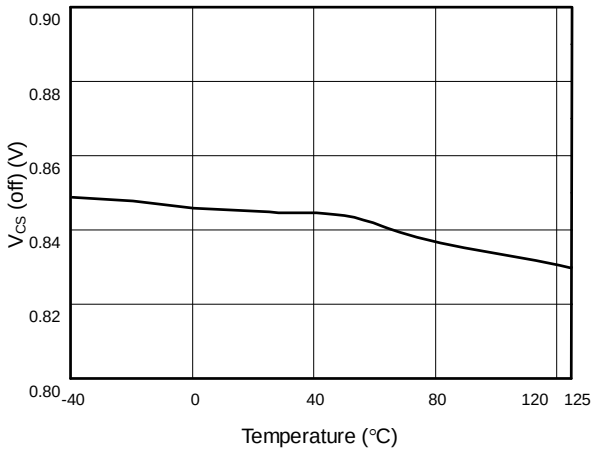


Fig. 8 V_{CS} (off) vs. Temperature

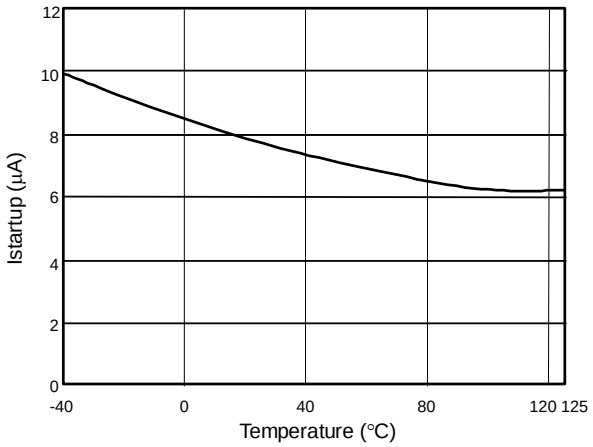


Fig. 9 Startup Current (Istartup) vs. Temperature

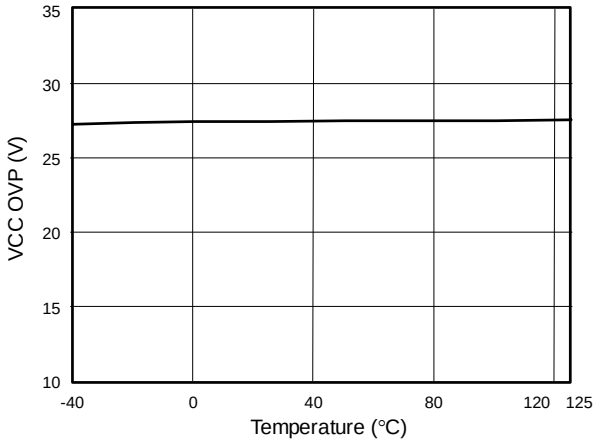


Fig. 10 VCC OVP vs. Temperature

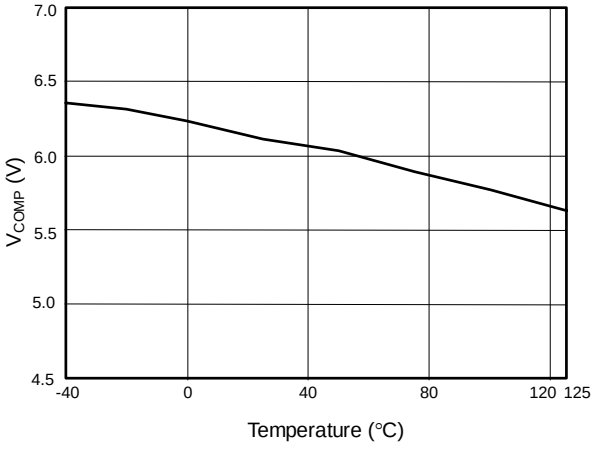


Fig. 11 V_{COMP} open loop voltage vs. Temperature

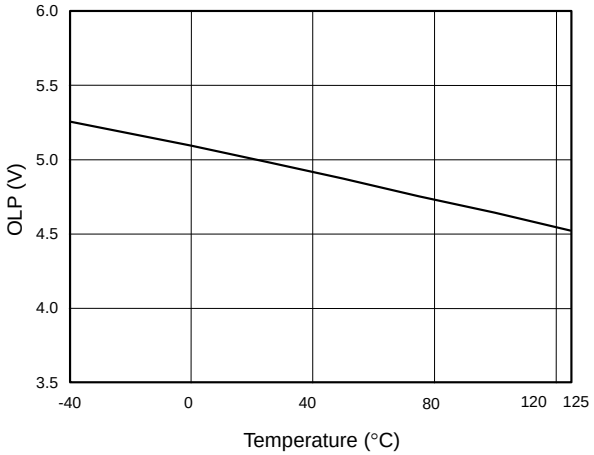


Fig. 12 OLP-Trip Level vs. Temperature

Application Information

Operation Overview

The LD7552B meet the green-power requirement and are intended for the use in those modern switching power suppliers and adaptors that demand higher power efficiency and power-saving. They integrated more functions to reduce the external component counts and the size. Their major features are described as below.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage on the VCC pin. It would assure the supply voltage enough to turn on the LD7552B PWM controller and further to drive the power MOSFET. As shown in Fig. 13, a hysteresis is built in to prevent the shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16.0V and 10.0V, respectively.

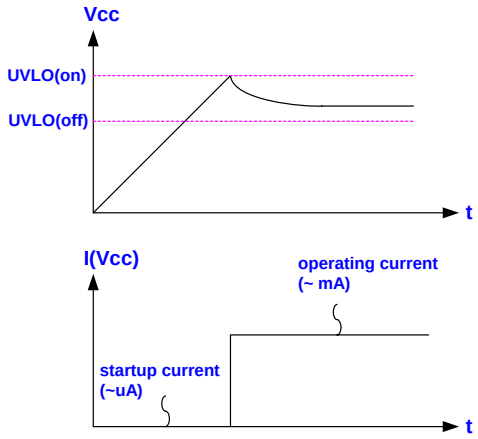


Fig. 13

Startup Current and Startup Circuit

The typical startup circuit to generate the LD7552B Vcc is shown in Fig. 14. During the startup transient, the Vcc is lower than the UVLO threshold thus there is no gate pulse produced from LD7552B to drive power MOSFET. Therefore, the current through R1 will provide the startup current and to charge the capacitor C1. Whenever the Vcc voltage is high enough to turn on the LD7552B and further to deliver the gate drive signal, the supply current is provided from the auxiliary winding of the transformer. Lower startup current requirement on the PWM controller will help to increase the value of R1 and then reduce the power consumption on R1. By using CMOS process and the special circuit design, the maximum startup current of LD7552B is only 20μA.

If a higher resistance value of the R1 is chosen, it usually takes more time to start up. To carefully select the value of R1 and C1 will optimize the power consumption and startup time.

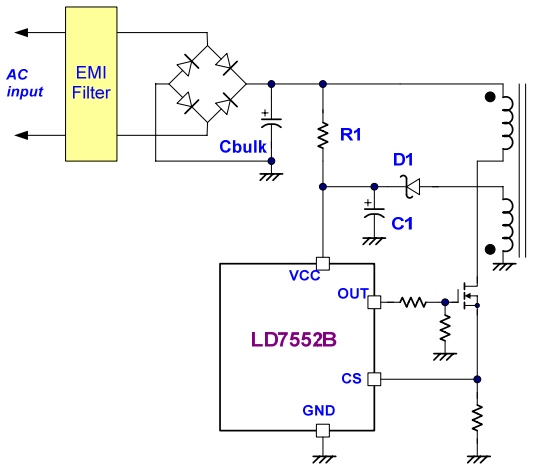


Fig. 14

Current Sensing and Leading-edge Blanking

The typical current mode of PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. As shown in Fig. 15, the LD7552B detect the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.85V. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{0.85V}{R_S}$$

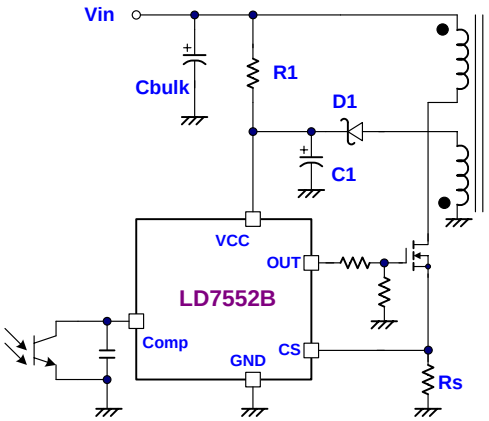


Fig. 15

A 350nS leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. In the low power application, if the total pulse width of the turn-on spikes is less than 350nS and the negative spike on the CS pin doesn't exceed -0.3V, it could eliminated the R-C filter (as shown in the figure16).

However, the total pulse width of the turn-on spike is decided by the output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller R-C filter (as shown in figure 17) for higher power application to avoid the CS pin being damaged by the negative turn-on spike.

Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer, with typical 500mA driving capability, is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of LD7552B is limited to 75% to avoid the transformer saturation.

Oscillator and Switching Frequency

Connect a resistor from RT pin to GND according to the equation below to program the normal switching frequency:

$$f_{SW} = \frac{65.0}{RT_{(K\Omega)}} \times 100(KHz)$$

The operating frequency range for the LD7552B is recommended to set between 50KHz and 130KHz.

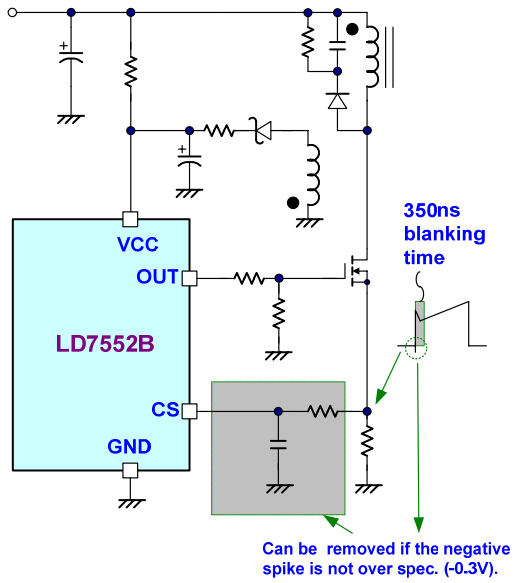


Fig. 16

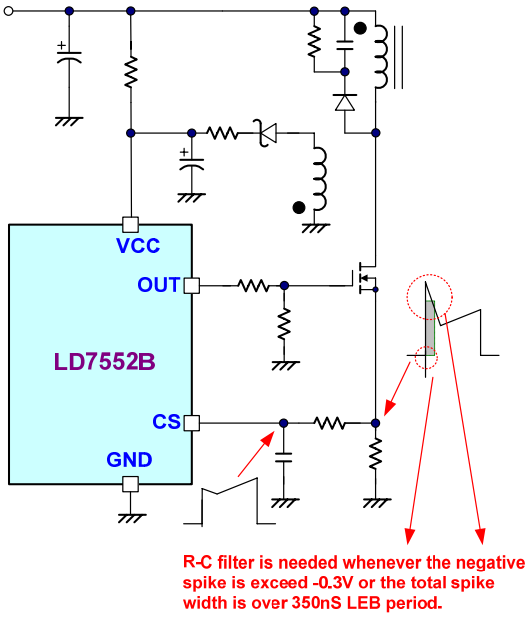


Fig. 17

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 at the secondary side through the photo-coupler to the COMP pin of the LD7552B. Similar to UC384X, the LD7552B would carry 2 diodes voltage offset at the stage to feed the voltage divider at the ratio of 1/3, that is,

$$V_{-(PWM_{COMPARATOR})} = \frac{1}{3} \times (V_{COMP} - 2V_F)$$

A pull-high resistor is embedded internally and can be eliminated externally.

Internal Slope Compensation

In the conventional application, the problem of the stability is a critical issue for current mode controlling, when it operates in higher than 50% of the duty-cycle. As UC384X, It takes slope compensation from injecting the ramp signal of the RT/CT pin through a coupling capacitor. It therefore requires no extra design for the LD7552B since it has integrated it already.

On/Off Control

The LD7552B can be turned off by pulling COMP pin lower than 1.2V. The gate output pin of the LD7552B will be disabled immediately under such condition. The off-mode can be released when the pull-low signal is removed.

Dual-Oscillator Green-Mode Operation

There are many different topologies has been implemented in different chips for the green-mode or power saving requirements such as “burst-mode control”, “skipping-cycle mode”, “variable off-time control “…etc. The basic operation theory of all these approaches intended to reduce the switching cycles under light-load or no-load condition either by skipping some switching pulses or reduces the switching frequency.

OVP (Over Voltage Protection) on Vcc

The V_{GS} ratings of the nowadays power MOSFETs are often limited up to max. 30V. To prevent the V_{GS} from the fault condition, LD7552B are implemented an OVP function on Vcc. Whenever the Vcc voltage is higher than the OVP threshold voltage, the output gate drive circuit will be shutdown simultaneously thus to stop the switching of the power MOSFET until the next UVLO(on).

The Vcc OVP function in LD7552B is an auto-recovery type protection. If the OVP condition, usually caused by the feedback loop opened, is not released, the Vcc will tripped the OVP level again and re-shutdown the output. The Vcc is working as a hiccup mode. The figure 18 shows its operation.

On the other hand, if the OVP condition is removed, the Vcc level will get back to normal level and the output will automatically return to the normal operation.

The OVP levels are 28.0V ± 1.5V.

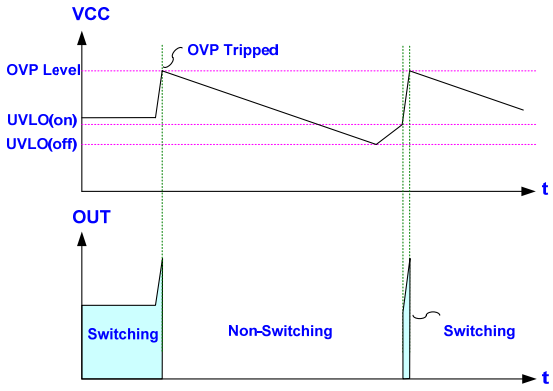


Fig. 18

Over Load Protection (OLP)

To protect the circuit from being damaged under over load condition or short condition, a smart OLP function is implemented in the LD7552B. The figure 19 shows the waveforms of the OLP operation. In this case, the feedback system will force the voltage loop proceed toward the saturation and then pull up the voltage on COMP pin (V_{COMP}). Whenever the V_{COMP} trips up to the OLP threshold 5V and stays longer than 60mS, the protection will activate and then turn off the gate output to stop the switching of power circuit. The 60mS delay time is to prevent the false trigger from the power-on and turn-off transient.

By such protection mechanism, the average input power can be reduced to very low level so that the component temperature and stress can be controlled within the safe operating area.

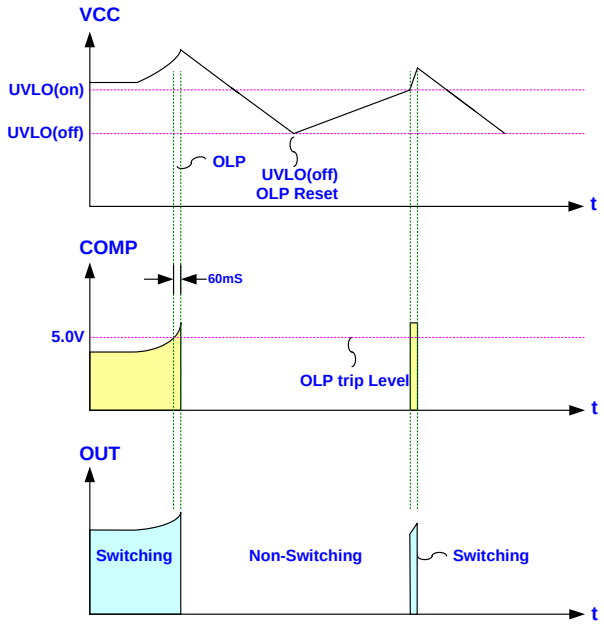


Fig. 19

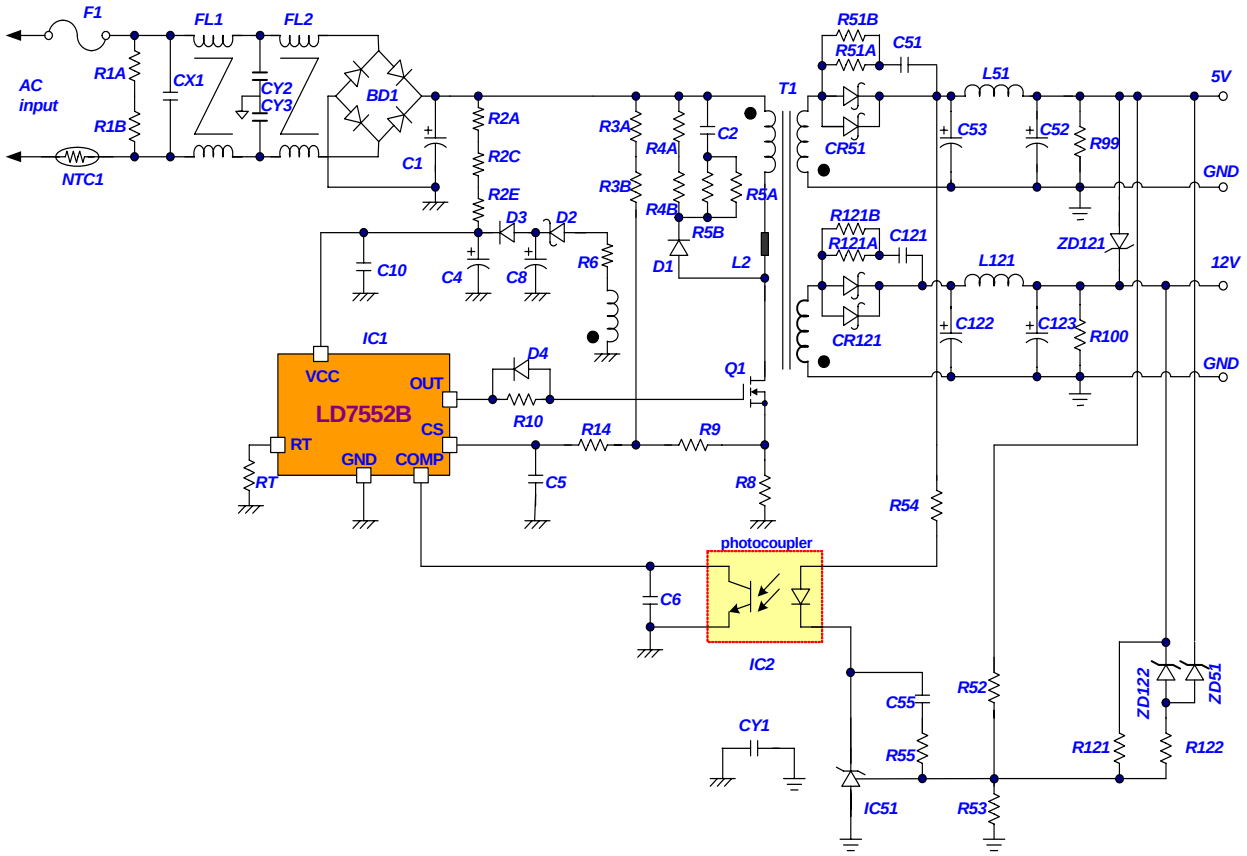
Fault Protection

There are several critical protections were integrated in the LD7552B to prevent the power supply or adapter from being damaged. Those damages usually come from open or short condition on the pins of LD7552B. Under the conditions listed below, the gate output will turn off immediately to protect the power circuit ---

- RT pin short to ground
- RT pin floating
- CS pin floating

Reference Application Circuit #1 --- 40W (5V/2A & 12V/2.5A) Adapter with 2-Stage Startup Circuit

Pin < 0.3W when Pout = 0W



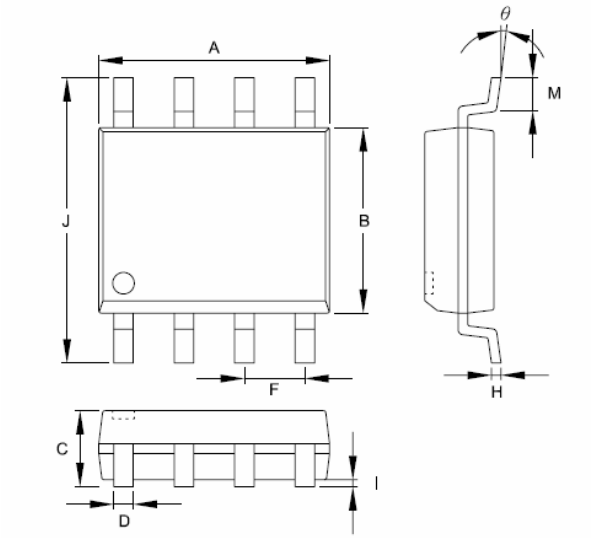
BOM

P/N	Component Value	Original
R1A	1MΩ, 1206	
R1B	1MΩ, 1206	
R2A	510KΩ, 1206	
R2C	510KΩ, 1206	
R3A	1MΩ, 1206	Open
R3B	1MΩ, 1206	Open
R4A	100KΩ, 1206	
R4B	100KΩ, 1206	
R5A	100Ω, 1206	
R5B	100Ω, 1206	
R6	10Ω, 1206	
R8	0.47Ω, 1W	
R9	1.5KΩ, 0805	
R10	10Ω, 1206	
R14	0Ω, 0805	
RT	100KΩ, 0805,1%	
R51A	100Ω, 1206	
R51B	100Ω, 1206	
R121A	100Ω, 1206	
R121B	100Ω, 1206	
R52	3.6KΩ, 0805, 1%	
R53	2.49KΩ, 0805, 1%	
R54	200Ω, 0805	
R55	1KΩ, 0805	
R99A	N/A	
R99B	N/A	
R100A	N/A	
R100B	N/A	
R121	33KΩ, 0805	
R122	1KΩ, 0805	
FL1	Leadtrend's Design	
FL2	Leadtrend's Design	
T1	Leadtrend's Design	
L2	Bead Core	
L51	Leadtrend's Design	
L121	Leadtrend's Design	

P/N	Component Value	Note
C1	100μF, 400V	L-tec
C2	1000pF, 1000V, 1206	X7R
C4	10μF, 50V	L-tec (LZG)
C5	100pF, 50V, 0805	X7R
C6	0.022μF, 50V, 0805	X7R
C8	33μF, 50V	L-tec (LZG)
C10	0.1μF, 50V, 0805	X7R
C51	1000pF, 250V, 1206	
C52	470μF, 16V	L-tec (LZG)
C53	1000μF, 25V	L-tec (LZG)
C55	0.01μF, 50V, 0805	X7R
C121	1000pF, 250V, 1206	
C122	1000μF, 25V	L-tec (LZG)
C123	470μF, 16V	L-tec (LZG)
CX1	0.22μF,X-cap	
CY1	2200pF,Y-cap, class2	
CY2	2200pF,Y-cap, class2	
CY3	2200pF,Y-cap, class2	
D1	1N4007	
D2	PS102R	
D3	1N4148	
D4	1N4148	
ZD51	5V1B	
ZD121	7.5V, 1W	
ZD122	15V	
Q1	6A, 600V	SSS6N60A
BD1	2A, 600V	2KBP06M
CR51	10A, 100V	Y1010DN
CR121	10A, 60V	SBL1060CF
IC1	LD7552B	Leadtrend
IC2	EL817B	EVERLIGHT
IC51	TL431, 1%	
F1	250V,T2A	Walter

Package Information

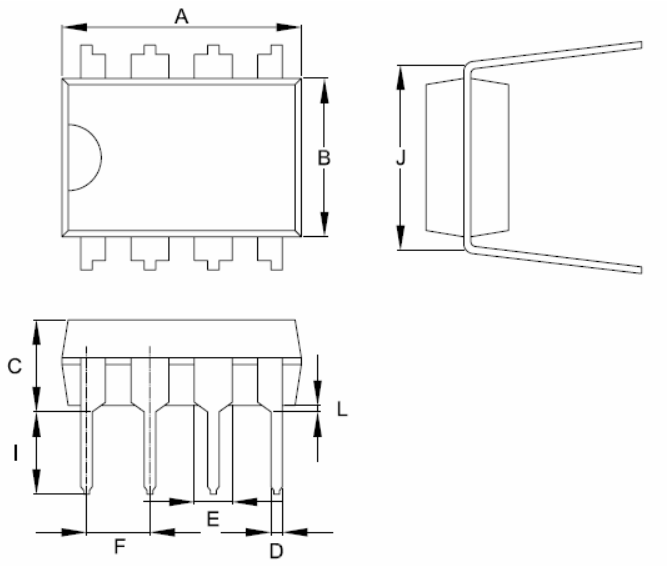
SOP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	4.801	5.004	5.004	0.197
B	3.810	3.988	3.988	0.157
C	1.346	1.753	1.753	0.069
D	0.330	0.508	0.508	0.020
F	1.194	1.346	1.346	0.053
H	0.178	0.229	0.229	0.009
I	0.102	0.254	0.254	0.010
J	5.791	6.198	6.198	0.244
M	0.406	1.270	1.270	0.050
θ	0°	8°	0°	8°

Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	---	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.290	0.325
L	0.381	---	0.015	---

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	09/20/2006	Original Specification.
01	01/29/2007	Revision: Block Diagram
01a	1/2/2008	Revision: Green Package Option