REALTEK

RTL8111B

INTEGRATED GIGABIT ETHERNET CONTROLLER
FOR PCI EXPRESS™ APPLICATIONS

DATASHEET

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2005/01/17	First release.
1.1	2005/03/24	Changed Table 8, Power & Ground, page 6. Added lead (Pb)-free package identification information on page 3 and on page 27.

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1.   General Description

The Realtek RTL8111B Gigabit Ethernet controller combines a triple-speed IEEE 802.3 compliant Media Access Controller (MAC) with a triple-speed Ethernet transceiver, PCI Express bus controller, and embedded memory. With state-of-the-art DSP technology and mixed-mode signal technology, the RTL8111B offers high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capability at high speeds.

The device supports the PCI Express 1.0a bus interface for host communications with power management and is compliant with the IEEE 802.3u specification for 10/100Mbps Ethernet and the IEEE 802.3ab specification for 1000Mbps Ethernet. It also supports an auxiliary power auto-detect function, and will auto-configure related bits of the PCI power management registers in PCI configuration space.

The RTL8111B supports the attachment of a 64Kbyte external Serial Peripheral Interface (SPI) Flash. The AT25F512 interface permits the RTL8111B to read from, and write data to, an external SPI Flash device and provides 64Kbytes of serial reprogrammable Flash memory.

Advanced Configuration Power management Interface (ACPI)—power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM)—is supported to achieve the most efficient power management possible. PCI Message Signaled Interrupt (MSI) is also supported.

In addition to the ACPI feature, remote wake-up (including AMD Magic Packet™, Re-LinkOk, and Microsoft® Wake-up frame) is supported in both ACPI and APM (Advanced Power Management) environments. To support WOL from a deep power down state (e.g., D3cold, i.e. main power is off and only auxiliary exists), the auxiliary power source must be able to provide the needed power for the RTL8111B.

The RTL8111B is fully compliant with Microsoft® NDIS5 (IP, TCP, UDP) Checksum and Segmentation Task-offload features, and supports IEEE 802 IP Layer 2 priority encoding and IEEE 802.1Q Virtual bridged Local Area Network (VLAN). The above features contribute to lowering CPU utilization, especially benefiting performance when in operation on a network server.

The device also features next-generation inter-connect PCI Express technology. PCI Express is a high-bandwidth, low pin count, serial, interconnect technology that offers significant improvements in performance over conventional PCI and also maintains software compatibility with existing PCI infrastructure.

The RTL8111B is suitable for multiple market segments and emerging applications, such as desktop, mobile, workstation, server, communications platforms, and embedded applications.

2. Features

- Integrated 10/100/1000 transceiver
- Auto-Negotiation with Next Page capability
- Supports PCI Express™ 1.0a
- Supports pair swap/polarity/skew correction
- Crossover Detection & Auto-Correction
- Wake-on-LAN and remote wake-up support
- Microsoft® NDIS5 Checksum Offload (IP, TCP, UDP) and Largesend Offload support
- Supports Full Duplex flow control (IEEE 802.3x)
- Fully compliant with IEEE 802.3, IEEE 802.3u, IEEE 802.3ab

- Supports IEEE 802.1P Layer 2 Priority Encoding
- Supports IEEE 802.1Q VLAN tagging
- Serial EEPROM
- SPI Flash Interface
- Transmit/Receive on-chip buffer (48KB) support
- Supports power down/link down power saving
- Supports PCI Message Signaled Interrupt (MSI)
- 64-pin QFN package

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3. System Applications

- PCI Express™ Gigabit Ethernet on Motherboard, Notebook, or Embedded system

4.   Pin Assignments
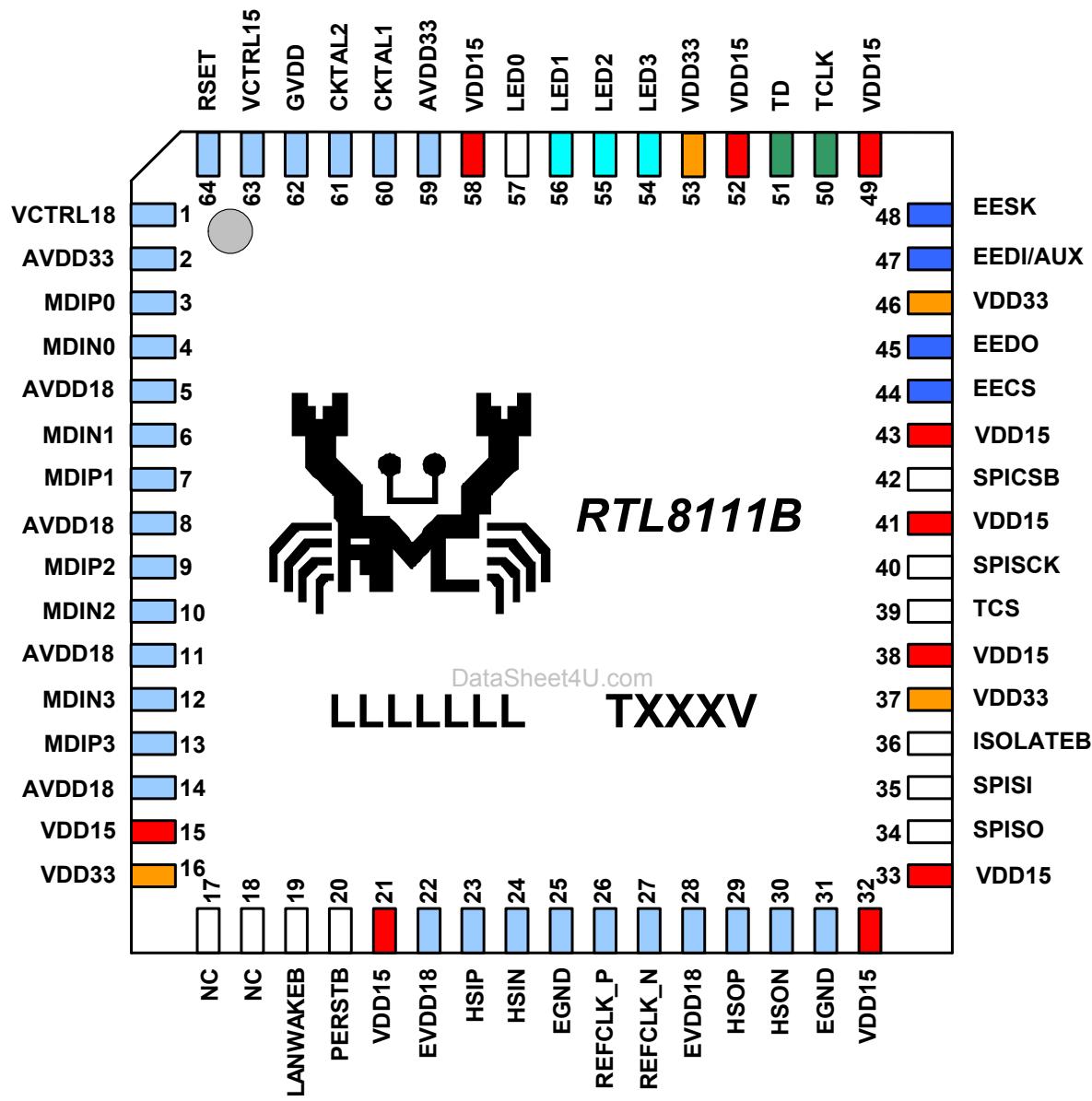
Figure 1.   Pin Assignments

4.1.   Lead (Pb)-Free Package Identification

Lead (Pb)-free package is indicated by an "L" in the location marked "T" in Figure 1.

5. Pin Descriptions

The signal type codes below are used in the following tables:

I:	Input	S/T/S:	Sustained Tri-State
O:	Output	O/D:	Open Drain
T/S:	Tri-State bi-directional input/output pin		

5.1. *Power Management/Isolation*

Table 1.   Power Management/Isolation

Symbol	Type	Pin No	Description
LANWAKEB	O/D	19	Power Management Event: Open drain, active low. Used to reactivate the PCI Express slot's main power rails and reference clocks.
ISOLATEB	I	36	Isolate Pin: Active low. Used to isolate the RTL8111B from the PCI Express bus. The RTL8111B will not drive its PCI Express outputs (excluding LANWAKEB) and will not sample its PCI Express input as long as the Isolate pin is asserted.

5.2. *PCI Express Interface*

Table 2.   PCI Express Interface

Symbol	Type	Pin No	Description
REFCLK_P	I	26	PCI Express Differential Reference Clock Source: 100MHz ± 300ppm.
REFCLK_N	I	27	
HSOP	O	29	PCI Express Transmit Differential Pair.
HSON	O	30	
HSIP	I	23	PCI Express Receive Differential Pair.
HSIN	I	24	
PERSTB	I	20	PCI Express Reset Signal: Active low. When the PERSTB is asserted at power-on state, the RTL8111B returns to a pre-defined reset state and is ready for initialization and configuration after the de-assertion of the PERSTB.

5.3. *EEPROM*

Table 3.   EEPROM

Symbol	Type	Pin No	Description
EESK	O	48	Serial data clock.
EEDI/AUX	O/I	47	EEDI: Output to serial data input pin of EEPROM. AUX: Input pin to detect if Aux. Power exists or not on initial power-on. This pin should be connected to EEPROM. To support wakeup from ACPI D3cold or APM power-down, this pin must be pulled high to Aux. Power via a resistor. If this pin is not pulled high to Aux. Power, the RTL8111B assumes that no Aux. Power exists.
EEDO	I	45	Input from serial data output pin of EEPROM.
EECS	O	44	EECS: EEPROM chip select.

5.4. Transceiver Interface

Table 4.   Transceiver Interface

Symbol	Type	Pin No	Description
MDIP0	I/O	3	In MDI mode, this is the first pair in 1000Base-T, i.e. the BI_DA+/- pair, and is the
MDIN0	I/O	4	transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDIP1	I/O	7	In MDI mode, this is the second pair in 1000Base-T, i.e. the BI_DB+/- pair, and is
MDIN1	I/O	6	the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDIP2	I/O	9	In MDI mode, this is the third pair in 1000Base-T, i.e. the BI_DC+/- pair.
MDIN2	I/O	10	In MDI crossover mode, this pair acts as the BI_DD+/- pair.
MDIP3	I/O	13	In MDI mode, this is the fourth pair in 1000Base-T, i.e. the BI_DD+/- pair.
MDIN3	I/O	12	In MDI crossover mode, this pair acts as the BI_DC+/- pair.

5.5. Clock

Table 5.   Clock

Symbol	Type	Pin No	Description
CKXTAL1	I	60	Input of 25MHz clock reference.
CKXTAL2	O	61	Output of 25MHz clock reference.

5.6. Regulator & Reference

Table 6.   Regulator & Reference

Symbol	Type	Pin No	Description
VCTRL15	O	63	Regulator Control. Voltage control to external 1.5V power transistor.
VCTRL18	O	1	Regulator Control. Voltage control to external 1.8V power transistor.
RSET	I	64	Reference. External resistor reference.

5.7. LEDs

Table 7.   LEDs

Symbol	Type	Pin No	Description				
LED0	O	57	LEDS1-0	00	01	10	11
LED1	O	56	LED0	Tx/Rx	LINK10/1000/ACT	Tx	LINK10/ACT
LED2	O	55					
LED3	O	54	LED1	LINK100	LINK100/1000/ACT	LINK	LINK100/ACT
			LED2	LINK10	FULL	Rx	FULL
			LED3	LINK1000	LINK1000	FULL	LINK1000/ACT

Note 1: During power down mode, the LED signals are logic high.
Note 2: LEDS1-0's initial value comes from the 93C46. If there is no 93C46, the
default value of the (LEDS1, LEDS0) = (1, 1).

5.8. *Power & Ground*

Table 8.   Power & Ground

Symbol	Type	Pin No	Description
VDD33	Power	16, 37, 46, 53	Digital 3.3V power supply.
VDD15	Power	15, 21, 32, 33, 38, 41, 43, 49, 52, 58	Digital 1.5V power supply.
AVDD18	Power	5, 8, 11, 14	Analog 1.8V power supply.
EVDD18	Power	22, 28	Analog 1.8V power supply.
GVDD	O	62	Output 1.5V.
AVDD33	Power	2, 59	Analog 3.3V power supply.
EGND	Power	25, 31	Analog Ground.

Note 1: GVDD is tied to the internal 1.5V power supply. Do not connect this pin to any other power supply. Connect only to two capacitors.
Note 2: Refer to the most updated schematic circuit for correct configuration.

5.9. *NC (Not Connected) Pins*

Table 9.   NC (Not Connected) Pins

Symbol	Type	Pin No	Description
NC		17, 18	Not Connected.

5.10. *SPI (Serial Peripheral Interface) Flash Pins*

Table 10.   SPI Flash Pins

Symbol	Type	Pin No	Description
SPISO	I	34	Input from serial data output pin of SPI Flash.
SPISI	O	35	Output to serial data input pin of SPI Flash.
SPISCK	O	40	Serial data clock.
SPICSB	O	42	SPI Flash chip select.

6. Functional Description

6.1. PCI Express Bus Interface

The RTL8111B is compliant with PCI Express Base Specification Revision 1.0a, and runs at a 2.5GHz signaling rate with X1 link width, i.e., one transmit and one receive differential pair. The RTL8111B supports four types of PCI Express messages: interrupt messages, error messages, power management messages, and hot-plug messages. To ease PCB layout constraints, PCI Express lane polarity reversal and link reversal are also supported.

6.1.1. PCI Express Transmitter

The RTL8111B's PCI Express block receives digital data from the Ethernet interface and performs data scrambling with Linear Feedback Shift Register (LFSR) and 8B/10B coding technology into 10-bit code groups. Data scrambling is used to reduce the possibility of electrical resonance on the link, and 8B/10B coding technology is used to benefit embedded clocking, error detection, and DC balance by adding an overhead to the system through the addition of 2 extra bits. The data code groups are passed through its serializer for packet framing. The generated 2.5Gbps serial data is transmitted onto the PCB trace to its upstream device via a differential driver.

6.1.2. PCI Express Receiver

The RTL8111B's PCI Express block receives 2.5Gbps serial data from its upstream device to generate parallel data. The receiver's PLL circuits are re-synchronized to maintain bit and symbol lock. Through 8B/10B decoding technology and data descrambling, the original digital data is recovered and passed to the RTL8111B's internal Ethernet MAC to be transmitted onto the Ethernet media.

6.2. LED Functions

The RTL8111B supports four LED signals in four different configurable operation modes. The following sections describe the various LED actions.

6.2.1. Link Monitor

The Link Monitor senses link integrity, such as LINK10, LINK100, LINK1000, LINK10/100/1000, LINK10/ACT, LINK100/ACT, or LINK1000/ACT. Whenever link status is established, the specific link LED pin is driven low. Once a cable is disconnected, the link LED pin is driven high, indicating that no network connection exists.

6.2.2. Rx LED

In 10/100/1000Mbps mode, blinking of the Rx LED indicates that receive activity is occurring.
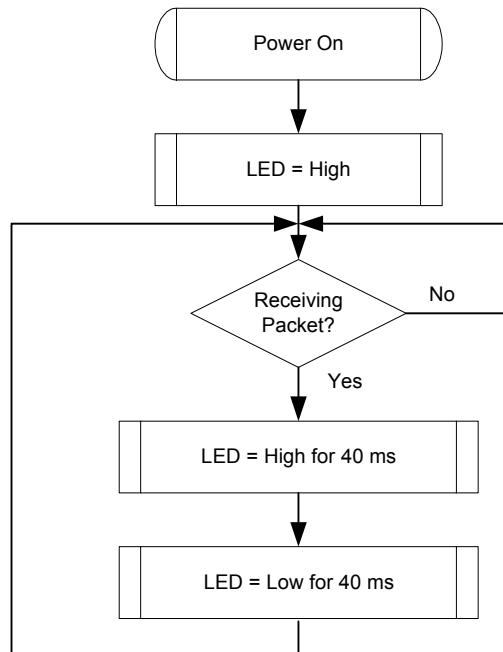
Figure 2.   Rx LED

6.2.3. Tx LED

In 10/100/1000Mbps mode, blinking of the Tx LED indicates that transmit activity is occurring.
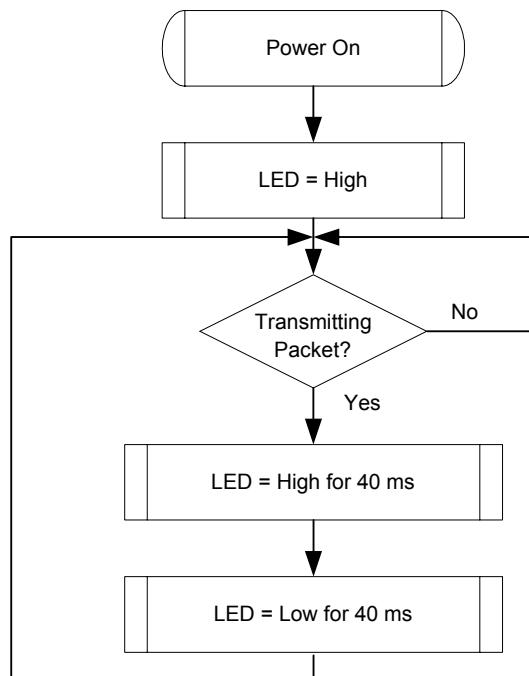
Figure 3.   Tx LED

6.2.4. Tx/Rx LED

In 10/100/1000Mbps mode, blinking of the Tx/Rx LED indicates that both transmit and receive activity is occurring.
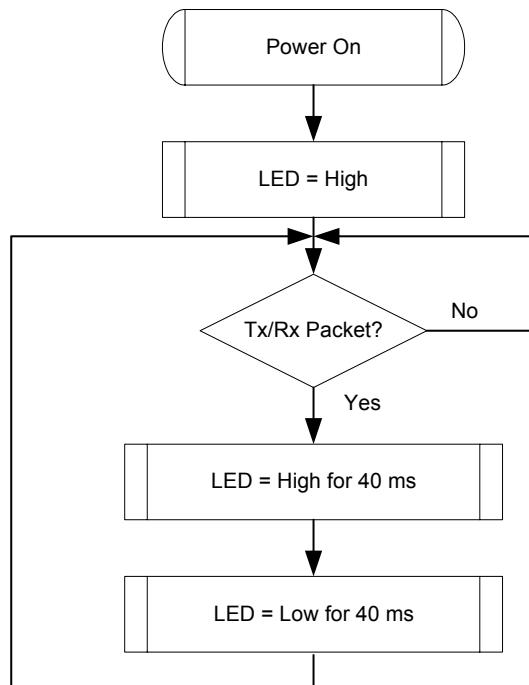
Figure 4.   Tx/Rx LED

6.2.5. LINK/ACT LED

In 10/100/1000Mbps mode, blinking of the LINK/ACT LED indicates that the RTL8111B is linked and operating properly. When this LED is high for extended periods, it indicates that a link problem exists.
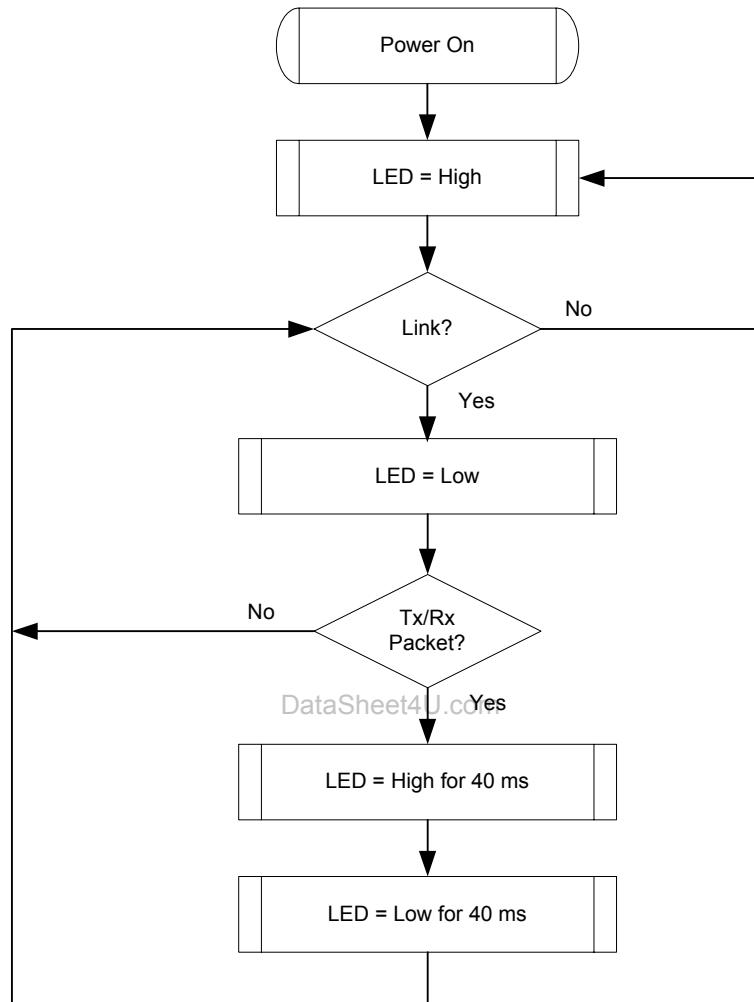

Figure 5.   LINK/ACT LED

6.3. PHY Transceiver

6.3.1. PHY Transmitter

Based on state-of-the-art DSP technology and mixed-mode signal processing technology, the RTL8111B operates at 10/100/1000Mbps over standard CAT.5 UTP cable (100/1000Mbps), and CAT.3 UTP cable (10Mbps).

GMII (1000Mbps) Mode

The RTL8111B's PCS layer receives data bytes from the MAC through the GMII interface and performs the generation of continuous code-groups through 4D-PAM5 coding technology. These code groups are passed through a waveform-shaping filter to minimize EMI effect, and are transmitted onto the 4-pair CAT5 cable at 125MBaud/s through a D/A converter.

MII (100Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 25MHz (TXC), are converted into 5B symbol code through 4B/5B coding technology, then through scrambling and serializing, are converted to 125Mhz NRZ and NRZI signals. After that, the NRZI signals are passed to the MLT3 encoder, then to the D/A converter and transmitted onto the media.

MII (10Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 2.5MHz (TXC), are serialized into 10Mbps serial data. The 10Mbps serial data is converted into a Manchester-encoded data stream and is transmitted onto the media by the D/A converter.

6.3.2. PHY Receiver

GMII (1000Mbps) Mode

Input signals from the media pass through the sophisticated on-chip hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. Afterwards, the received signal is processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. Then, the 8-bit-wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The Rx MAC retrieves the packet data from the receive MII/GMII interface and sends it to the Rx Buffer Manager.

MII (100Mbps) Mode

The MLT3 signal is processed with an ADC, equalizer, BLW (Baseline Wander) correction, timing recovery, MLT3 and NRZI decoder, descrambler, 4B/5B decoder, and is then presented to the MII interface in 4-bit-wide nibbles at a clock speed of 25MHz.

MII (10Mbps) Mode

The received differential signal is converted into a Manchester-encoded stream first. Next, the stream is processed with a Manchester decoder and is de-serialized into 4-bit-wide nibbles. The 4-bit nibbles are presented to the MII interface at a clock speed of 2.5MHz.

6.4. Next Page

If 1000Base-T mode is advertised, three additional Next Pages are automatically exchanged between the two link partners. Users can set PHY Reg4.15 to 1 to manually exchange extra Next Pages via Reg7 and Reg8 as defined in IEEE 802.3ab.

6.5. EEPROM Interface

The RTL8111B requires the attachment of an external EEPROM. The 93C46/93C56 is a 1K-bit/2K-bit EEPROM. The EEPROM interface permits the RTL8111B to read from, and write data to, an external serial EEPROM device.

Values in the external EEPROM allow default fields in PCI configuration space and I/O space to be overridden following a power-on or software EEPROM auto-load command. The RTL8111B will auto-load values from the EEPROM. If the EEPROM is not present, the RTL8111B initialization uses default values for the appropriate Configuration and Operational Registers. Software can read and write to the EEPROM using bit-bang accesses via the 9346CR Register, or using PCI VPD (Vital Product Data). The interface consists of EESK, EECS, EEDO, and EEDI.

The correct EEPROM (i.e. 93C46/93C56) must be used in order to ensure proper LAN function.

Table 11.   EEPROM Interface

EEPROM	Description
EECS	93C46/93C56 chip select.
EESK	EEPROM serial data clock.
EEDI/Aux	Input data bus/Input pin to detect whether Aux. Power exists on initial power-on. This pin should be connected to EEPROM. To support wakeup from ACPI D3cold or APM power-down, this pin must be pulled high to Aux. Power via a resistor. If this pin is not pulled high to Aux. Power, the RTL8111B assumes that no Aux. Power exists.
EEDO	Output data bus.

6.6. Power Management

The RTL8111B is compliant with ACPI (Rev 1.0, 1.0b, 2.0), PCI Power Management (Rev 1.1), PCI Express Active State Power Management (ASPM), and Network Device Class Power Management Reference Specification (V1.0a), such as to support an Operating System-directed Power Management (OSPM) environment.

The RTL8111B can monitor the network for a Wakeup Frame, a Magic Packet, or a Re-LinkOk, and notify the system via a PCI Express Power Management Event (PME) Message, Beacon, or LANWAKEB pin when such a packet or event occurs. Then the system can be restored to a normal state to process incoming jobs.

When the RTL8111B is in power down mode (D1 ~ D3):

- The Rx state machine is stopped. The RTL8111B monitors the network for wakeup events such as a Magic Packet, Wakeup Frame, and/or Re-LinkOk, in order to wake up the system. When in power down mode, the RTL8111B will not reflect the status of any incoming packets in the ISR register and will not receive any packets into the Rx on-chip buffer.

- The on-chip buffer status and packets that have already been received into the Rx on-chip buffer before entering power down mode are held by the RTL8111B.

- Transmission is stopped. PCI Express transactions are stopped. The Tx on-chip buffer is held.

- After being restored to D0 state, the RTL8111B transmits data that was not moved into the Tx on-chip buffer during power down mode. Packets that were not transmitted completely last time are re-transmitted.

The D3cold_support_PME bit (bit15, PMC register) and the Aux_I_b2:0 bits (bit8:6, PMC register) in PCI configuration space depend on the existence of Aux power (bit15, PMC) = 1.

If EEPROM D3cold_support_PME bit (bit15, PMC) = 0, the above 4 bits are all 0's.

Example:

If EEPROM D3c_support_PME = 1:

- If aux. power exists, then PMC in PCI config space is the same as EEPROM PMC
  (if EEPROM PMC = C2 F7, then PCI PMC = C2 F7)

- If aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's (if EEPROM PMC = C2 F7, then PCI PMC = 02 76)

In the above case, if wakeup support is desired when main power is off, it is suggested that the EEPROM PMC be set to C2 F7 (Realtek EEPROM default value).

If EEPROM D3c_support_PME = 0:

- If aux. power exists, then PMC in PCI config space is the same as EEPROM PMC
  (if EEPROM PMC = C2 77, then PCI PMC = C2 77)

- If aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's (if EEPROM PMC = C2 77, then PCI PMC = 02 76)

In the above case, if wakeup support is not desired when main power is off, it is suggested that the EEPROM PMC be set to 02 76.

Link Wakeup occurs only when the following conditions are met:

- The LinkUp bit (CONFIG3#4) is set to 1, the PMEn bit (CONFIG1#0) is set to 1, and the corresponding wake-up method (message, beacon, or LANWAKEB) can be asserted in the current power state.

Magic Packet Wakeup occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the RTL8111B, e.g., a broadcast, multicast, or unicast packet addressed to the current RTL8111B adapter.
- The received Magic Packet does not contain a CRC error.
- The Magic bit (CONFIG3#5) is set to 1, the PMEn bit (CONFIG1#0) is set to 1, and the corresponding wake-up method (message, beacon, or LANWAKEB) can be asserted in the current power state.
- The Magic Packet pattern matches, i.e. 6 * FFh + MISC (can be none) + 16 * DID (Destination ID) in any part of a valid Ethernet packet.

A Wakeup Frame event occurs only when the following conditions are met:

- The destination address of the received Wakeup Frame is acceptable to the RTL8111B, e.g., a broadcast, multicast, or unicast address to the current RTL8111B adapter.
- The received Wakeup Frame does not contain a CRC error.
- The PMEn bit (CONFIG1#0) is set to 1.
- The 16-bit CRC[A] of the received Wakeup Frame matches the 16-bit CRC of the sample Wakeup Frame pattern given by the local machine's OS. Or, the RTL8111B is configured to allow direct packet wakeup, e.g., a broadcast, multicast, or unicast network packet.

  Note: 16-bit CRC: The RTL8111B supports two normal wakeup frames (covering 64 mask bytes from offset 0 to 63 of any incoming network packet) and three long wakeup frames (covering 128 mask bytes from offset 0 to 127 of any incoming network packet).

The corresponding wake-up method (message, beacon, or LANWAKEB) is asserted only when the following conditions are met:

- The PMEn bit (bit0, CONFIG1) is set to 1.
- The PME_En bit (bit8, PMCSR) in PCI Configuration Space is set to 1.
- The RTL8111B may assert the corresponding wake-up method (message, beacon, or LANWAKEB) in the current power state or in isolation state, depending on the PME_Support (bit15-11) setting of the PMC register in PCI Configuration Space.
- A Magic Packet, LinkUp, or Wakeup Frame has been received.
- Writing a 1 to the PME_Status (bit15) of the PMCSR register in the PCI Configuration Space clears this bit and causes the RTL8111B to stop asserting the corresponding wake-up method (message, beacon, or LANWAKEB) (if enabled).

When the RTL8111B is in power down mode, e.g., D1-D3, the IO and MEM accesses to the RTL8111B are disabled. After a PERSTB assertion, the device's power state is restored to D0 automatically if the original power state was D3$_{cold}$. There is almost no hardware delay at the device's power state transition. When in ACPI mode, the device does not support PME (Power Management Enable) from D0 (this is the Realtek default setting of the PMC register auto-loaded from EEPROM). The setting may be changed from the EEPROM, if required.

6.7. *Vital Product Data (VPD)*

Bit 31 of the Vital Product Data (VPD) capability structure in the RTL8111B's PCI Configuration Space is used to issue VPD read/write commands and is also a flag used to indicate whether the transfer of data between the VPD data register and the 93C46/93C56 has completed or not.

1. Write VPD register: (write data to the 93C46/93C56)
   Set the flag bit to 1 at the same time the VPD address is written to write VPD data to EEPROM. When the flag bit is reset to 0 by the RTL8111B, the VPD data (4 bytes per VPD access) has been transferred from the VPD data register to EEPROM.
2. Read VPD register: (read data from the 93C46/93C56)
   Reset the flag bit to 0 at the same time the VPD address is written to retrieve VPD data from EEPROM. When the flag bit is set to 1 by the RTL8111B, the VPD data (4 bytes per VPD access) has been transferred from EEPROM to the VPD data register.

Note1: Refer to the PCI 2.2 Specifications for further information.

Note2: The VPD address must be a DWORD-aligned address as defined in the PCI 2.2 Specifications. VPD data is always consecutive 4-byte data starting from the VPD address specified.

Note3: Realtek reserves offset 40h to 7Fh in EEPROM mainly for VPD data to be stored.

Note4: The VPD function of the RTL8111B is designed to be able to access the full range of the 93C46/93C56 EEPROM.

6.8. SPI Flash Interface

The RTL8111B supports the attachment of a 64Kbyte external Serial Peripheral Interface (SPI) Flash. The AT25F512 provides 64Kbytes of serial reprogrammable Flash memory.

SPI Flash is enabled by the RTL8111B through the Chip Select pin, and accessed via a 3-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). The AT25F512/1024 utilizes an 8-bit instruction register. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low transition.

Instead of a parallel bus interface, the Serial Peripheral Interface provides simpler wiring and much less interaction (crosstalk) among the conductors in the cable. This minimizes the number of conductors, pins, and the IC package size, reducing the cost of making, assembling, and testing the electronics.

Table 12.   SPI Flash Interface

SPI Flash	Description
SO	Input data bus.
SI	Output data bus.
SCK	SPI Flash serial data clock.
CS	SPI Flash chip select.

7.   Characteristics

7.1.   Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 13.   Absolute Maximum Ratings

Symbol	Description	Minimum	Maximum	Unit
VDD3, HV1VDD	Supply Voltage 3.3V	-0.5	4.6	V
V0VDD	Supply Voltage 2.5V	-0.5	3	V
VDD1A	Supply Voltage 1.8V	-0.5	2.1	V
LVVDD	Supply Voltage V*			
VDD1	Supply Voltage 1.5V	-0.5	2	V
DCinput	Input Voltage	-0.5	Corresponding Supply Voltage + 0.5	V
DCoutput	Output Voltage	-0.5	Corresponding Supply Voltage + 0.5	V
	Storage Temperature	-55	+125	°C

Refer to the most updated schematic circuit for correct configuration.

7.2.   Recommended Operating Conditions

Table 14.   Recommended Operating Conditions

Description	Pins	Minimum	Typical	Maximum	Unit
Supply Voltage VDD	VDD3, HV1VDD	3.0	3.3	3.6	V
	V0VDD	2. 25	2.5	2.75	V
	VDD1A	1.71	1.8	1.89	V
	LVVDD	*			V
	VDD1	1.425	1.5	1.575	V
Ambient Temperature T_A		0		70	°C
Maximum Junction Temperature				125	°C

Refer to the most updated schematic circuit for correct configuration.

7.3.   Crystal Requirements

Table 15.   Crystal Requirements

Symbol	Description/Condition	Minimum	Typical	Maximum	Unit
F_{ref}	Parallel resonant crystal reference frequency, fundamental mode, AT-cut type.		25		MHz
F_{ref} Stability	Parallel resonant crystal frequency stability, fundamental mode, AT-cut type. T_a=25°C.	-50		+50	ppm
F_{ref} Tolerance	Parallel resonant crystal frequency tolerance, fundamental mode, AT-cut type. T_a=-20°C ~+70°C.	-30		+30	ppm
F_{ref} Duty Cycle	Reference clock input duty cycle.	40		60	%
C_L	Load Capacitance.				pF
ESR	Equivalent Series Resistance.				Ω
DL	Drive Level.			0.5	mW

7.4. Thermal Characteristics

Table 16. Thermal Characteristics

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Operating Ambient Temperature	0	70	°C

7.5. DC Characteristics

Table 17. DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VDD3, HV1VDD	3.3V Supply Voltage		3.0	3.3	3.6	V
V0VDD	2.5V Supply Voltage		2.25	2.5	2.75	V
VDD1A,	1.8V Supply Voltage		1.71	1.8	1.89	V
LVVDD	Supply Voltage*					V
VDD1	1.5V Supply Voltage		1.425	1.5	1.575	V
Voh	Minimum High Level Output Voltage	Ioh = -8mA	0.9 * VDD3		VDD3	V
Vol	Maximum Low Level Output Voltage	Iol= 8mA			0.1 * VDD3	V
Vih	Minimum High Level Input Voltage		0.5 * VDD3		VDD3+0.5	V
Vil	Maximum Low Level Input Voltage		-0.5		0.3 * VDD3	V
Iin	Input Current	Vin = VDD3 or GND	-1.0		1.0	µA
Icc33	Average Operating Supply Current from 3.3V			TBD		mA
Icc25	Average Operating Supply Current from 2.5V			TBD		mA
Icc18	Average Operating Supply Current from 1.8V			TBD		mA
Icc15	Average Operating Supply Current from 1.5V			TBD		mA

* Refer to the most updated schematic circuit for correct configuration.

7.6. AC Characteristics

7.6.1. Serial EEPROM Interface Timing

93C46(64*16)/93C56(128*16)
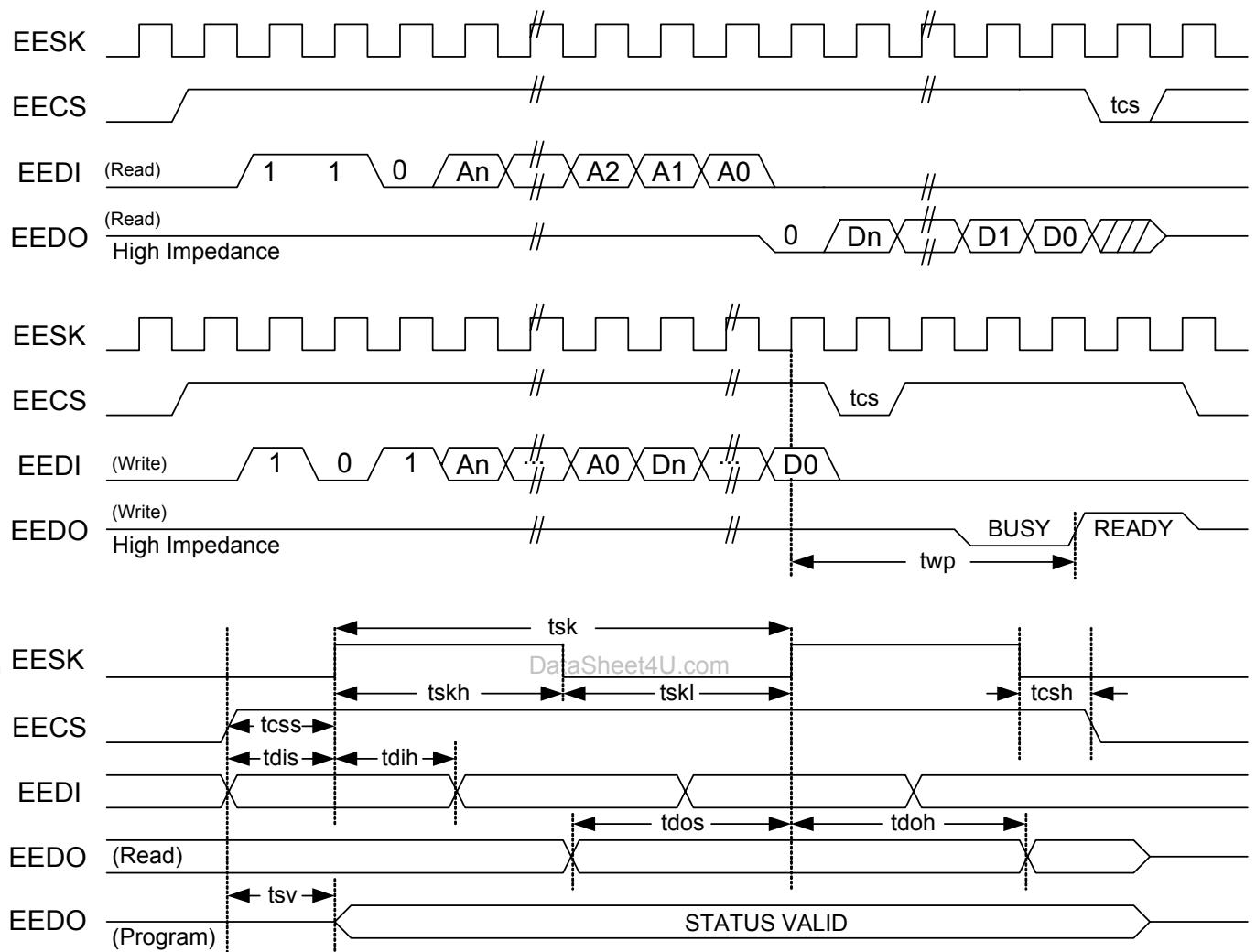
Figure 6.   Serial EEPROM Interface Timing

Table 18. EEPROM Access Timing Parameters

Symbol	Parameter	EEPROM Type	Min.	Max.	Unit
tcs	Minimum CS Low Time	9346	1000		ns
twp	Write Cycle Time	9346		10	ms
tsk	SK Clock Cycle Time	9346	4		µs
tskh	SK High Time	9346	1000		ns
tskl	SK Low Time	9346	1000		ns
tcss	CS Setup Time	9346	200		ns
tcsh	CS Hold Time	9346	0		ns
tdis	DI Setup Time	9346	400		ns
tdih	DI Hold Time	9346	400		ns
tdos	DO Setup Time	9346	2000		ns
tdoh	DO Hold Time	9346		2000	ns
tsv	CS to Status Valid	9346		1000	ns

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7.6.2. SPI Flash Interface Timing
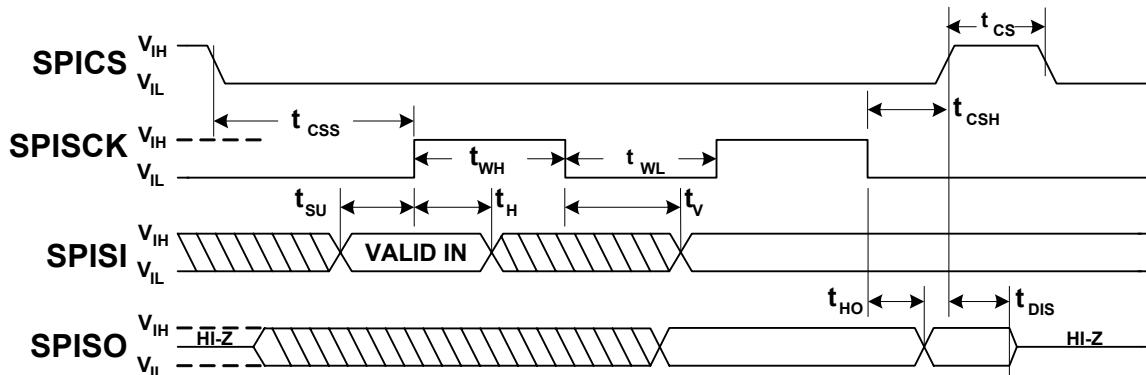
Figure 7.   Synchronous Data Timing
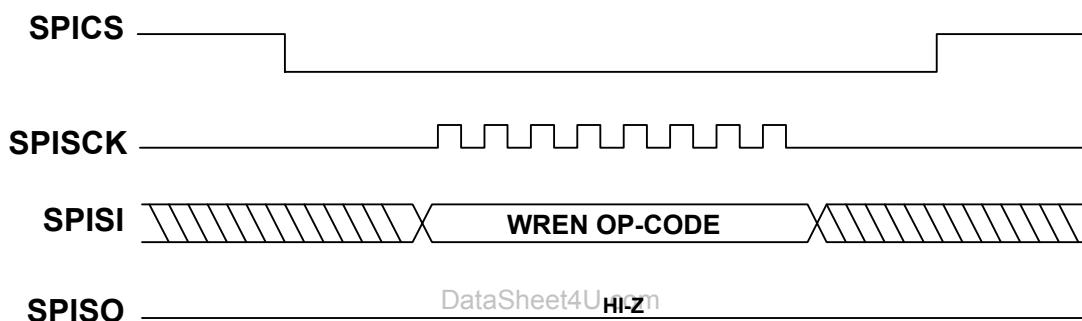
Figure 8.   WREN Timing
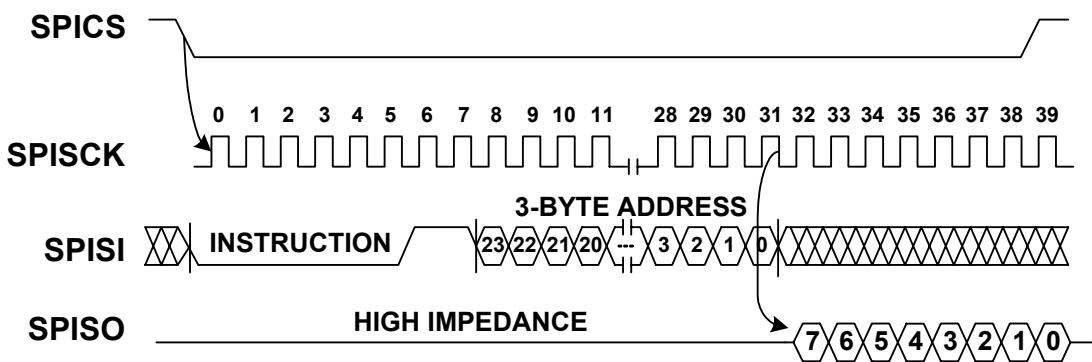
Figure 9.   Read Timing

REALTEK
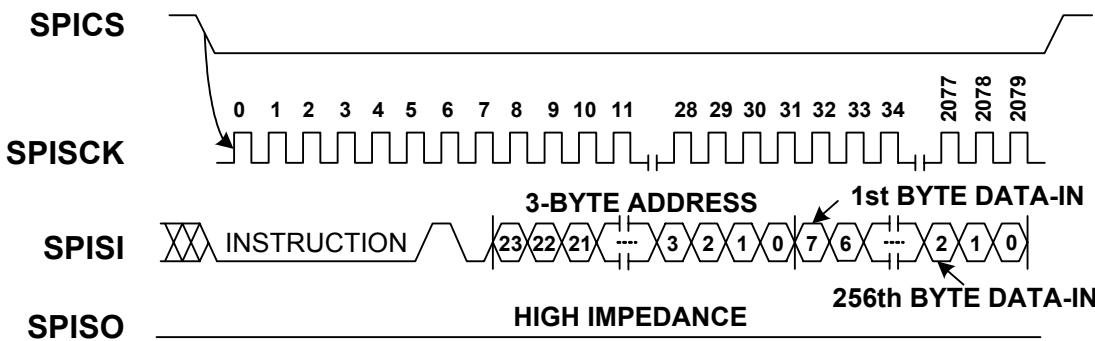
Figure 10.   Program Timing
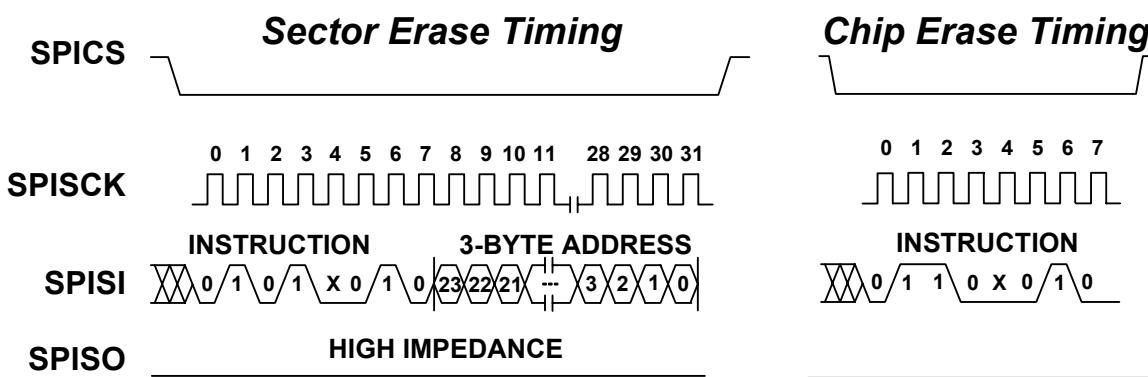
Figure 11.   Sector/Chip Erase Timing

Table 19.   SPI Flash Timing Parameters

Symbol	Parameter	Compatible Type	Min	Max	Unit
t_{CSS}	SPICS Setup Time	AT25F512	25		ns
t_{CSH}	SPICS Hold Time	AT25F512	25		ns
t_{CS}	SPICS High Time	AT25F512	25		ns
t_{WH}	SPISCK High Time	AT25F512	20		ns
t_{WL}	SPISCK Low Time	AT25F512	20		ns
t_{SU}	Data In Setup Time	AT25F512	5		ns
t_{H}	Data In Hold Time	AT25F512	5		ns
t_{V}	Output Valid	AT25F512		20	ns
t_{HO}	Output Hold Time	AT25F512	0		ns
t_{DIS}	Output Disable Time	AT25F512		100	ns

7.7. *PCI Express Bus Parameters*

7.7.1. Differential Transmitter Parameters

Table 20. Differential Transmitter Parameters

Symbol	Parameter	Min	Typical	Max	Units
UI	Unit Interval[2]	399.88	400	400.12	ps
$V_{TX-DIFFp-p}$	Differential Peak to Peak Output Voltage	0.800		1.2	V
$V_{TX-DE-RATIO}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB
T_{TX-EYE}	Minimum Tx Eye Width	0.70			UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.15	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D- Tx Output Rise/Fall Time	0.125			UI
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage			20	mV
$V_{TX-CM-DCACTIVE-IDLEDELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0		100	mV
$V_{TX-CM-DCLINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0		25	mV
$V_{TX-IDLE-DIFFp}$	Electrical Idle Differential Peak Output Voltage	0		20	mV
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection			600	mV
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0		3.6	V
$I_{TX-SHORT}$	TX Short Circuit Current Limit			90	mA
$T_{TX-IDLE-MIN}$	Minimum time spent in Electrical Idle	50			UI
$T_{TX-IDLE-SETTO-IDLE}$	Maximum time to transition to a valid Electrical Idle after sending an Electrical Idle ordered set			20	UI
$T_{TX-IDLE-TOTO-DIFF-DATA}$	Maximum time to transition to valid TX specifications after leaving an Electrical Idle condition			20	UI
$RL_{TX-DIFF}$	Differential Return Loss	12			dB
RL_{TX-CM}	Common Mode Return Loss	6			dB
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω
Z_{TX-DC}	Transmitter DC Impedance	40			Ω
$L_{TX-SKEW}$	Lane-to-Lane Output Skew			500+2 UI	ps
C_{TX}	AC Coupling Capacitor	75		200	nF
$T_{crosslink}$	Crosslink Random Timeout	0		1	ms

Note1: Refer to PCI Express Base Specification, rev.1.0a, for correct measurement environment setting of each parameter.
Note2: The data rate can be modulated with an SSC (Spread Spectrum Clock) from +0 to -0.5% of the nominal data rate frequency, at a modulation rate in the range not exceeding 30 kHz – 33 kHz. The +/- 300 ppm requirement still holds, which requires the two communicating ports be modulated such that they never exceed a total of 600 ppm difference.

7.7.2. Differential Receiver Parameters

Table 21. Differential Receiver Parameters

Symbol	Parameter	Min.	Typical	Max.	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{RX-DIFFp-p}$	Differential Input Peak to Peak Voltage	0.175		1.200	V
T_{RX-EYE}	Minimum Receiver Eye Width	0.4			UI
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.3	UI
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage			150	mV
$RL_{RX-DIFF}$	Differential Return Loss	15			dB
RL_{RX-CM}	Common Mode Return Loss	6			dB
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω
Z_{RX--DC}	DC Input Impedance	40	50	60	Ω
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200 k			Ω
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65		175	mV
$T_{RX-IDLE-DET-DIFFENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time			10	ms
$L_{RX-SKEW}$	Total Skew			20	ns

Note: Refer to PCI Express Base Specification, rev.1.0a, for correct measurement environment setting of each parameter.

7.7.3. REFCLK Parameters

Table 22. REFCLK Parameters

Symbol	Parameter	100MHz Input Min	100MHz Input Max	Units
T_{absmin}	Absolute min. DIF CLK Period	9.872		ns
T_{rise}	Rise Time	175	700	ps
T_{fall}	Fall Time	175	700	ps
hΔ T_{rise}	Rise Time Variation		125	ps
Δ T_{fall}	Fall Time Variation		125	ps
Rise/Fall Matching			20	%
V_{high}	Voltage High (typical 0.71V)	660	850	mV
V_{low}	Voltage Low (typical 0.0V)	-150		mV
$V_{cross\ absolute}$	Absolute Crossing Point Voltages	250	550	mV
$V_{cross\ relative}$	Relative Crossing Point Voltages	Note[2]	Note[2]	V
Total Δ V_{cross}	Total Variation of V_{cross} over all edges		140	mV
$T_{ccjitter}$	Cycle to Cycle Jitter		125	ps
Duty Cycle		45	55	%
V_{ovs}	Maximum Voltage (Overshoot)		$V_{high\ avg}$ + 0.3	V
V_{uds}	Minimum Voltage (Undershoot)		-0.3	V
V_{rb}	Ringback Voltage	0.2	N/A	V

Note1: Refer to PCI Express Base Specification, rev.1.0a, for correct measurement environment setting of each parameter.
Note2: Vcross relative Min = 0.5(Vhigh_avg – 0.710) + 0.250, Vcross relative Max = 0.5(Vhigh_avg – 0.710) + 0.550.
The crossing point must meet the absolute and relative crossing point specifications simultaneously.
Note3: The nominal single-ended swing for each clock is 0 to 0.7V with a nominal frequency of 100MHz ±300 PPM.
Note4: The reference clocks may support spread spectrum clocking. The minimum clock period cannot be violated.
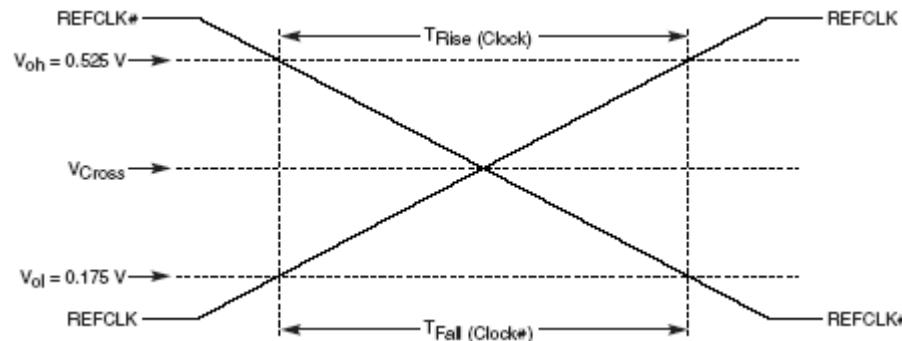
Figure 12.   REFCLK Single-Ended Measurement Points for T$_{rise}$ and T$_{fall}$
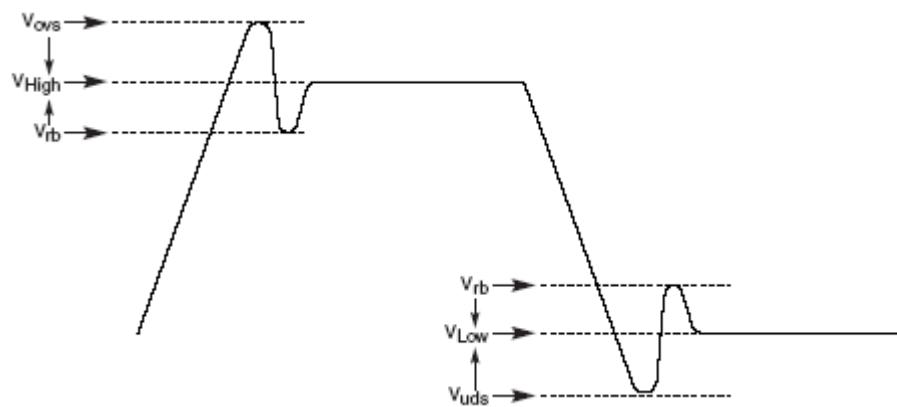
Figure 13.   REFCLK Single-Ended Measurement Points for V$_{ovs}$, V$_{uds,}$ and V$_{rb}$
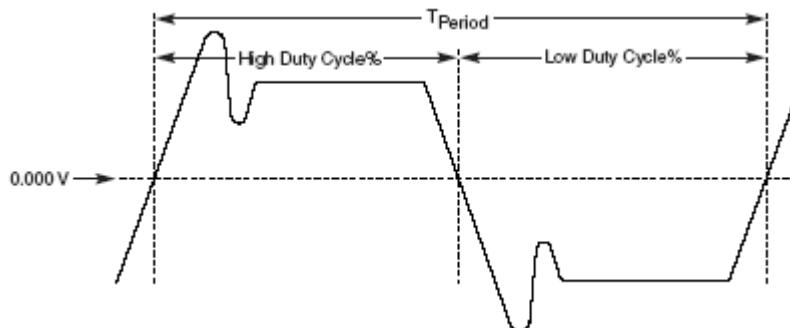
Figure 14.   REFCLK Differential Measurement Points for T$_{period}$, Duty Cycle, and Jitter

V_{cross} (rel) Max = 0.5 (V_{havg} − 0.170) + .550
V_{cross} (rel) Min = 0.5 (V_{havg} − 0.170) + .250
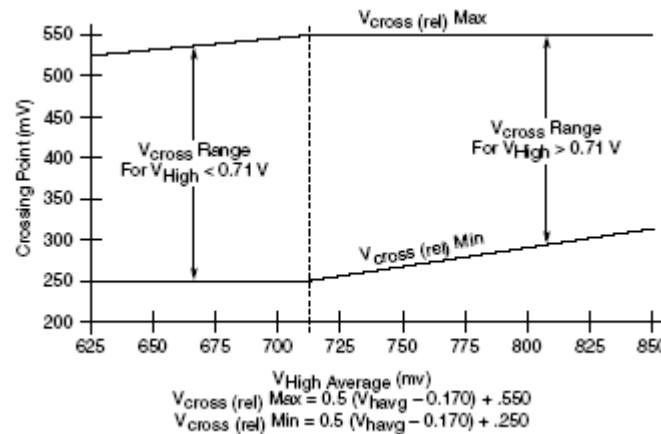
Figure 15.   REFCLK V_{cross} Range

7.7.4.   Auxiliary Signal Timing Parameters

Table 23.   Auxiliary Signal Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{PVPERL}	Power stable to PERSTB inactive	100		ms
$T_{PERST-CLK}$	REFCLK stable before PERSTB inactive	100		µs
T_{PERST}	PERSTB active time	100		µs
T_{FAIL}	Power level invalid to PWRGD inactive		500	ns
T_{WKRF}	LANWAKEB rise – fall time		100	ns
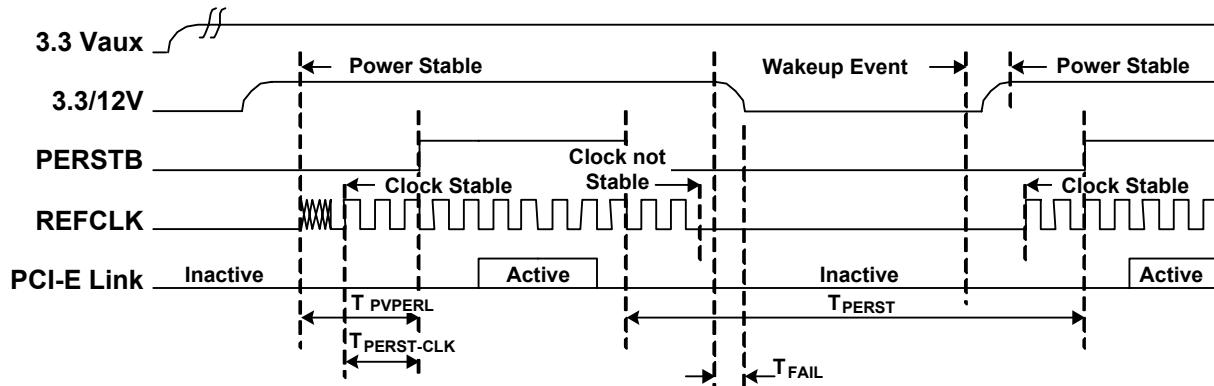
Figure 16.   Auxiliary Signal Timing

8. Mechanical Dimensions

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.0008	0.002
A2	---	0.65	1.00	---	0.026	0.039
A3	0.20 REF			0.008 REF		
b	0.18	0.23	0.30	0.007	0.009	0.012
D	9.00 BSC			0.354 BSC		
D1	8.75 BSC			0.344 BSC		
E	9.00 BSC			0.354 BSC		
E1	8.75 BSC			0.344 BSC		
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	---	12°	0°	---	12°
aaa	---	---	0.25	---	---	0.010
bbb	---	---	0.10	---	---	0.004
chamfer	---	---	0.60	---	---	0.024

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER

2. REFERENGE DOCUMENT: PROPSED JEDEC MO-220.

Exposed Pad Size & Support bar table

L/F	D2 (mm)			E2 (mm)			※
①	6.90	7.05	7.20	6.90	7.05	7.20	YES / NO
②	6.70	6.85	7.00	6.70	6.85	7.00	NO
③	5.54	5.69	5.84	5.54	5.69	5.84	NO
④	3.64	3.79	3.94	3.64	3.79	3.94	NO

OVER MOLD

TITLE : 64LD QFN (9X9 mm) PACKAGE OUTLINE			
L/F MATERIAL : A194 FH(PPF)			
APPR.	Holman Chen	DWG NO.	CE064-SW1
ENG.	C.Y.Horng	REV NO.	c
QM.	S.T.Liao	PRODUCT CODE	CE0641A
CHK.	Y.Y.Lai	DATE	06/18/'02

COPY CONTROLLED	REV NO	DESCRIPTION	DATE	DWG.	R.K.Wang	SHT No.	1/1
	C	Add Exposed Pad Size & Support bar table	06/17/02	SILICONWARE PRECISION INDUSTRIES CO., LTD.			

9. Ordering Information

Table 24.   Ordering Information

Part Number	Package	Status
RTL8111B	64-Pin QFN	
RTL8111B-LF	64-Pin QFN Lead (Pb)-Free package	

Note: See page 3 for lead (Pb)-free package ID information.