GENERAL INSTRUMENT

AY-3-1270

Digital Thermometer and Temperature Controller

FEATURES

- Measurement and control range −399° C to +399° C (option 200° C to 499° C)
- Accuracy ±1.5° C, 0° C to −30° C using Thermistor temperature sensor
- Direct drive of liquid crystal displays
- Direct drive of 0.6" common anode L.E.D. displays
- 40 pin dual in line package
- Can be used as a digital voltmeter with digital autozero ±399 range
- 9 volt supply
- Leading zero blanking
- Power failure and over-range indication by flashing display
- Adjustable Hysteresis 0, 0.2, 0.4, 0.8, 2, 4, 8 degrees
- Two control/alarm outputs, HIGH and LOW

DESCRIPTION

The Digital Thermometer/Controller chip is an N-Channel MOS integrated circuit which when used in conjunction with a Thermistor, an L.E.D. or L.C.D. display and a power supply forms a complete unit intended primarily for use in Deep Freezers, though it may also be used for the display and control of any parameter.

Two control outputs are provided, one which operates when the reading is higher than the set point and the other when the reading is lower. The switching hysteresis is presettable as required.

A power fail detector is incorporated on the chip. If power is removed for more than a specified time, the initial reading at restoration of power will be retained and the display will flash. The display will also flash if during normal operation an over-range condition occurs.

With minor changes to the peripheral circuitry, the chip can be used for other temperature ranges, or used as a 2¾ digit digital voltmeter.

OPERATION

The chip uses a single ramp conversion technique to measure the imbalance of a thermistor bridge temperature sensor. A digital autozero system which operates on every other measurement cycle, is employed to compensate for offsets in the comparators.

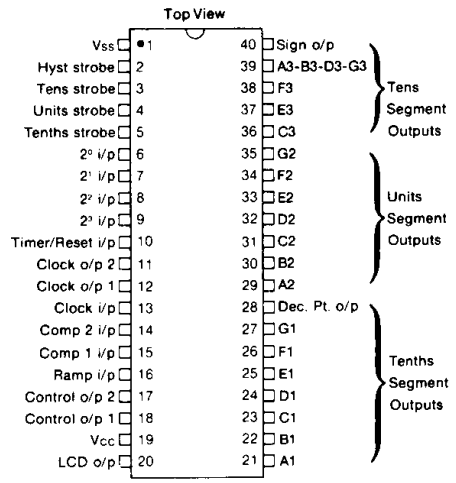
The chip may be used as a digital voltmeter by removing the thermistor network and connecting the signal to be measured between the two comparator inputs.

The set point circuitry compares the actual reading to the value presented to the set point inputs.

Two outputs are provided, one which operates at Set Point plus Hysteresis and the other which operates at Set Point minus Hysteresis. In addition, .05° display hysteresis has been introduced

PIN CONFIGURATION

40 LEAD DUAL IN LINE



to prevent control output and L.S.D. jitter. An optional power failure detection circuit is provided. At power up the chip will read normally for about 10 sec—actual time determined by an external capacitor—then it will store the last reading and flash the display. In this condition the chip will continue to make measurements and operate the control outputs normally. Operating the reset button will restore the normal display. If there is a short duration power failure the circuit will ignore it, if it lasts longer than 10 sec the alarm condition will occur.

HIGH READING OPTION

For normal operation Pin 39 drives segments A3, B3, D3 and G3 in parallel. Pin 38 drives segment F3, Pin 37 drives segments E3 and Pin 36 drives segment C3.

For 20.0 to 49.9 range Pin 39 drives segment C3. Pin 38 drives segment E3, Pin 37 drives segment A3 and D3 and Pin 36 drives segment F3. Segments B3, G3 are connected to Pin 28 (Decimal Point).

PIN FUNCTIONS

Pin No.	Name	Description
1	V_{SS}	Negative Supply (0_V)
2	Hysteresis Strobe Output	Common output for Hysteresis and LED select switches
3	Tens Strobe Output	Common output for Tens and Sign select switches
4	Units Strobe Output	Common output for Units select switches
5	Tenths Strobe Output	Common output for Tenths select switches
6	Set Point 2^0 Input (Control & Hysteresis)	Common input for 2^0 bit
7	Set Point 2^1 Input (Control & Hysteresis)	Common input for 2^1 bit
8	Set Point 2^2 Input (Control & Hysteresis)	Common input for 2^2 bit
9	Set Point 2^3 Input (Control & Hysteresis)	Common input for 2^3 bit
10	Timer Input/Reset Timer Input	Connected to a capacitor to V_{SS} and switch to V_{CC} for power failure detection and reset. The nominal delay time is 10 sec when a 10μF capacitor is used
11	Clock Output 2	Connected to frequency determining network
12	Clock Output 1	See Figure 1
13	Clock Input	
14	Comparator Input 2	Connected to nominal $V_{CC}/2$ reference
15	Comparator Input 1	Connect to thermistor network
16	Ramp Input	Connect to Resistor to V_{CC} and Capacitor to V_{SS}
17	Control Output 2 (HIGH)	Open drain output which turns ON when reading is greater than (Set Point + Hysteresis). Turns OFF again when reading equals Set Point
18	Control Output 1 (LOW)	Open drain output which turns OFF when reading equals (Set Point—Hysteresis)
19	V_{CC}	Positive supply (9V nom.)
20	LCD Backplate Output	Square wave output to drive backplate of LCD display
21	Segment A1 Output	
22	Segment B1 Output	
23	Segment C1 Output	
24	Segment D1 Output	
25	Segment E1 Output	
26	Segment F1 Output	
27	Segment G1 Output	
28	Decimal Point Output	
29	Segment A2 Output	Tens, Units and Tenths 7 segment outputs
30	Segment B2 Output	In LED mode these are open drain outputs
31	Segment C2 Output	designed to sink 12.5mA per segment
32	Segment D2 Output	In LCD mode these are push pull outputs
33	Segment E2 Output	
34	Segment F2 Output	
35	Segment G2 Output	
36	Segment C3 Output	
37	Segment E3 Output	
38	Segment F3 Output	
39	Segment A3, B3, D3, G,	
40	Sign Output	On for a negative reading

CLOCK OSCILLATOR

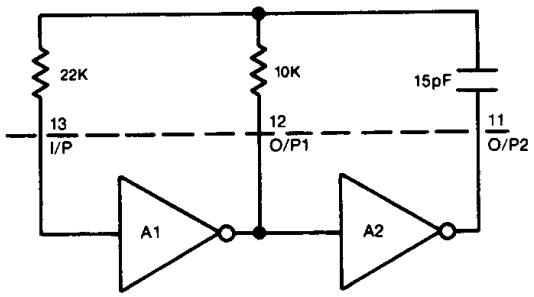
The Clock oscillator is designed to operate with an R-C network, an LC network or a Ceramic resonator. The choice will depend on the system Temperature and Voltage stability requirements.

As the thermometer reading is directly proportional to the clock frequency a ceramic resonator is recommended for frequency stability. In systems where only small variations in supply voltage and ambient temperature occur an R-C network could be used. The frequency variation over the specified operating range with an R-C is about ±22% (i.e. from 7V to 11V supply variation and −25° C to 70° C Temperature variation).

CHIP INTERFACE CIRCUITS

The input configuration on the Set Point inputs is shown in Fig. 2.

The circuit for the display drive is shown in Fig. 3. and shows the internal switching required to drive LED or LCD displays.



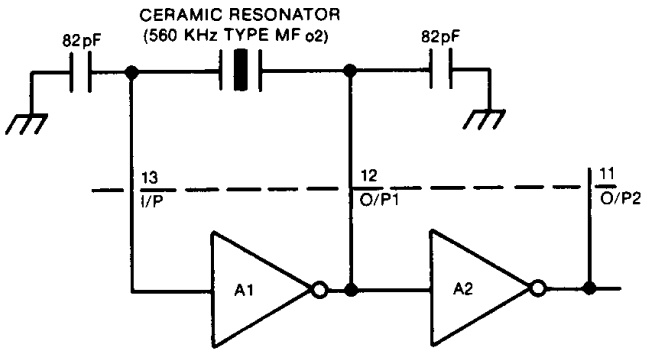


Fig. 1 TYPICAL OSCILLATOR CONFIGURATIONS

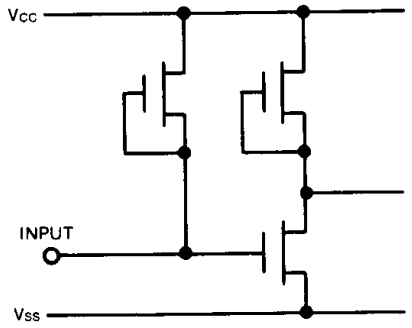


Fig. 2 SET POINTS INPUTS

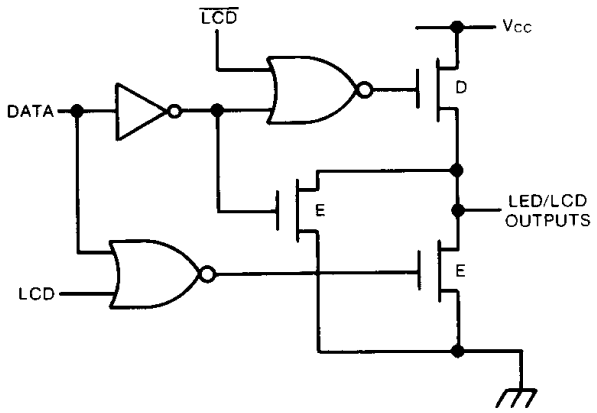


Fig. 3 DISPLAY OUTPUTS

ANALOG CIRCUITRY

The Temperature measuring circuit consists of a bridge network connected across the power supplies.

One side of the bridge (which is connected to comparator 2 input) consists of two equal value fixed resistors. These set up a reference potential of approximately Vcc/2 (4.5V). The other side of the bridge (which is connected to Comparator 1 Input) consists of a Thermistor and a series resistor connected to Vcc and a resistor connected to Vss. A suitable thermistor is Mullard Type 640-90003.

The bridge is arranged to balance at 0°. As the temperature varies, the voltage at Comparator 2 input goes from approximately 3V (at −39.9°) to 6V (at +39.9°) in a non linear fashion.

A non linear ramp is generated by R and C and the time taken for the ramp voltage to change from one comparator input voltage to the other gives the temperature. R is varied to adjust the FSD. The non linearity of the ramp to a large extent compensates for the non linearity of the thermistor network.

For use with linear sensors or as a digital voltmeter the Resistor would be replaced by a current source.

Reading will be negative if comparator input 1 voltage < comparator input 2.

Typical circuit diagrams showing the AY-3-1270 displaying temperature in a freezer are shown in Fig. 9 (with LED display) and Fig. 10 (with LCD display).

SET POINT PROGRAMMING

To set the control temperature, diodes are inserted in the program matrix with the cathodes connected to the strobe lines on pins 2, 3, 4. The code is B. C. D., and any temperature within the operating range can be selected by a suitable combination of diodes. For a negative temperature set point, a diode is inserted between pins 8 and 3.

When an L.E.D. display is being used the diode between pins 9 and 2 is inserted, which inhibits the L.C.D. backplate waveform. This waveform is shown in Fig. 4.

A timing waveform for the strobe lines is shown in Fig. 5.

2^0 (pin 6)	2^1 (pin 7)	2^2 (pin 8)	2^3 (pin 9)	
0.1	0.2	0.4	0.8	Tenths (pin 5)
1	2	4	8	Units (pin 4)
10	20	Minus	Do not Use	Tens (pin 3)
A	B	C	LED Display	Hysteresis (pin 2)

To set the hysteresis level, that is the temperature difference above and below the "set point" at which the control outputs operate, diodes are inserted in locations A, B, and C according to the following table. Fig. 6 shows the control output characteristics with temperature.

	Hysteresis	A	B	C
	0			
	±0.2	*		
	±0.4		*	
	±0.8	*	*	
Note 2	±2	*		*
Note 2	±4		*	*
Note 2	±8	*	*	*

*indicates presence of a programming diode

NOTES:

1. Set points must consist of valid BCD codes or incorrect readings will occur.
2. The ½° LSD Control and Display hysteresis should also be taken into account.
3. When in the "High Reading" mode it is necessary to program a set point 10° C lower than that required.
   e.g. To select 44° C diodes are inserted in the matrix between pins 6, 3/7, 3/8, 4.
4. Nominal hysteresis value; for actual hysteresis obtained see table on following page.

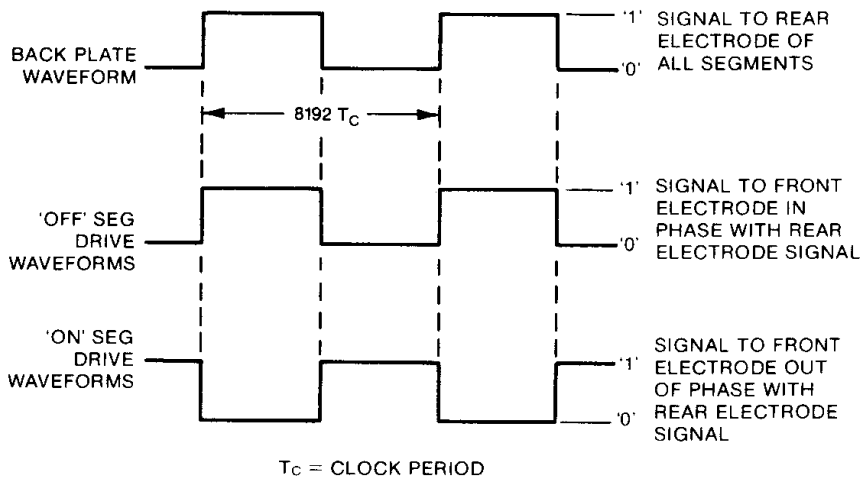
HYSTERESIS

When ±2, ±4 or ±8 is set the actual hysteresis obtained is as shown:

Set Temp.	Hyst. ±2	Hyst. ±4	Hyst. ±8
+XX9	+2.0/−1.9	+4.0/−3.9	+8.0/−7.9
+XX8	+2.1/−1.8	+4.1/−3.8	+8.1/−7.8
+XX7	+2.2/−1.7	+4.2/−3.7	+8.2/−7.7
+XX6	+2.3/−1.6	+4.3/−3.6	+8.3/−7.6
+XX5	+2.4/−1.5	+4.4/−3.5	+8.4/−7.5
+XX4	+2.5/−1.4	+4.5/−3.4	+8.5/−7.4
+XX3	+2.6/−1.3	+4.6/−3.3	+8.6/−7.3
+XX2	+2.7/−1.2	+4.7/−3.2	+8.7/−7.2
+XX1	+2.8/−1.1	+4.8/−3.1	+8.8/−7.1
+XX0	+2.9/−2.0	+4.9/−4.0	+8.9/−8.0
+000	+2.9/−2.9	+4.9/−4.9	+8.9/−8.9
−000	+2.9/−2.9	+4.9/−4.9	+8.9/−8.9
−XX0	+2.0/−2.9	+4.0/−4.9	+8.0/−8.9
−XX1	+1.1/−2.8	+3.1/−4.8	+7.1/−8.8
−XX2	+1.2/−2.7	+3.2/−4.7	+7.2/−8.7
−XX3	+1.3/−2.6	+3.3/−4.6	+7.3/−8.6
−XX4	+1.4/−2.5	+3.4/−4.5	+7.4/−8.5
−XX5	+1.5/−2.4	+3.5/−4.4	+7.5/−8.4
−XX6	+1.6/−2.3	+3.6/−4.3	+7.6/−8.3
−XX7	+1.7/−2.2	+3.7/−4.2	+7.7/−8.2
−XX8	+1.8/−2.1	+3.8/−4.1	+7.8/−8.1
−XX9	+1.9/−2.0	+3.9/−4.0	+7.9/−8.0

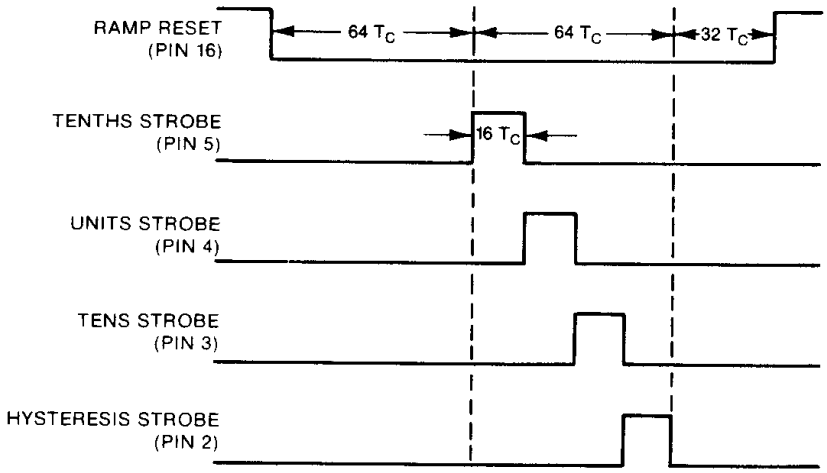
When ±2, ±4 or ±8 is set and the set point is less than or equal to the hysteresis setting then the actual hysteresis is given by the following table:

Set Temp.	Hyst. ±2	Hyst. ±4	Hyst. ±8
+XX9	+2.0/−2.8	+4.0/−4.8	+8.0/−8.8
+XX8	+2.1/−2.7	+4.1/−4.7	+8.1/−8.7
+XX7	+2.2/−2.6	+4.2/−4.6	+8.2/−8.6
+XX6	+2.3/−2.5	+4.3/−4.5	+8.3/−8.5
+XX5	+2.4/−2.4	+4.4/−4.4	+8.4/−8.4
+XX4	+2.5/−2.3	+4.5/−4.3	+8.5/−8.3
+XX3	+2.6/−2.2	+4.6/−4.2	+8.6/−8.2
+XX2	+2.7/−2.1	+4.7/−4.1	+8.7/−8.1
+XX1	+2.8/−2.0	+4.8/−4.0	+8.8/−8.0
+XX0	+2.9/−2.9	+4.9/−4.9	+8.9/−8.9
+000	+2.9/−2.9	+4.9/−4.9	+8.9/−8.9
−000	+2.9/−2.9	+4.9/−4.9	+8.9/−8.9
−XX0	+2.9/−2.9	+4.9/−4.9	+8.9/−8.9
−XX1	+2.0/−2.8	+4.0/−4.8	+8.0/−8.8
−XX2	+2.1/−2.7	+4.1/−4.7	+8.1/−8.7
−XX3	+2.2/−2.6	+4.2/−4.6	+8.2/−8.6
−XX4	+2.3/−2.5	+4.3/−4.5	+8.3/−8.5
−XX5	+2.4/−2.4	+4.4/−4.4	+8.4/−8.4
−XX6	+2.5/−2.3	+4.5/−4.3	+8.5/−8.3
−XX7	+2.6/−2.2	+4.6/−4.2	+8.6/−8.2
−XX8	+2.7/−2.1	+4.7/−4.1	+8.7/−8.1
−XX9	+2.8/−2.0	+4.8/−4.0	+8.8/−8.0



T_C = CLOCK PERIOD

Fig. 4 LCD DRIVE WAVEFORM



T_C IS CLOCK PERIOD

REPETITION RATE OF ABOVE CYCLES IS TWICE MEASUREMENT CYCLE

Fig. 5 STROBE OUTPUT TIMING

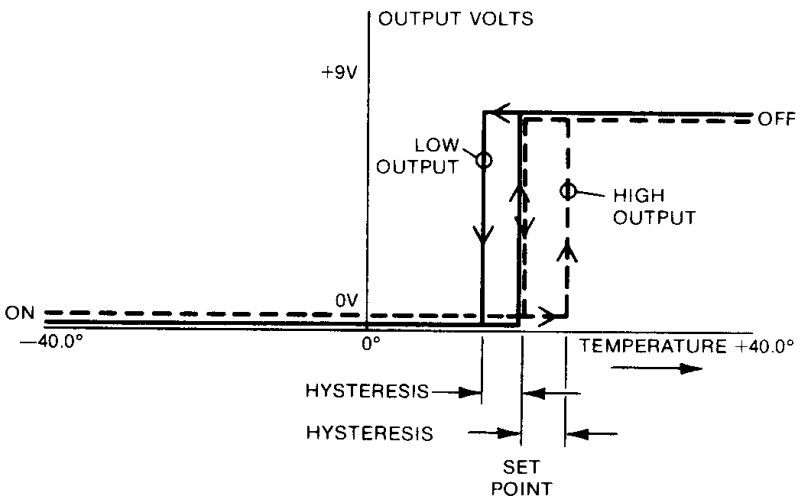


Fig. 6 SET POINT HYSTERESIS

MEASUREMENT AND READ CYCLE

In order to compensate for offsets in the comparators, a digital autozero cycle operates on every other measurement cycle. Fig. 7 shows the internal ramp and comparator waveform.

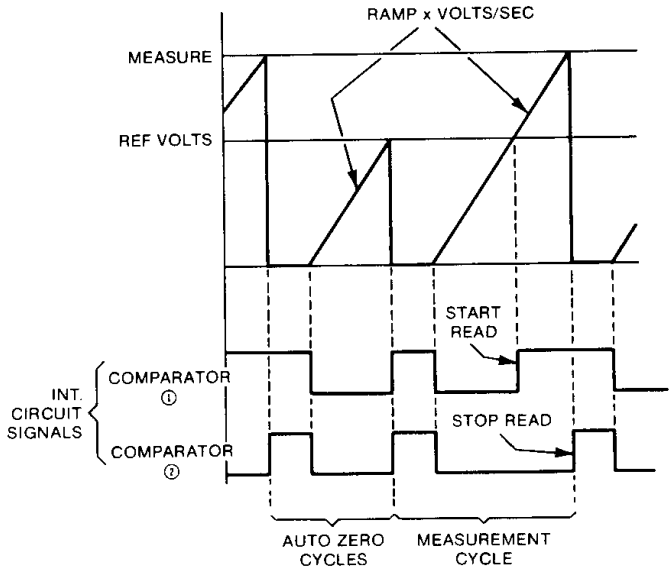


Fig. 7 TYPICAL MEASUREMENT/READ CYCLE

SYSTEM DIAGRAM

Fig. 8 shows a block schematic of the AY-3-1270 circuit.

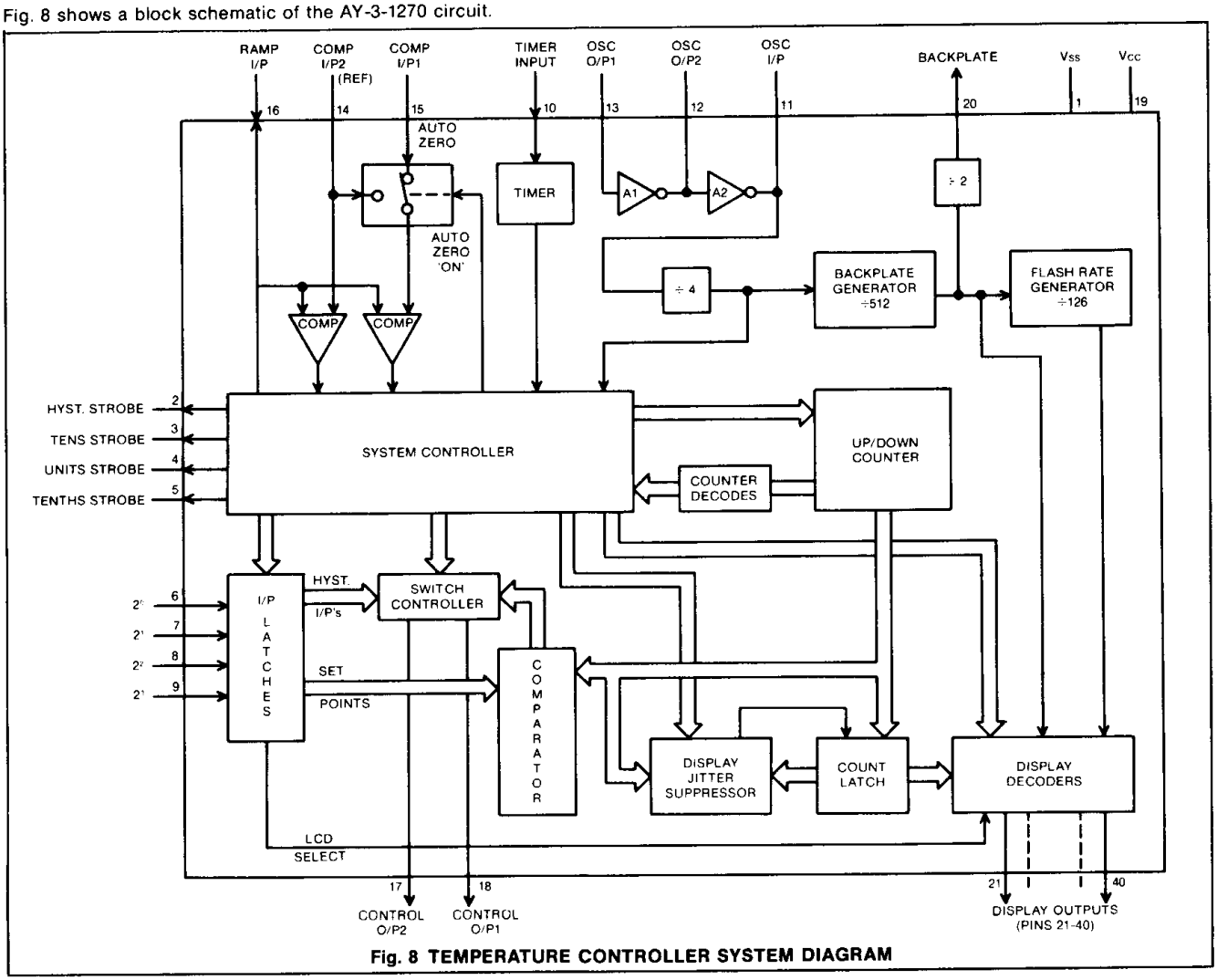


Fig. 8 TEMPERATURE CONTROLLER SYSTEM DIAGRAM

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any Pin with Respect to V_{SS} ..... −0.3 to +18
Storage Temperature Range ..... −65°C to +150°C
Ambient Operating Temperature Range ..... −25°C to +70°C
Maximum Power Dissipation at 70°C 800mW
Maximum Segment Output Current (LED Mode) 20mA
Maximum Switch Output Current 30mA
Maximum Total Output Current 250mA

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise stated):

V_{SS} = 0V V_{CC} = (7.2V to 10.8V) T_{amb} = −25°C to +70°C, positive logic convention

Characteristics	Min	Typ	Max	Units	Conditions
Segment, DP, Sign Outputs LED mode					
On resistance	—	—	120	Ω	V_{out} = +1.5V I_{sink} = 12.5mA
On resistance E3	—	—	60	Ω	V_{out} = +1.5V I_{sink} = 25mA
On resistance DP	—	—	40	Ω	V_{out} = +1.5V I_{sink} = 37.5mA
On resistance (A3, B3, D3, G3)	—	—	30	Ω	V_{out} = +1.5V I_{sink} = 50mA
Segment, DP, Sign Outputs LCD mode					
Logic '0' output	—	—	400	mV	Load = 50pF + 1M Ohm to
Logic '1' output	V_{CC}−400	—	—	mV	E3 load = 100pF + 500K DP load = 150pF + 330K A3, B3, D3, G3 load = 200pF + 250K Backplate load = 1000pF + 50K
Rise time	—	—	—	—	Under specified load conditions
Fall time	—	—	—	—	Under specified load conditions
Frequency	—	68	—	Hz	Clock (560kHz)
Control Outputs					
On resistance	—	—	75	Ω	V_{out} = +1.5V I_{sink} = 20mA
Off leakage	—	—	10	μA	V_{out} = +15 Volts
Strobe Outputs					
On resistance	—	—	400	Ω	V_{out} = +1V I_{sink} = 2.5mA
Off leakage	—	—	10	μA	V_{out} = V_{CC}
Frequency	—	—	—	—	2 x reading rate
Pulse width	—	28.6	—	μs	Clock frequency = 560kHz
Set Point Inputs					
Logic '0' level	V_{SS}	—	2	V	
Logic '1' level	6	—	V_{CC}	V	
Pull up resistance	20	—	100	KΩ	to V_{CC} V_{in} = V_{SS}
Comparator Inputs					
Leakage current •	—	—	1	μA	V_{in} = V_{CC}
Resolution	5	—	—	mV	
Common Mode Range	0.1	—	V_{CC}−3V	V	
Impedance between either input and ramp input	1	—	—	MΩ	Clock frequency = 560kHz
Ramp Input					
Discharge resistance	—	—	100	Ω	V_{out} = +1V I_{sink} = 10mA See note 1
Leakage current	—	—	1	μA	V_{in} = V_{CC}
Timer Input					
Flash Threshold	0.5V_{OC}	—	0.7V_{OC}	V	
Reset Threshold	—	—	6	V	
Pull up resistance	500	—	2500	KΩ	to V_{CC} (V_{in} = V_{SS})
Pull down resistance	50	—	250	KΩ	to V_{SS} (V_{in} = V_{CC})
Open circuit input voltage (V_{OC})	2	2.6	3.5	V	
Clock					
Frequency	300	—	800	kHz	
Gain to output 1 (A1)	3	—	—	—	small signal open loop
Gain to output 2 (A2)	3	—	—	—	AC gain, F = 560kHz
Input capacitance	—	—	12	pF	
Count frequency	—	6.25	—	kHz	Clock (560kHz) ÷ 32 see note 2
Flash rate, Overrange and Power Fail	—	1	—	Hz	Clock (560kHz) ÷ 158048
Supply current	—	25	—	mA	V_{CC} = 9V, T_{amb} = 25°C
	—	—	45	mA	V_{CC} = 11V, T_{amb} = − 25°C

NOTES: 1. Minimum resistance to V_{CC} = 1KΩ Maximum capacitance to V_{SS} = 10μf.

2. Reading is measurement time divided by Count Frequency period. Measurement time depends on both the voltage difference at the Comparator inputs and ramp speed at pin 16.

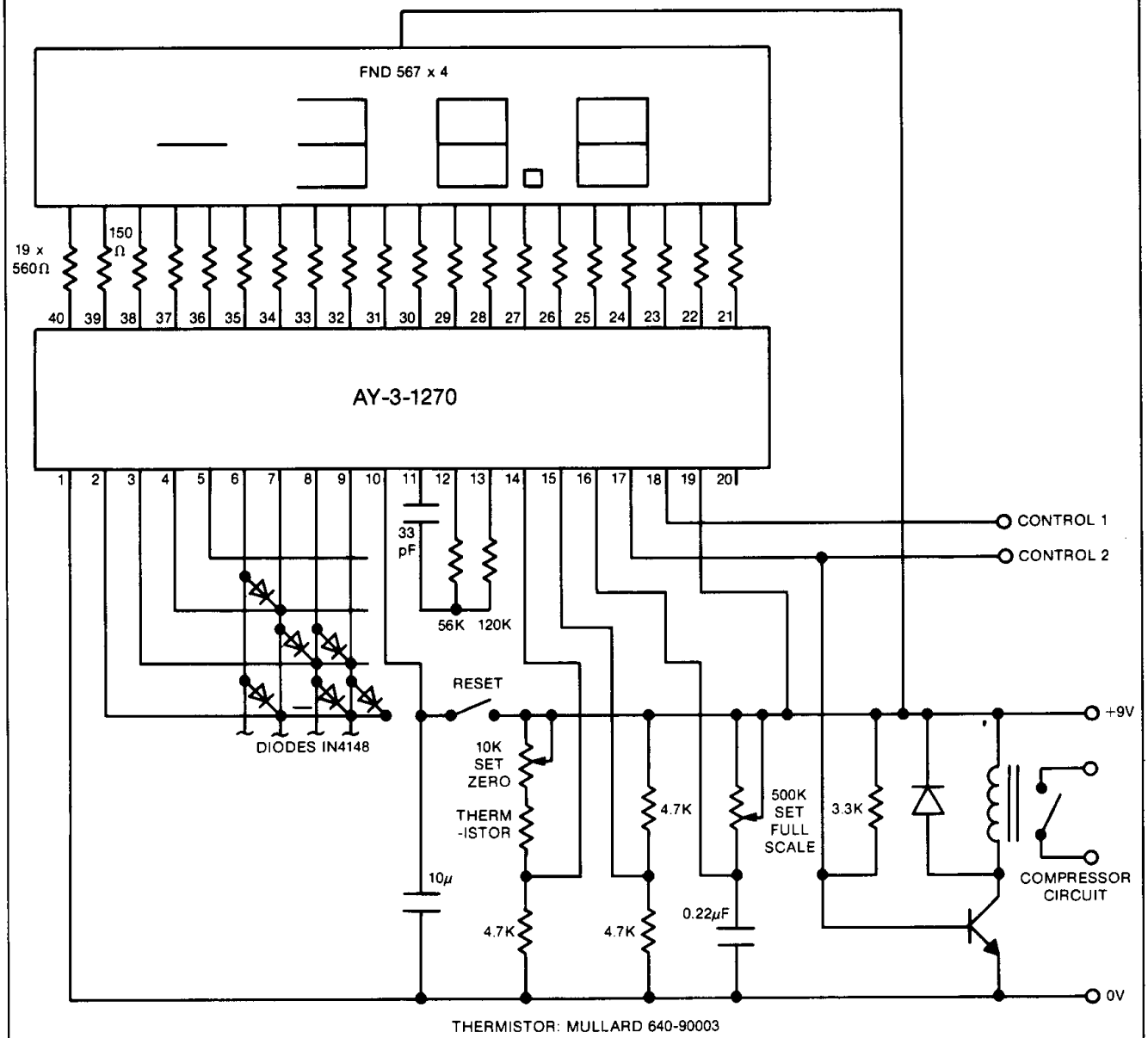


Fig. 9 THERMOMETER WITH LEAD DISPLAY