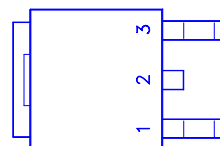
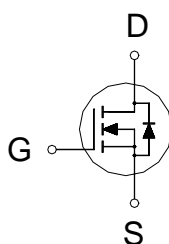


NIKO-SEM**N-Channel Logic Level Enhancement
Mode Field Effect Transistor****P3055LDG**
TO-252 (DPAK)
Lead-Free**PRODUCT SUMMARY**

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
25	50m	12A



1. GATE
2. DRAIN
3. SOURCE

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25\text{ }^\circ\text{C}$	I_D	12	A
	$T_C = 100\text{ }^\circ\text{C}$		8	
Pulsed Drain Current ¹		I_{DM}	45	
Avalanche Energy	$L = 0.1\text{mH}$	E_{AS}	60	mJ
Repetitive Avalanche Energy ²	$L = 0.05\text{mH}$	E_{AR}	3	
Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	48	W
	$T_C = 100\text{ }^\circ\text{C}$		20	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	$^\circ\text{C}$
Lead Temperature ($1/16$ " from case for 10 sec.)		T_L	275	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		3	$^\circ\text{C} / \text{W}$
Junction-to-Ambient	$R_{\theta JA}$		75	
Case-to-Heatsink	$R_{\theta CS}$	1		

¹Pulse width limited by maximum junction temperature.²Duty cycle $\leq 1\%$ **ELECTRICAL CHARACTERISTICS ($T_C = 25\text{ }^\circ\text{C}$, Unless Otherwise Noted)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	25			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	0.8	1.2	2.5	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$			± 250	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}$			25	μA
		$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}, T_J = 125\text{ }^\circ\text{C}$			250	

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Lead-Free

On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 10V, V_{GS} = 10V$	12			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 5V, I_D = 12A$		70	120	m
		$V_{GS} = 10V, I_D = 12A$		50	90	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 15V, I_D = 12A$		16		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 15V, f = 1MHz$		450		pF
Output Capacitance	C_{oss}			200		
Reverse Transfer Capacitance	C_{rss}			60		
Total Gate Charge ²	Q_g	$V_{DS} = 0.5V_{(BR)DSS}, V_{GS} = 10V,$ $I_D = 6A$		15		nC
Gate-Source Charge ²	Q_{gs}			2.0		
Gate-Drain Charge ²	Q_{gd}			7.0		
Turn-On Delay Time ²	$t_{d(on)}$	$V_{DS} = 15V, R_L = 1$ $I_D \cong 12A, V_{GS} = 10V, R_{GS} = 2.5$		6.0		nS
Rise Time ²	t_r			6.0		
Turn-Off Delay Time ²	$t_{d(off)}$			20		
Fall Time ²	t_f			5.0		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_c = 25^\circ C$)						
Continuous Current	I_S			12		A
Pulsed Current ³	I_{SM}			20		
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$		1.5		V
Reverse Recovery Time	t_{rr}	$I_F = I_S, di_F/dt = 100A / \mu S$		30		nS
Peak Reverse Recovery Current	$I_{RM(REC)}$			15		A
Reverse Recovery Charge	Q_{rr}			0.043		μC

¹Pulse test : Pulse Width $\leq 300 \mu sec$, Duty Cycle $\leq 2\%$.²Independent of operating temperature.³Pulse width limited by maximum junction temperature.**REMARK: THE PRODUCT MARKED WITH "P3055LDG", DATE CODE or LOT #****Orders for parts with Lead-Free plating can be placed using the PXXXXXXG parts name.**

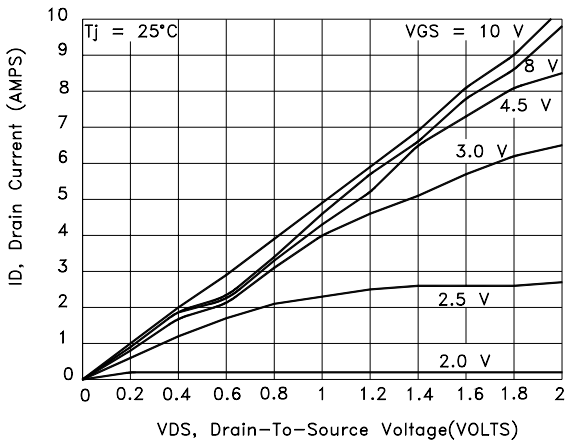


Fig.1 On-Resistance Variation with Temperature

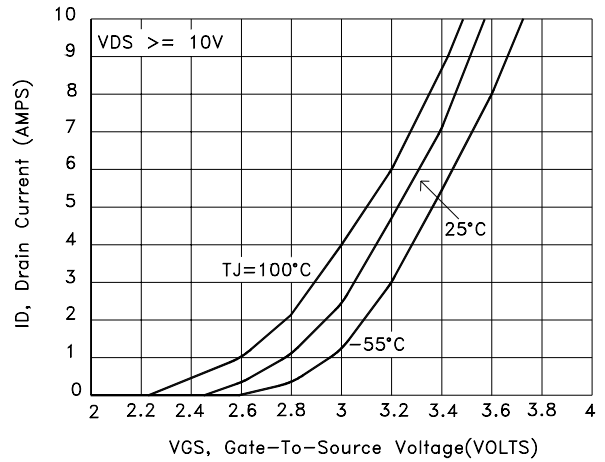


Fig.2 Transfer Characteristics

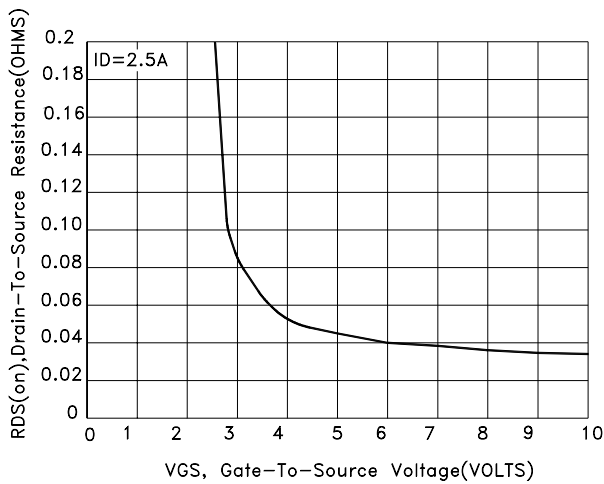


Fig.3 On-Resistance versus Gate-To-Source Voltage

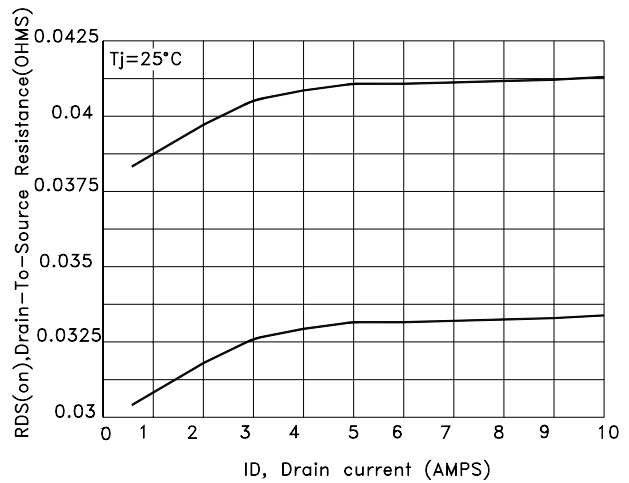


Fig.4 On-Resistance versus Drain Current and Gate Voltage

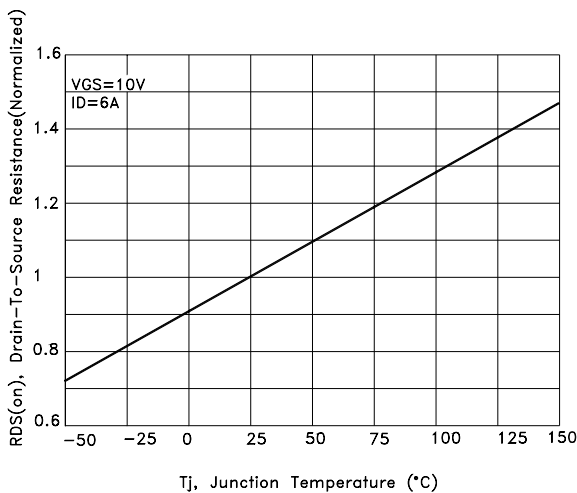


Fig.5 On-Resistance Variation with Temperature

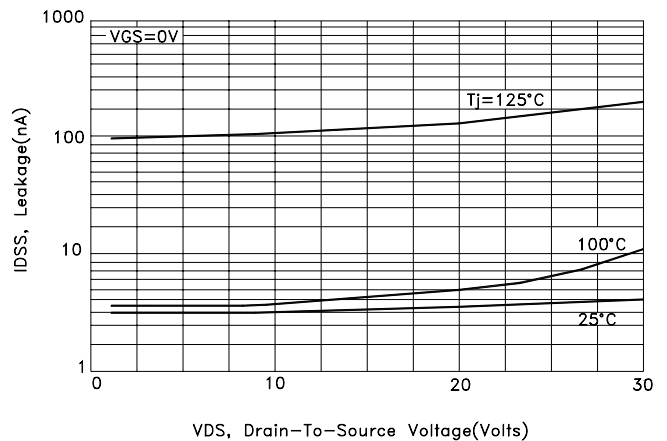


Fig.6 Drain-To-Source Leakage Current versus Voltage

NIKO-SEM**N-Channel Logic Level Enhancement
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TO-252 (DPAK)
Lead-Free**TO-252 (DPAK) MECHANICAL DATA**

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	9.35		10.4	H	0.89		2.03
B	2.2		2.4	I	6.35		6.80
C	0.45		0.6	J	5.2		5.5
D	0.89		1.5	K	0.6		1
E	0.45		0.69	L	0.5		0.9
F	0.03		0.23	M	3.96	4.57	5.18
G	5.2		6.2	N			

