0 ERRATA & RECOMMENDATION

VER 1.21 (DEC.19.2001)

RECOMMENDATIONS & CAUTIONS

1. All unused power pins and input pins (including nTRST, EXTCLK, RTCVDD) have to be tied to proper voltage level. Any floated input pins will make any CMOS semiconductor unstable.
2. The FLAG bit of ADCCON register needs some cautions. Please refer to the manual.
3. To reduce the stop current, cautions are needed. Please refer to the manual.

ERRATA from S3C44B0X User's Manual Preliminary 0.1

[FORMAT]
🗁 **<CHAPTER> : <PAGE> : <CHANGED_ITEM>**
<CHANGED DESCRIPTIONS>

🗁 **OVERVIEW 1-1, 1-2 and 1-4 Operation frequency**
System operation frequency is changed to 66MHz from 75MHz.

🗁 **OVERVIEW 1-16 Output pad current**
The phot6 output pad current is changed to 6mA from 4mA.

🗁 **MEMORY CONTROLLER 4-6, 4-7, 4-13, 4-14 and 4-15 Page removed**
nWAIT, nXBREQ/nXBACK, nGCS, DRAM and SDRAM timing diagrams are moved to chapter 19.

🗁 **MEMORY CONTROLLER 4-12 BWSCON : ST7, ST6 and DW7 bits**
The typo is corrected and added additional explanation.

WS7	[30]	This bit determines WAIT status for bank 7 **(If bank7 has DRAM or SDRAM, WAIT function is not supported)** 0 = WAIT disable 1 = WAIT enable	0
DW7	[29:28]	These two bits determine data bus width for bank 7 **00** = 8-bit 01 = 16-bit, 10 = 32-bit	0
ST6	[27]	This bit determines SRAM for using UB/LB for bank 6 0 = Not using UB/LB (Pin[14:11] is dedicated nWBE[3:0]) 1 = Using UB/LB (Pin[14:11] is dedicated nBE[3:0])	0
WS6	[26]	This bit determines WAIT status for bank 6 **(If bank6 has DRAM or SDRAM, WAIT function is not supported)** 0 = WAIT disable, 1 = WAIT enable	0

🗁 **CLOCK & POWER MANAGEMENT 5-13 NOTE**
The following note is added.

NOTE: Fpllo must be greater than 20Mhz and less than 66Mhz.

🗁 **DMA CONTROLLER 7-3 Figure 7-2**
The request sources of nXDREQ0/1 and nXACK0/1 are removed.

🗁 DMA CONTROLLER 7-5 Figure 7-5

The figure 7-5 is fixed.

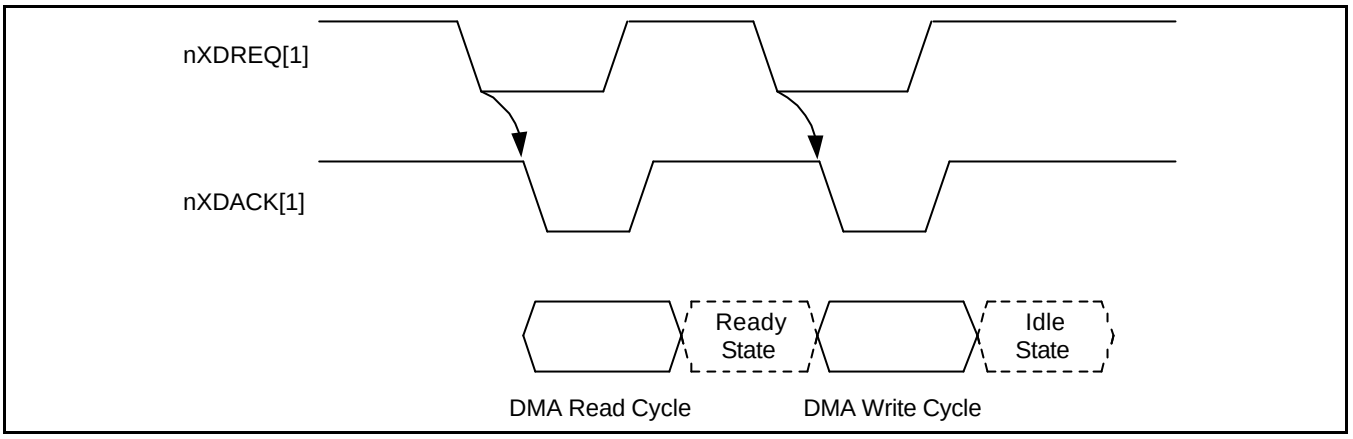

Figure 7-5. Single Step Mode (Case 2)

🗁 DMA CONTROLLER 7-9 Block Transfer Mode

The following note is added.

NOTE: The ADDR[3:0] should be '0' to meet 16-byte align condition in Block Transfer Mode.

🗁 DMA CONTROLLER 7-11 DMA REQUEST SOURCE SELECTION

The request source of nXDREQ0/1 is removed.

🗁 DMA CONTROLLER 7-12 ZDCONn : CMD bits

The descriptions are added additional explanation.

CMD	[1:0]	Software commands 00: No command. After writing 01,10,11, CMD bit is cleared automatically. nXDREQ is available. 01: Starts DMA operation by S/W without nXDREQ. **S/W start function can be used only in the whole mode.** As DMA is in the whole mode, the DMA will operate until the counter is 0. If nXDREQ is used , this command must not be issued. 10: Pauses DMA operation. But nXDREQ is still available. 11: Cancels DMA operation.	00

🗁 DMA CONTROLLER 7-16 BDCONn : CMD bits

The descriptions are changed.

CMD	[1:0]	Software commands 00: No command. After writing 01, 10, 11, CMD bits are cleared automatically. **01: Reserved** **10: Reserved** 11: Cancels DMA operation.	00

🗁 DMA CONTROLLER 7-18 BDIDESn/BDCDESn : TDM bits

The note is added.

TDM	[31:30]	Transfer direction mode 00 = Reserved 01 = M2IO (from external memory to internal peripheral) 10 = IO2M (from internal peripheral to external memory) 11 = IO2IO (from internal peripheral to internal peripheral) **NOTE: The initial value is '00' , but you must change TDM value as another though the BDMA channel is unused.**	00

🗁 DMA CONTROLLER 7-19 BDICNT0/BDCCNT0 and BDICNT1/BDCCNT1 : CMD bits

The descriptions are changed.

BDICNT0/BDCCNT0	Bit	Description	Initial State
QSC	[31:30]	DMA request source selection **00 = N/A** 01 = IIS 10 = UART0 11 = SIO	00

BDICNT1/BDCCNT1	Bit	Description	Initial State
QSC	[31:30]	DMA request source selection **00 = N/A** 01 = Timer 10 = UART1 11 = SIO	00

🗁 I/O PORTS 8-5 PORT CONFIGURATION REGISTER (PCONA-G)

The wakeup signals are changed to PG0-PG7 from PG0-PG0.

🗁 UART CONTROLLER 10-12 UART FIFO STATUS REGISTER

The descriptions are changed.

Delta CTS	**[4]**	This bit indicates that the nCTS input to S3C44B0X has changed state since the last time it was read by CPU. (Refer to Fig. 10-7) 0 = Has not changed 1 = Has changed	0
Reserved	**[3:1]**	Reserved	

.

🗁 INTERRUPT CONTROLLER 11-12 INTERRUPT MASK REGISTER (INTMSK)

The following note is added.

IMPORTANT NOTE : INTMSK register can be masked only when it is sure that the corresponding interrupt does not be requested. If your application should mask any interrupt mask bit(INTMSK) just when the corresponding interrupt is issued, please contact our FAE(field application engineer).

🗁 LCD CONTROLLER 12-26 Example 1

The calculations of LCD load in system are changed .

🗁 A/D CONVERTER 13-1 Revision schedule

Cancel the schedule of 8-bit ADC revision.

🗁 A/D CONVERTER 13-1 Change some features

The max integral linearity error(Max. ± 3 LSB) is added.
The conversion rate is changed from 500KSPS to 100KSPS.
The input voltage range(0~2.5V) is added.
The input bandwidth is added(0~100Hz).

🗁 A/D CONVERTER 13-2 A/D Conversion Time

A/D Conversion time and note are changed like below,

66 MHz / 2(20+1) / 16(at least 16 cycle by 10-bit operation) = 98.2 KHz = 10.2 us

NOTE: Because this A/D converter has no sample-and-hold circuit, analog input frequency should not exceed 100Hz for accurate conversion although the maximum conversion rate is 100KSPS.

🗁 A/D CONVERTER 13-3 Sleep Mode

The programming notes are removed.

🗁 A/D CONVERTER 13-3 External reference pin configuration

Fig. 13-2 is changed.

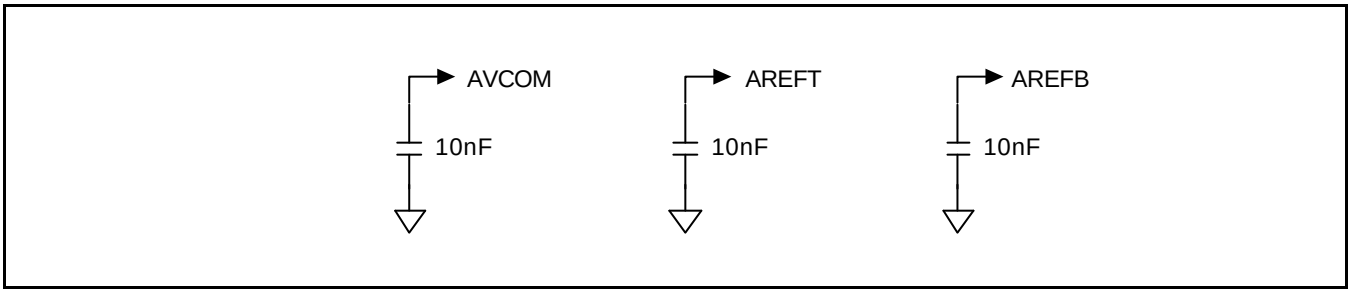

Figure 13-2. External reference pin configuration

🗁 A/D CONVERTER 13-4 The Programming Technique in ADC

The programming technique is added.

🗁 IIS-BUS INTERFACE 17-7 IIS FIFO CONTROL REGISTER (IISFCON)

The below descriptions are added.

To start IIS operation, the following procedure is needed.

1) Enable the FIFO in IISFCON register
2) Enable DMA request in IISCON register
3) Enable IIS interface start in IISCON register

To end IIS operation, the following procedure is needed.

1) Disable the FIFO. If you want to transmit the data remained in FIFO, you must not disable the FIFO and skip this step 1.
2) Disable DMA request in IISCON register.
3) Disable DMA Disable IIS interface start in IISCON register

🗁 IIS-BUS INTERFACE 17-7 IIS PRESCALER REGISTER (IISPSR)

The descriptions are changed and inserted additional explanation table.

IISPSR	Bit	Description	Initial State
Prescaler value A	[7:4]	prescaler division factor for the prescaler A *clock_prescaler_A = MCLK/<division factor>*	0x0
Prescaler value B	[3:0]	prescaler division factor for the prescaler B *clock_prescaler_B = MCLK/<division factor>*	0x0

IISPSR[3:0] / [7:4]	Division Factor	IISPSR[3:0] / [7:4]	Division Factor
0000b	2	1000b	1
0001b	4	1001b	-
0010b	6	1010b	3*
0011b	8	1011b	-
0100b	10	1100b	5*
0101b	12	1101b	-
0110b	14	1110b	7*
0111b	16	1111b	-

NOTES: 1.If the prescaler value is 3,5,7, the duty is not 50%. In this case, the H duration is 0.5 MCLK.

🗁 INTERRUPT CONTROLLER 11-14,11-20 F_ISPR REGISTER

There has been no F_ISPR register in S3C44B0X. The F_ISPR is removed.

ERRATA from S3C44B0X User's Manual Revision 1

MEMORY CONTROLLER 4-3 Programming Memory Controller
The typo is corrected.

```
ldr     r0, =SMRDATA
ldmia   r0, {r1-r13}
ldr     r0, =0x01c80000         ;       BWSCON Address
stmia   r0, {r1-r13}
```

DMA CONTROLLER 7-8 Figure 7-9
The figure 7-9 is fixed.

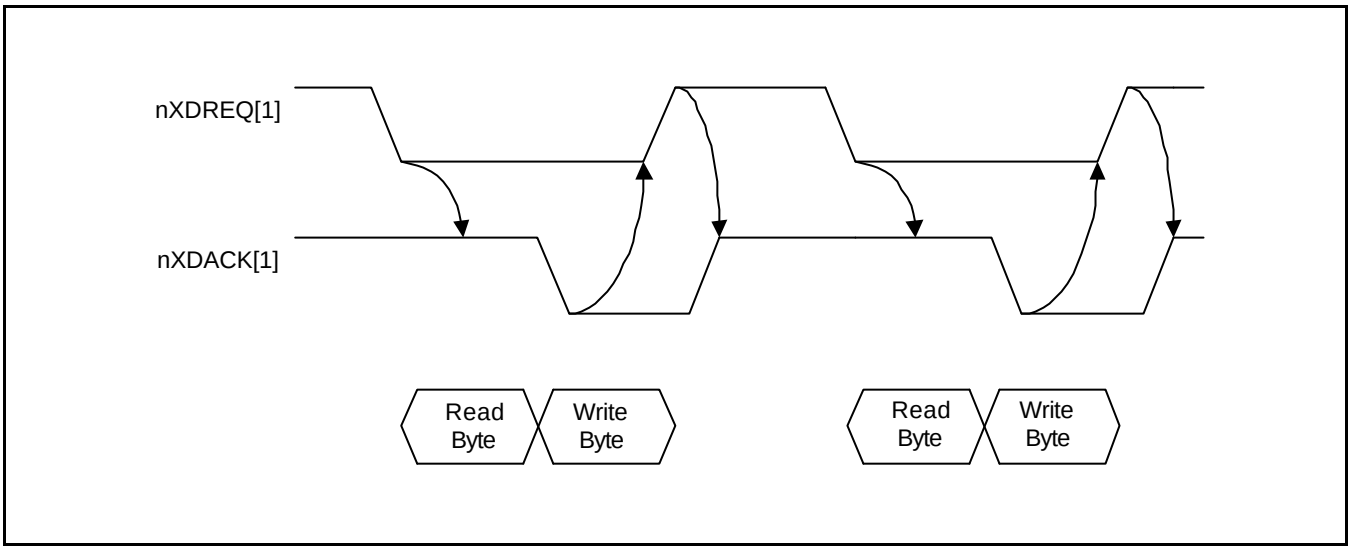

Figure 7-9. Unitary Transfer Mode with Handshake mode

IIC-BUS INTERFACE 16-11 MULTI-MASTER IIC-BUS CONTROL REGISTER(IICCON)
The following note is added.

NOTES:
1. Interfacing with EEPROM, the ack generation may be disabled before reading the last data in order to generate the STOP condition in Rx mode.
2. A IIC-bus interrupt occurs 1)when a 1-byte transmit or receive operation is completed, 2)when a general call or a slave address match occurs, or 3) if bus arbitration fails.
3. To time the setup time of IICSDA before IISSCL rising edge, IICDS has to be written before clearing the IIC interrupt pending bit.
4. IICCLK is determined by IICCON[6].
   Tx clock can vary by SCL transition time.
   When IICCON[6]=0, IICCON[3:0]=0x0 or 0x1 is not available.
5. If the IICON[5]=0, IICON[4] does not operate correctly.
   So, It is recommended to set IICCON[5]=1, although you does not use the IIC interrupt.

🗁 CLOCK & POWER MANAGEMENT 5-5 PLL Lock Time

The typo is corrected.

The lock time should be bigger than **208**us.

🗁 PRODUCT OVERVIEW 1-3 A/D Converter

The typo is corrected.

Max. **100KSPS**/10-bit.

🗁 SIO 18-7 Figure SIO Timing diagram

The typo is corrected.

Figure 18-7 SIO in **Non-**Hand-Shaking Mode Timing diagram(Auto Run Mode)

🗁 DMA CONTROLLER 7-12 ZDCONn : INT bits

These bits are changed to reserved.

INT	[7:6]	**Reserved**	00

🗁 DMA CONTROLLER 7-15 ZDICNTn : EN bit

The note is added.

EN	[20]	DMA H/W enable/disable 0 = Disable DMA 1 = Enable DMA. If the QDS bit is 00b, DMA request can be serviced. Also if the S/W command is Start, the DMA operation will occur. If the EN bit is 0, DMA will not operate even though S/W command is Start. If the S/W Command is Cancel, the DMA operation will be canceled and EN bit will be cleared to 0. At the terminal count, the EN bit will be cleared to 0. **NOTE:** Do not set the EN bit and the other bits of ZDICNT register at the same time. User have to set EN bit after setting the other bits of ZDICNT register as following steps, 1. Set ZDICNT register with disabled En bit. 2. Set EN bit enable.	00

🗁 DMA CONTROLLER 7-16 BDCONn : INT bits

These bits are changed to reserved.

INT	[7:6]	**Reserved**	00

🗁 DMA CONTROLLER 7-19,20 BDICNTn : EN bit

The note is added.

EN	[20]	DMA H/W enable/disable 0 = Disable DMA 1 = Enable DMA. If the QDS bit is 00b, DMA request can be serviced. Also if the S/W command is Start, the DMA operation will occur. If the EN bit is 0, DMA will not operate even though S/W command is Start. If the S/W Command is Cancel, the DMA operation will be canceled and EN bit will be cleared to 0. At the terminal count, the EN bit will be cleared to 0. **NOTE:** Do not set the EN bit and the other bits of BDICNT register at the same time. User have to set EN bit after setting the other bits of BDICNT register as following steps, 1. Set BDICNT register with disabled En bit. 2. Set EN bit enable.	00

🗁 SIO 18-8 SIOCON : SIO start bit

The description is changed.

SIO start	[3]	This bit determines whether the SIO functions is running or has stopped. **(When BDMA Tx is used, this bit should be ' 0' .)** 0 = No action 1 = Clear 3-bit counter and start shit. This bit is cleared just after writing this bit as 1.	0

🗁 SIO 18-3 Flag Run Mode

The SIORDY signal can' t be used for SIO handshake signal.

There is problem in SIORDY function. If SIORDY is negated just when the one DMA(Memory to SIO, SIO to Memory) transfer operation is completed, the next DMA operation will not occurred although the SIORDY signal is asserted.

🗁 PRODUCT OVERVIEW 1-11,12 Table1-1 I/O State @Initial

The DATA[31:0] state is changed.

Pin No.	Pin Name	Default Function	I/O State(2) @BUS REQ.	I/O State(2) @STOP	I/O State @Initial	I/O TYPE(6)
xxx	DATA[31:0]	DATA[31:0]	Hi-z	Hi-z	**I**	phbsu50ct12sm

🗁 PWM TIMER 9-15,16,17,18,19 TCMPBn

The note is added.

TCMPBn	Bit	Description	Initial State
Timer n compare buffer register	[15:0]	Setting compare buffer value for Timer n **NOTE:** This value must be smaller than TCNTBn value.	0x00000000

🗁 ELECTRICAL DATA 19-2 Table19-3. Normal I/O PAD DC Electrical Characteristics

The typo is corrected.

Symbol	Parameters	Condition	Min	Typ	Max	Unit
I_{DD}	Operating current				1.2	mA/**MHz**

🗁 ELECTRICAL DATA 19-14 Figure 19-16. External nWAIT READ Timing

The typo is corrected Tacs as **Tcos**, which is the parameter of nOE signal.

🗁 CLOCK & POWER MANAGEMENT 5-8 STOP Mode

The following important notes are added.

4) If STOP mode is issued, CPU will enter into STOP mode after 16 X-tal clocks. If the wake-up is asserted for the 14th clocking duration among 16 clocks, S3C44B0X will never respond to any wake-up signaling. It' s strongly recommended that any wake-up signals should not be asserted until entering into STOP mode completely.

5) When S3C44B0X enters STOP mode, MCLK should be more than 2.5 times of Fin (X-tal frequency). After wake-up (in NORMAL mode), user can change MCLK to the frequency that user want. For example, if Fin is 20MHz and a user want MCLK=36MHz, the MCLK before entering into STOP mode should be more than 50MHz. After wake-up and S3C44B0X returns to NORMAL mode from STOP mode, MCLK can be changed from 50MHz to 36MHz by setting PLLCON register.

6) When S3C44B0X enters STOP mode in the level triggered EINT mode, the level EINT wake-up should not be active. If the level EINT wake-up is active, S3C44B0X should skip entering into STOP mode.

🗁 CLOCK & POWER MANAGEMENT 5-4 Usual Condition for PLL & Clock Generator

The feedback 1Mohm resister is added.

Loop filter capacitance	700-820 pF
Feedback resistance	**1Mohm**
External X-tal frequency	6-20 Mhz
External capacitance used for X-tal	15-22 pF

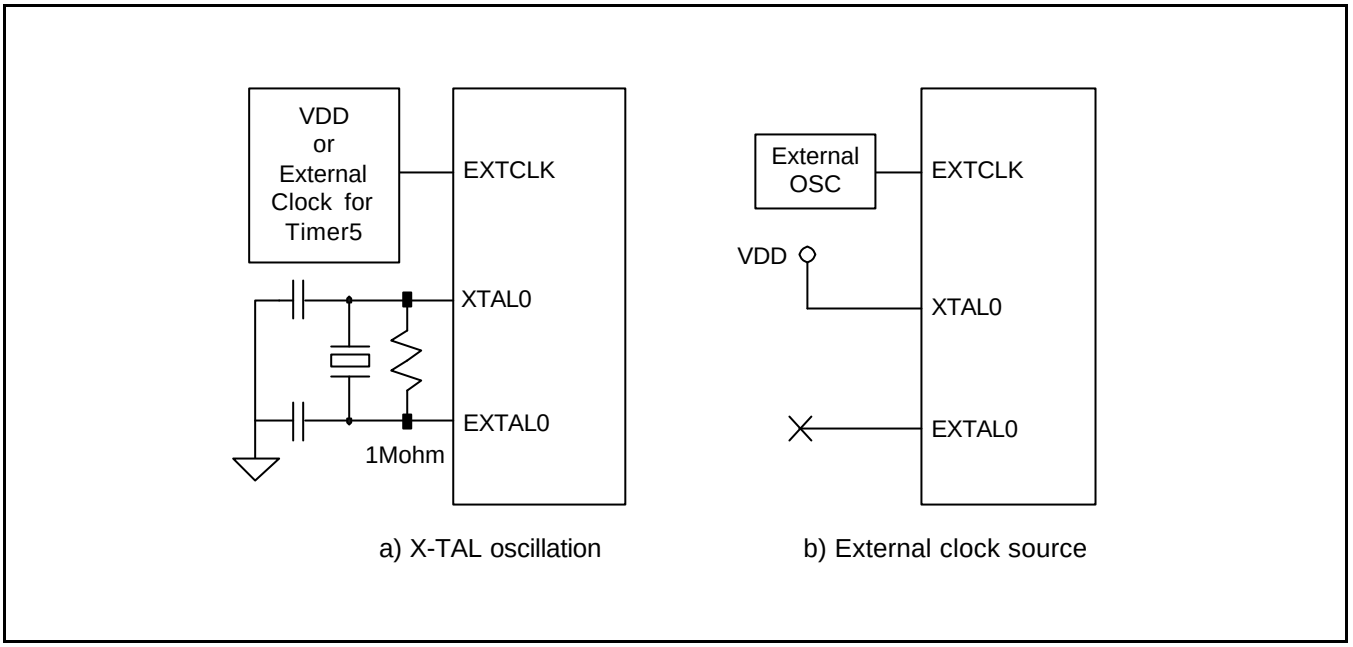

Figure 5-3. Main Oscillator Circuit Examples

🗁 RTC(Real Time Clock) 14-10 TICK TIME COUNT REGISTER(TICNT)

The typo is corrected.

Register	Address	R/W	Description	Reset Value
TICNT	0x01D7008C(L) 0x01D7008**F**(B)	R/W (by byte)	Tick time count Register	0x00000000

🗁 LCD CONTROLLER 12-4 TIMING GENERATOR

A sentence is modified as follow.

In case of 4-bit dual scan display the number of valid VD data line should be 4 and in case of 8-bit signal scan display mode, the number of valid VD data lines should be 8.

🗁 DMA CONTROLLER 7-13 ZDMA0 INITIAL SOURCE/DESTINATION ADDRESS AND COUNT REGISTERS

The typos are corrected.

(ZDISRC**0**, ZDIDES**0**, ZDICNT**0**)