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M02013

CMOS Transimpedance Amplifier with AGC Intended for Fiber-optic Networks up to 3.2 Gbps Data Sheet

TABLE OF CONTENTS

3.2 Gbps CMOS Transimpedance Amplifier with AGC

FEATURES

- Typical -23 dBm sensitivity, +3 dBm saturation at 3.2 Gbps (-24 dBm at 2.5 Gbps) when used with 0.9 A/W InGaAs PINs. (Cpd ≤ 0.5 pF BER 10^{-10})
- Typical differential transimpedance: 10 kΩ
- Fabricated in CMOS
- Differential output
- Operates with standard +3.3 Volt supply
- Available as die only
- Monitor Output
- AGC provides dynamic range of more than 25 dBm

APPLICATIONS

- ATM/SDH/SONET
- 2x Fiber Channel

DESCRIPTION

The M02013 is a transimpedance amplifier (TIA) with AGC manufactured in a sub-micron, CMOS process. The AGC allows more than 25 dBm of dynamic range, providing a low-cost solution for longer-reach 3.2 Gbps ATM/SONET systems.

For optimum system performance, the M02013 die should be mounted with a silicon or InGaAs PIN photodetector inside a lensed TO-Can or other optical sub-assembly.

The M02013 reverse biases the PIN by approximately 1.8 volts to optimise performance.

A replica of the average photodiode current is available at the MON pad for alignment and 'LOSS of SIGNAL' monitoring.

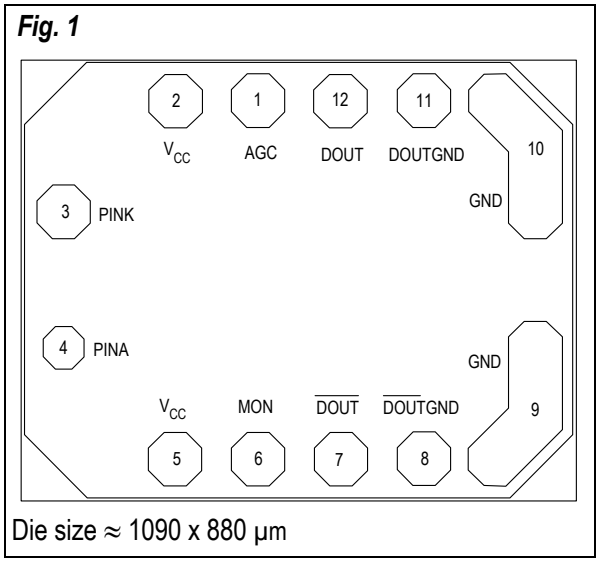
TABLE 1 ORDERING INFORMATION

Part	Pin Package
M02013-XX *	Waffle Pack
M02013-XX *	Expanded whole wafer on a ring

* For full ordering number please contact sales

CONNECTIONS

Fig. 1



Die size ≈ 1090 x 880 µm

TOP LEVEL DIAGRAM

Fig. 2

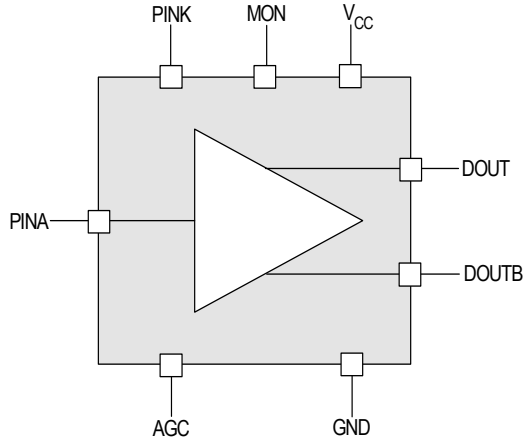


TABLE 2 PAD DESCRIPTION

Die Pad No	Name	Function
1	AGC	Monitor or force AGC voltage. Enable self test oscillator when V_{AGC} >V_{CC}+1.2
2	V_{CC}	Power pin. Connect to most positive supply
3	PINK	AC common PIN input. Connect photo diode cathode here and a 470 pF capacitor to Gnd (1)
4	PINA	Active PIN input. Connect photo diode anode here
5	V_{CC}	Power pin. Connect to most positive supply (only one V_{CC} pad needs to be connected)
6	MON	Analog current sink output. Current matched to average photodiode current
7	$\overline{\text{DOUT}}$	Differential data output (goes low as light increases)
8	$\overline{\text{DOUT}}$GND	Ground return for $\overline{\text{DOUT}}$ pad (all GND pads must be connected)
9	GND	Ground pin. Connect to the most negative supply (all GND pads must be connected)
10	GND	Ground pin. Connect to the most negative supply (all GND pads must be connected)
11	DOUTGND	Ground return for DOUT pad (all GND pads must be connected)
12	DOUT	Differential data output (goes high as light increases)
NA	Backside	Backside. Connect to the lowest potential, usually ground

Note: (1) Alternatively the photodiode cathode may be connected to a decoupled positive supply e.g. V_{CC}.

TABLE 3 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Units
V_{CC}	Power supply (V_{CC}-GND)	4	V
T_A	Operating ambient	-40 to +85	°C
T_{STG}	Storage temperature	-65 to +150	°C

TABLE 4 RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Rating	Units
V_{CC}	Power supply (V_{CC}-GND)	3.3 ± 10%	V
C_{PD}	Max. Photodiode capacitance (V_r = 1.8 V), for 3.2 Gbps data rate	0.5	pF
T_A	Operating ambient temperature	-40 to +85	°C

TABLE 5 DC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Units
V_B	Photodiode bias voltage (PINK - PINA)	1.6	1.8	2	V
V_{CM}	Common mode output voltage	0.7	1	1.3	V
V_{OL} and V_{OH}	Output voltage swing	.45	1	1.55	V
I_{CC}	Supply current (no loads)	31	42	58	mA
R_{LOAD}	Recommended differential output loading	85	100 (1)	-	Ω

NOTE (1) 100Ω is the load presented by the input of the Mindspeed M02049 limiting amplifier.

TABLE 6 AC CHARACTERISTICS

Symbol	Parameter	Min.	Typ. (2)	Max.	Units
R_{OUT}	Output impedance (single ended)	25	40	60	Ω
LFC	Low frequency cutoff	-	50	80	KHz
V_D	Differential output voltage	-	275	500	mV
DCD	Duty cycle distortion	-	-	20	ps
DJ	Deterministic jitter (includes DCD)	-	-	35	ps, p-p
In, rms	Total input RMS noise, DC to 2.3 GHz, Cin = 0.5 pF	-	475	600	nA
Pin	Example dynamic range of optical input 3	-22	-	+3	dBm
PIN (mean), min	Optical Sensitivity 3 at 3.2 Gbps	-	-23	-	dBm
PIN (mean), min	Optical Sensitivity 3 at 2.5 Gbps	-	-24	-	dBm

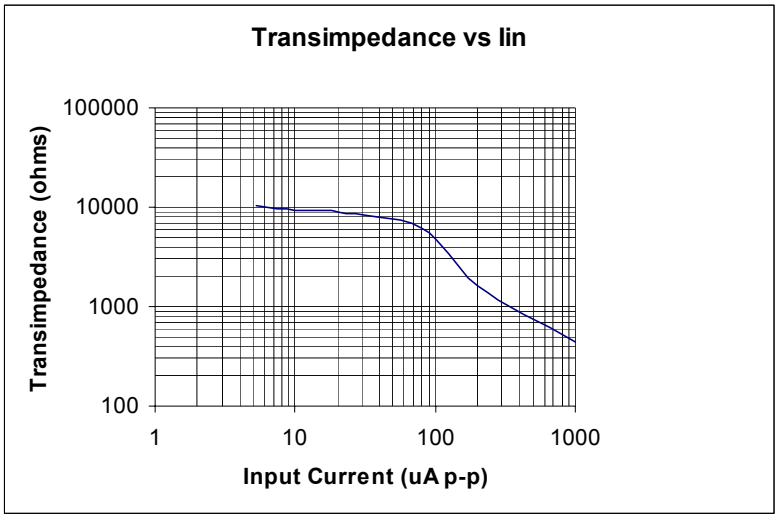
NOTE (2) Die designed to operate over an ambient temperature range of -40 °C to +85 °C, T_A and V_{CC} range from 3.0 - 3.6V. Typical values are tested at T_A = 25° C and Vcc = 3.3V.
NOTE (3) BER 10^{-10}, PD capacitance = 0.5 pF, Responsivity 0.9 A/W, Extinction Ratio = 10.

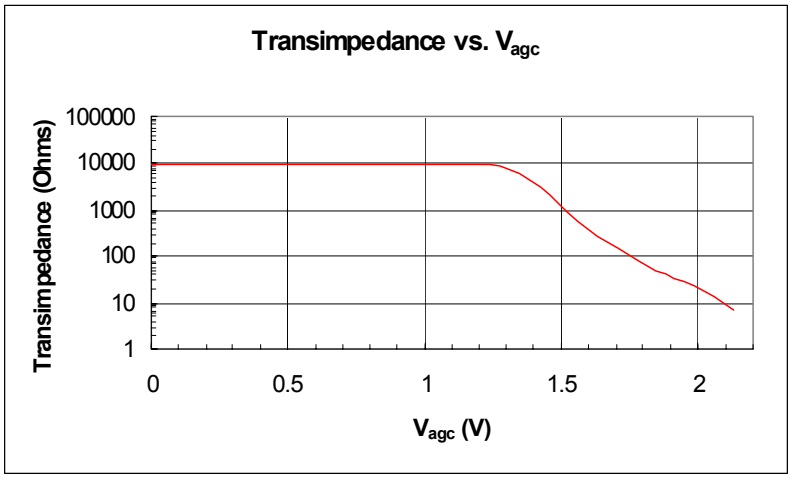
TABLE 7 DYNAMIC CHARACTERISTICS

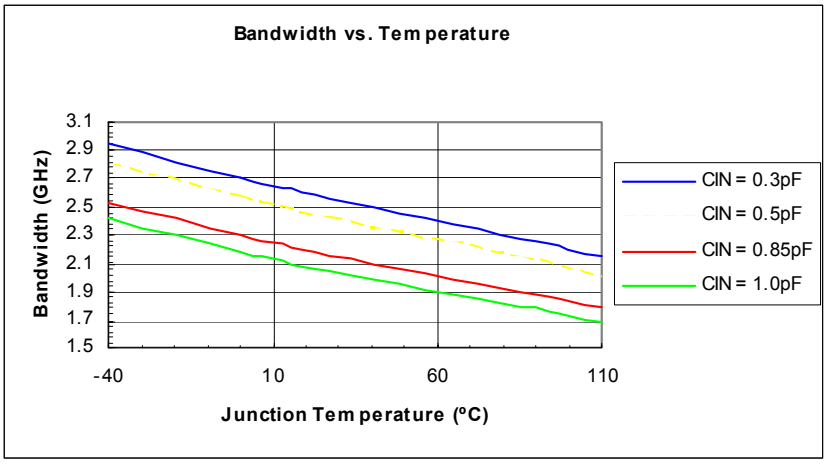
Symbol	Parameter	Min.	Typ.	Max.	Units
G	Transimpedance - Single ended - Differential	 3.5 7	 5 10	 7 14	KΩ
BW	Bandwidth to -3 dB point @ -22 dBm, 0.9A/W, 0.5 pF PD	2.0	2.4	-	GHz
RC	AGC loop time constant	-	2	-	µs
I_{AGC}	AGC threshold	30			µA, p-p
PSRR	Power supply rejection, f < 4 MHz	20	28	-	dB

TYPICAL PERFORMANCE

Fig. 3.



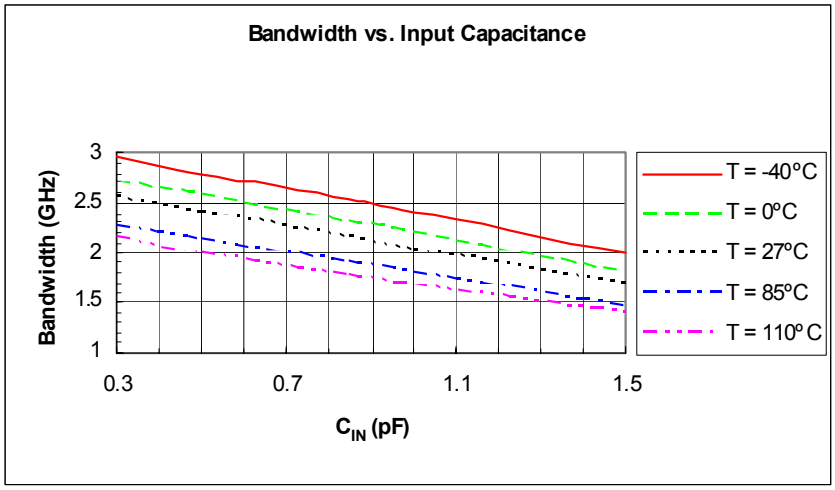


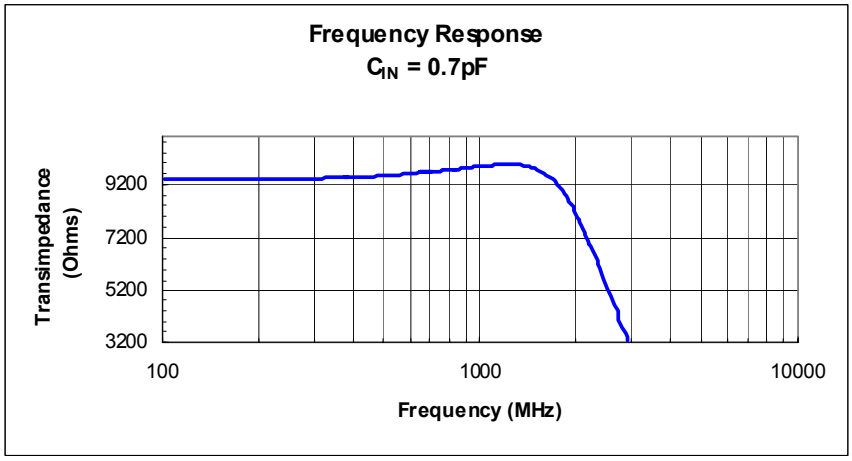


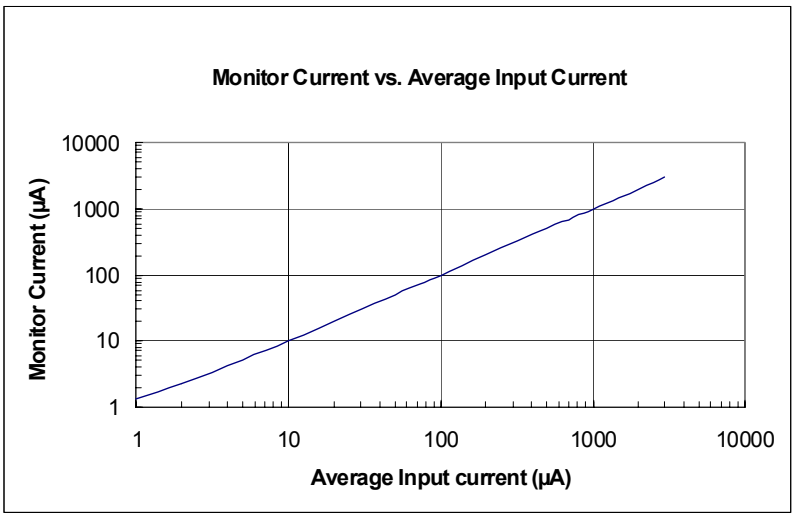
Note: *Vcc = 3.3V, Temperature = 25 °C, Lin = 1 nH, unless otherwise stated, TIA gain is differential.*

TYPICAL PERFORMANCE (CONT.)

Fig. 3 (cont.)



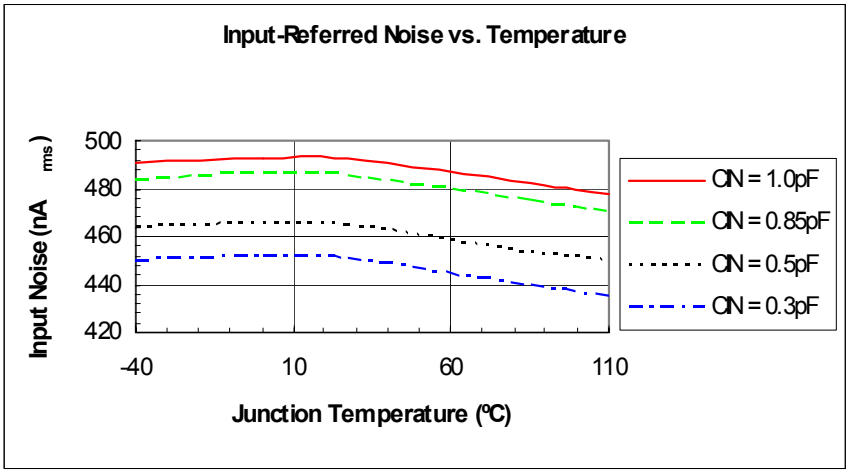


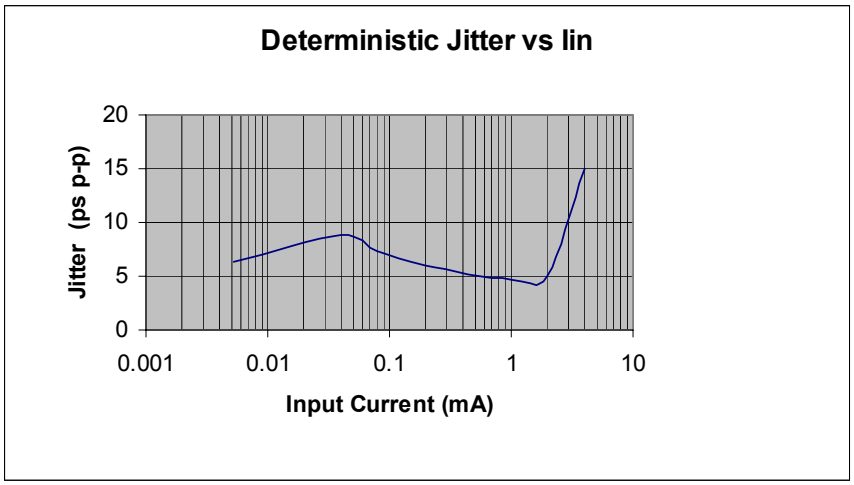


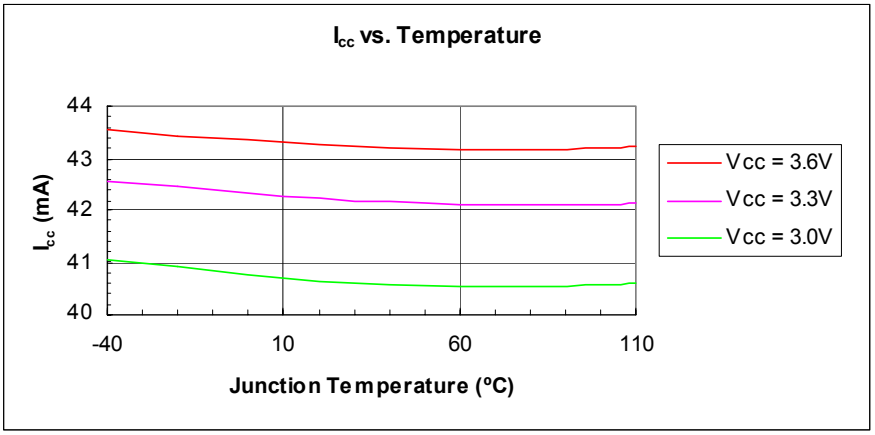
Note: *Vcc = 3.3V, Temperature = 25 °C, Lin = 1 nH, unless otherwise stated, TIA gain is differential.*

TYPICAL PERFORMANCE (CONT.)

Fig. 3 (cont.)

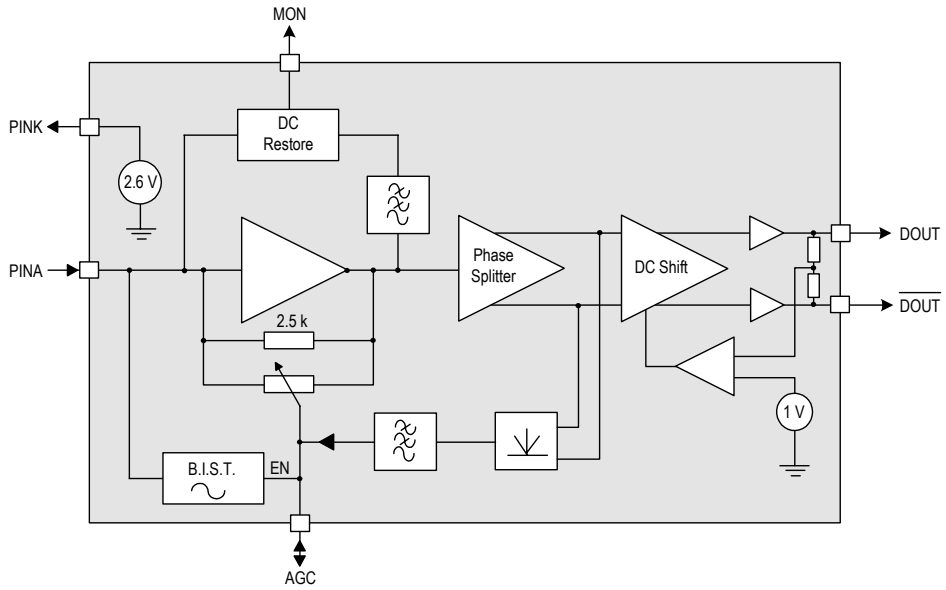






FUNCTIONAL DIAGRAM

Fig. 4



FUNCTIONAL DESCRIPTION

TIA (Transimpedance Amplifier)

The transimpedance amplifier consists of a high gain single-ended CMOS amplifier (TIA), with a feedback resistor. The feedback creates a virtual earth low impedance at the input and virtually all of the input current passes through the feedback resistor, defining the voltage at the output. Advanced CMOS design techniques are employed to maintain the stability of this stage across all input conditions.

Single-ended amplifiers have inherently poor power supply noise rejection. For this reason, an on-chip low dropout linear regulator has been incorporated into the design to give excellent noise rejection up to several MHz. Higher frequency power supply noise is removed by the external 470 pF decoupling capacitor connected to PINK.

The circuit is designed for PIN photodiodes in the "grounded cathode" configuration, with the anode connected to the input of the TIA and the cathode connected to AC ground, such as the provided PINK terminal. Reverse DC bias is applied to reduce the photodiode capacitance. Avalanche photodiodes can be connected externally to a higher voltage.

AGC

The M02013 has been designed to operate over the input range of +3 dBm to –23 dBm @ 3.2 Gbps and –24 dBm @ 2.5 Gbps. This represents a ratio of 1:300, whereas the acceptable dynamic range of the output is only 1:30 which implies a compression of 10:1 in the transimpedance. The design uses a MOS transistor operating in the triode region as a "voltage controlled resistor" to achieve the transimpedance variation.

Another feature of the AGC is that it only operates on signals greater than –17.5 dBm (@ 0.9 A/W). This knee in the gain response is important when setting "signal detect" functions in the following post amplifier. It also aids in active photodiode alignment.

The AGC pad allows the AGC to be disabled during photodiode alignment by grounding the pad through a low impedance. The AGC control voltage can be monitored during normal operation at this pad by a high impedance (>10 MΩ) circuit. In addition, taking this pad to V_{CC} +1.2 V enables an internal test oscillator which supplies a 1 MHz 10 µApp (approximate) square wave current internally into the PINA pad to emulate a photodiode for test purposes.

Output Stage

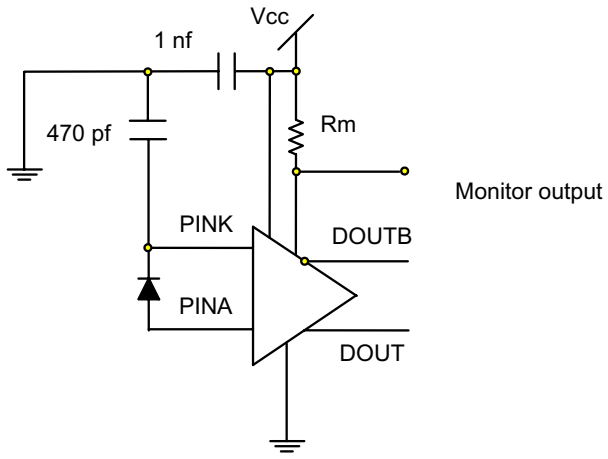
The signal from the TIA enters a phase splitter followed by a DC-shift stage and a pair of voltage follower outputs. These are designed to drive a differential (100 Ω) load. They are stable for driving capacitive loads, such as interstage filters. Each output has its own GND pad, all four GND pads on the chip should be connected for proper operation. Since the M02013 exhibits rapid roll-off (3 pole), simple external filtering is sufficient.

Monitor O/P

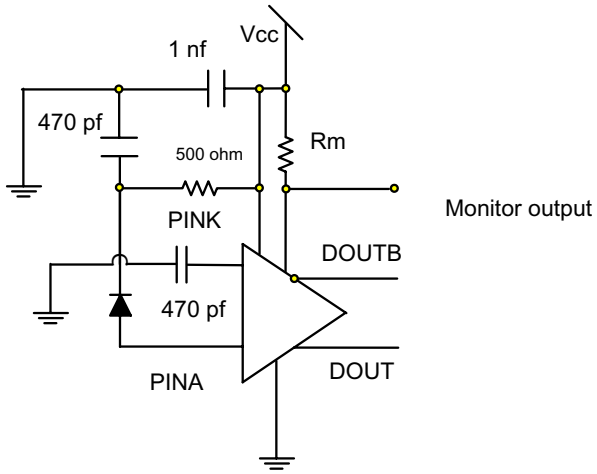
High impedance O/P sinks replicate average photodiode current for monitoring purposes.

SUGGESTED PIN DIODE CONNECTION METHODS

Fig. 5



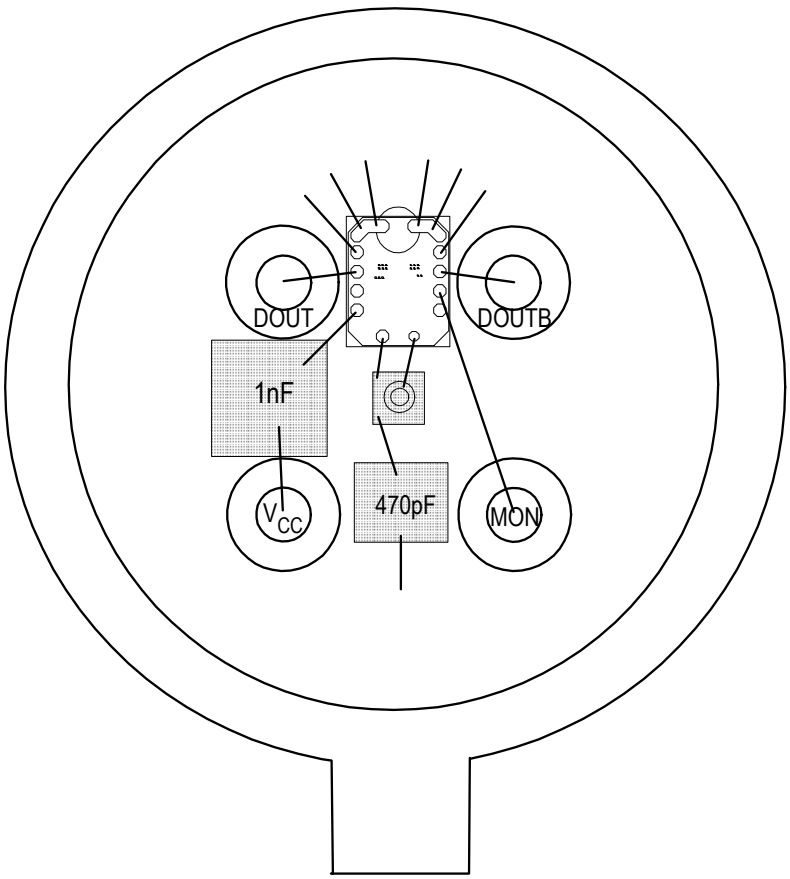
Recommended Circuit



Alternative Circuit (Cathode Connected to Vcc)

TYPICAL APPLICATION DIAGRAM

Fig. 6



Notes:
Typical application inside of a five lead TO-Can.
Only one of the V_{CC} pads and all of the GND pads need to be connected. The backside must be connected to the lowest potential, usually ground, with conductive epoxy or a similar die attach material.

Assembly

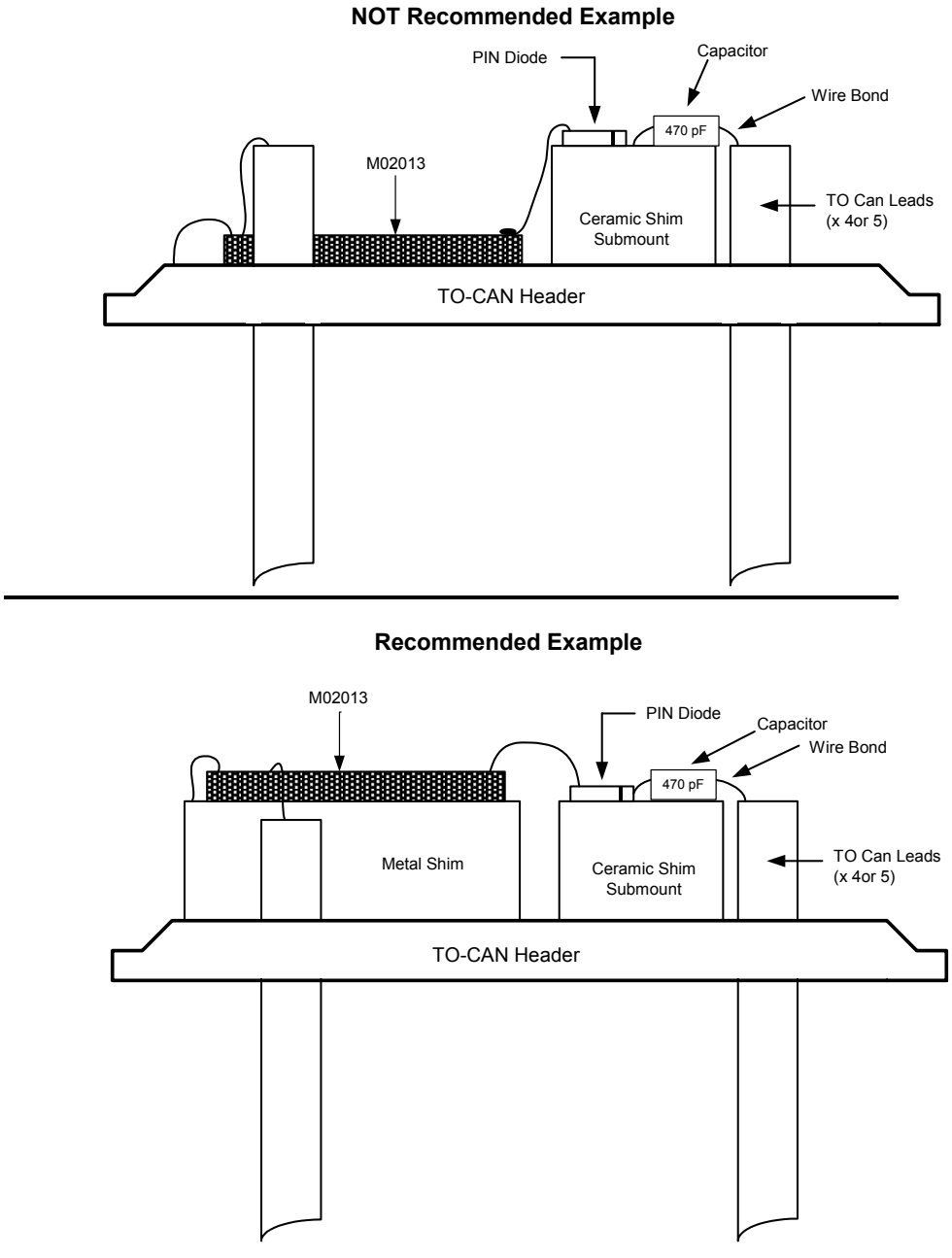
The M02013 is designed to work with a wirebond inductance of 1 nh +/- 0.25 nh. Many existing TO-Can configurations will not allow wirebond lengths that short, since the PIN diode submount and the TIA die are more than 1 mm away in the vertical direction, due to the need to have the PIN diode in the correct focal plane. This can be remediated by raising up the TIA die with a conductive metal shim. This will effectively reduce the bond wire length. Refer to Figure 5 on the following page for details. Mindspeed recommends ball bonding with a 1 mil (24.4 µm) gold wire.

In addition, please refer to the Mindspeed Product Bulletin (document number 0201X-PBD-001). Care must be taken when selecting chip capacitors, since they must have good low ESR characteristics up to 1.6 Ghz. It is also important that the termination materials of the capacitor be compatible with the attach method used.

For example, Tin/Lead (Pb/Sn) solder finish capacitors are incompatible with silver-filled epoxies. Palladium/ Silver (Pd/Ag) terminations are compatible with silver filled epoxies. Solder can be used only if the substrate thick-film inks are compatible with Pb/Sn solders.

TO-CAN ASSEMBLY DIAGRAM

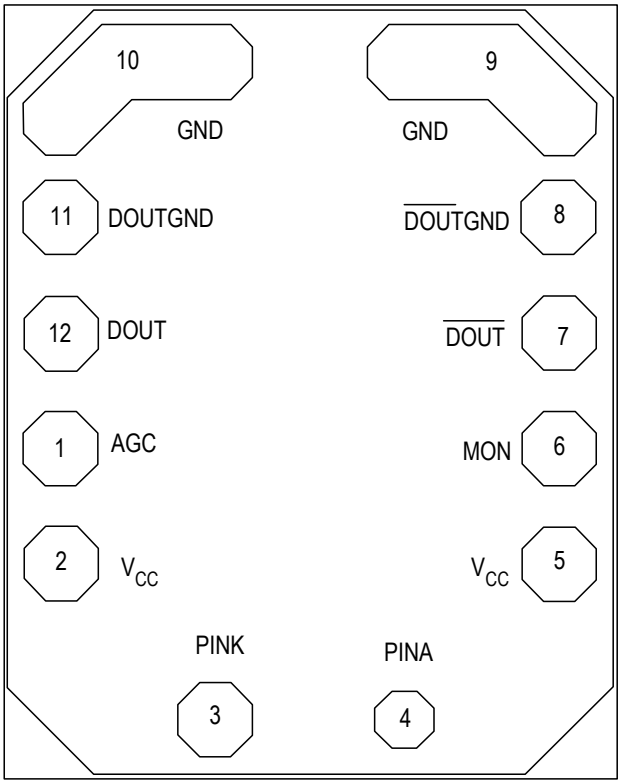
Fig. 7



BARE DIE INFORMATION

BARE DIE LAYOUT

Fig. 8



Pad Number	Pad	X	Y
1	AGC	-76	329
2	V_{CC}	-228	329
3	PINK	-434	124
4	PINA	-434	-124
5	V_{CC}	-228	-329
6	MON	-76	-329
7	$\overline{DOUT}$	76	-329
8	$\overline{DOUT}$GND	228	-329
9c*	GND	360	-329
9b*	GND	434	-255
9a*	GND	434	-124
10a*	GND	434	124
10b*	GND	434	255
10c*	GND	360	329
11	DOUTGND	228	329
12	DOUT	76	329

Notes:
Process technology: CMOS, Silicon Nitride passivation
Die thickness: 300 µm
Pad metallization: Aluminum
Die size: 1090 µm x 880 µm
Pad opening: 86 µmsq
Octagonal pad: 70 µm across flat PINA (70 µm x 70 µm)
Pad Centers in µm referenced to center of device
Backside bias to ground

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