PRELIMINARY

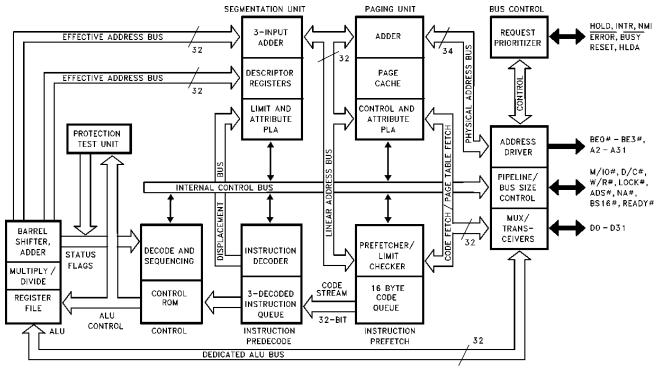
Intel386™ DX MICROPROCESSOR 32-BIT CHMOS MICROPROCESSOR WITH INTEGRATED MEMORY MANAGEMENT (PQFP SUPPLEMENT)

- **Flexible 32-Bit Microprocessor**
  - **— 8, 16, 32-Bit Data Types**
  - **— 8 General Purpose 32-Bit Registers**
- **Very Large Address Space**
  - **— 4 Gigabyte Physical**
  - **— 64 Terabyte Virtual**
  - **— 4 Gigabyte Maximum Segment Size**
- **Integrated Memory Management Unit**
  - **— Virtual Memory Support**
  - **— Optional On-Chip Paging**
  - **— 4 Levels of Protection**
  - **— Fully Compatible with 80286**
- **Object Code Compatible with All 8086 Family Microprocessors**
- **Virtual 8086 Mode Allows Running of 8086 Software in a Protected and Paged System**
- **Hardware Debugging Support**
- **Optimized for System Performance**
  - **— Pipelined Instruction Execution**
  - **— On-Chip Address Translation Caches**
  - **— 20, 25 and 33 MHz Clock**
  - **— 40, 50 and 66 Megabytes/Sec Bus Bandwidth**
- **Numerics Support via Intel387™ DX Math Coprocessor**
- **Complete System Development Support**
  - **— Software: C, PL/M, Assembler System Generation Tools**
  - **— Debuggers: PSCOPE, ICE™-386**
- **High Speed CHMOS IV Technology**
- **132 Pin PQFP Package**
  (See Packaging Specification, Order # 231369)

The Intel386 DX Microprocessor is an entry-level 32-bit microprocessor designed for single-user applications and operating systems such as MS-DOS and Windows. The 32-bit registers and data paths support 32-bit addresses and data types. The processor addresses up to four gigabytes of physical memory and 64 terabytes (2**46) of virtual memory. The integrated memory management and protection architecture includes address translation registers, multitasking hardware and a protection mechanism to support operating systems. Instruction pipelining, on-chip address translation, ensure short average instruction execution times and maximum system throughput.

The Intel386 DX CPU offers new testability and debugging features. Testability features include a self-test and direct access to the page translation cache. Four new breakpoint registers provide breakpoint traps on code execution or data accesses, for powerful debugging of even ROM-based systems.

Object-code compatibility with all 8086 family members (8086, 8088, 80186, 80188, 80286) means the Intel386 DX offers immediate access to the world's largest microprocessor software base.



Intel386™ DX Pipelined 32-Bit Microarchitecture

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MS-DOS and Windows are Trademarks of MICROSOFT Corporation.

January 1994 **Order Number: 241267-003**

Intel386™ DX Microprocessor High-Performance 32-Bit CHMOS Microprocessor with Integrated Memory Management (PQFP Supplement)

CONTENTS

CONTENTS

This document should be used in conjunction with the Intel386™ DX Microprocessor data sheet (order number 231630-011, October 1993).

1.0 PIN ASSIGNMENT

The Intel386 DX pinout as viewed from the top side of the component is shown by Figure 1-1.

V_{CC} and GND connections must be made to multiple V_{CC} and V_{SS} (GND) pins. Each V_{CC} and V_{SS} must be connected to the appropriate voltage level. The circuit board should include V_{CC} and GND planes for power distribution and all V_{CC} and V_{SS} pins must be connected to the appropriate plane.

NOTE:
Pins identified as "N.C." should remain completely unconnected.

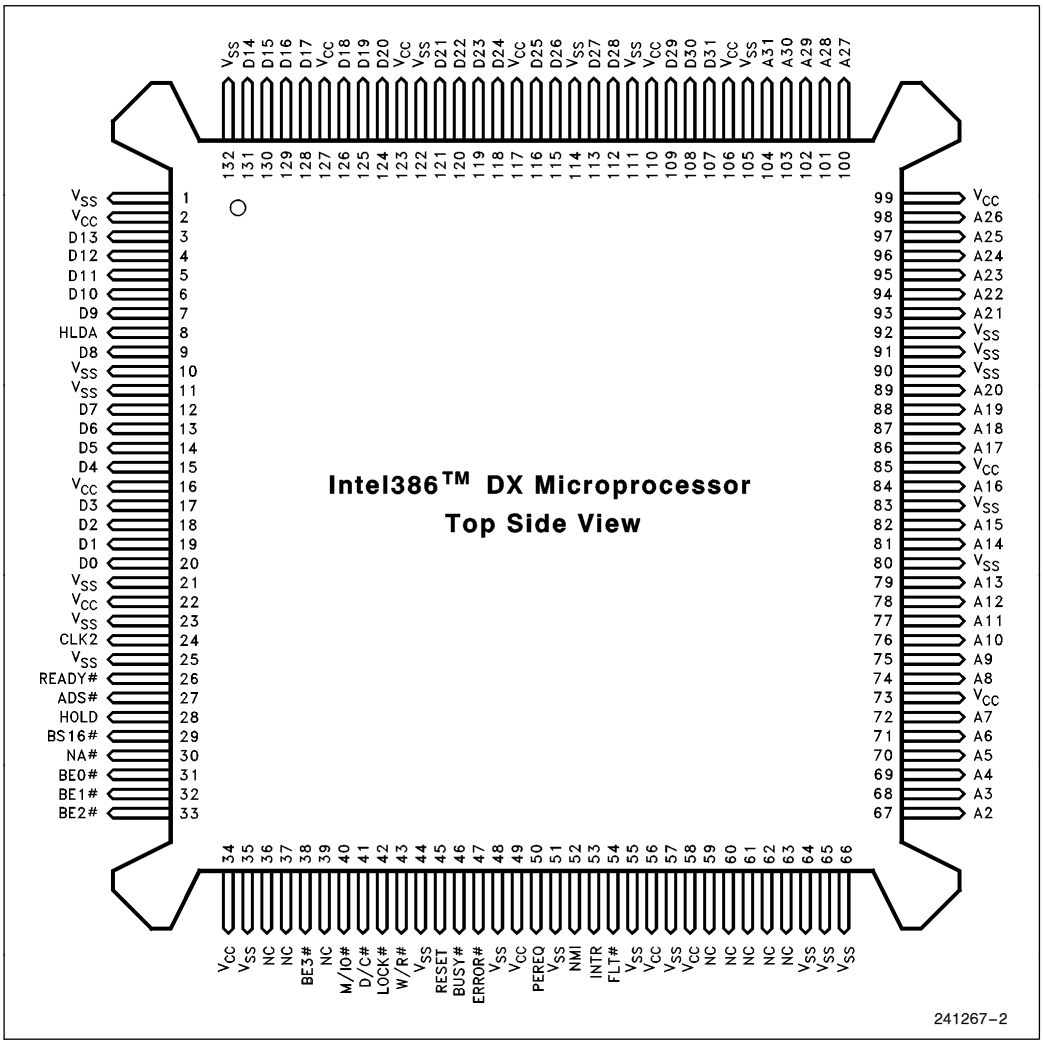


Figure 1-1. Intel386™ DX PQFP Pinout—View from Top Side

Table 1-1. Intel386™ DX PQFP Pinout—Functional Grouping

Address		Data		Control		N/C	V_{SS}	V_{CC}
A2	67	D0	20	ADS#	27	36	1	2
A3	68	D1	19	BE0#	31	37	10	16
A4	69	D2	18	BE1#	32	39	11	22
A5	70	D3	17	BE2#	33	59	21	34
A6	71	D4	15	BE3#	38	60	23	49
A7	72	D5	14	BS16#	29	61	25	56
A8	74	D6	13	BUSY#	46	62	35	58
A9	75	D7	12	CLK2	24	63	44	73
A10	76	D8	9	D/C#	41		48	85
A11	77	D9	7	ERROR#	47		51	99
A12	78	D10	6	FLT#	54		55	106
A13	79	D11	5	HLDA	8		57	110
A14	81	D12	4	HOLD	28		64	117
A15	82	D13	3	INTR	53		65	123
A16	84	D14	131	LOCK#	42		66	127
A17	86	D15	130	M/IO#	40		80	
A18	87	D16	129	NA#	30		83	
A19	88	D17	128	NMI	52		90	
A20	89	D18	126	PEREQ	50		91	
A21	93	D19	125	READY#	26		92	
A22	94	D20	124	RESET	45		105	
A23	95	D21	121	W/R#	43		111	
A24	96	D22	120				114	
A25	97	D23	119				122	
A26	98	D24	118				132	
A27	100	D25	116					
A28	101	D26	115					
A29	102	D27	113					
A30	103	D28	112					
A31	104	D29	109					
		D30	108					
		D31	107					

1.1 Pin Description Table

The following table lists a brief description of each pin on the Intel386 DX. The following definitions are used in these descriptions:

- # The named signal is active LOW.
- I Input signal.
- O Output signal.
- I/O Input and Output signal.
- — No electrical connection.

Symbol	Type	Name and Function
CLK2	I	**CLK2** provides the fundamental timing for the Intel386 DX.
$D_{31}-D_0$	I/O	**DATA BUS** inputs data during memory, I/O and interrupt acknowledge read cycles and outputs data during memory and I/O write cycles.
$A_{31}-A_2$	O	**ADDRESS BUS** outputs physical memory or port I/O addresses.
BE0#–BE3#	O	**BYTE ENABLES** indicate which data bytes of the data bus take part in a bus cycle.
W/R#	O	**WRITE/READ** is a bus cycle definition pin that distinguishes write cycles from read cycles.
D/C#	O	**DATA/CONTROL** is a bus cycle definition pin that distinguishes data cycles, either memory or I/O, from control cycles which are: interrupt acknowledge, halt, and instruction fetching.
M/IO#	O	**MEMORY I/O** is a bus cycle definition pin that distinguishes memory cycles from input/output cycles.
LOCK#	O	**BUS LOCK** is a bus cycle definition pin that indicates that other system bus masters are denied access to the system bus while it is active.
ADS#	O	**ADDRESS STATUS** indicates that a valid bus cycle definition and address (W/R#, D/C#, M/IO#, BE0#, BE1#, BE2#, BE3# and $A_{31}-A_2$) are being driven at the Intel386 DX pins.
NA#	I	**NEXT ADDRESS** is used to request address pipelining.
READY#	I	**BUS READY** terminates the bus cycle.
BS16#	I	**BUS SIZE 16** input allows direct connection of 32-bit and 16-bit data buses.
HOLD	I	**BUS HOLD REQUEST** input allows another bus master to request control of the local bus.

1.1 Pin Description Table (Continued)

Symbol	Type	Name and Function
HLDA	O	**BUS HOLD ACKNOWLEDGE** output indicates that the Intel386 DX has surrendered control of its local bus to another bus master.
BUSY#	I	**BUSY** signals a busy condition from a processor extension.
ERROR#	I	**ERROR** signals an error condition from a processor extension.
PEREQ	I	**PROCESSOR EXTENSION REQUEST** indicates that the processor extension has data to be transferred by the Intel386 DX.
FLT#	I	**FLOAT** is an input which forces all bidirectional and output signals, including HLDA, to the tri-state condition. This allows the electrically isolated 386 DX PQFP to use On-Circuit Emulation (ONCE) directly on the motherboard. The FLT# pin has an internal pull-up resistor; if the FLT# pin is not used, it should not be connected.
INTR	I	**INTERRUPT REQUEST** is a maskable input that signals the Intel386 DX to suspend execution of the current program and execute an interrupt acknowledge function.
NMI	I	**NON-MASKABLE INTERRUPT REQUEST** is a non-maskable input that signals the Intel386 DX to suspend execution of the current program and execute an interrupt acknowledge function.
RESET	I	**RESET** suspends any operation in progress and places the Intel386 DX in a known reset state. See **Interrupt Signals** for additional information.
N/C	—	**NO CONNECT** should always remain unconnected. Connection of a N/C pin may cause the processor to malfunction or be incompatible with future steppings of the Intel386 DX.
V_{CC}	I	**SYSTEM POWER** provides the +5V nominal D.C. supply input.
V_{SS}	I	**SYSTEM GROUND** provides 0V connection from which all inputs and outputs are measured.

1.2 Float Pin Description

Activating the FLT# input floats all Intel386 DX bidirectional and output signals, including HLDA. Asserting FLT# isolates the Intel386 DX microprocessor from the surrounding circuitry.

Packaged in a surface mount PQFP, it cannot be removed from the motherboard when In-Circuit Emulation (ICE) is needed. The FLT# input allows the Intel386 CPU to be electrically isolated from the surrounding circuitry. This allows connection of an emulator to the processor without removing it from the PCB. This method of emulation is referred to as ON-Circuit Emulation (ONCE).

ENTERING AND EXITING FLOAT

FLT# is an asynchronous, active-low input. It is recognized on the rising edge of CLK2. When recognized, it aborts the current bus cycle and floats the outputs of the processor (Figure 1-2). FLT# must be held low for a minimum of 16 CLK2 cycles. Reset should be asserted and held asserted until after FLT# is deasserted. This will ensure that the Intel386 DX CPU will exit float in a valid state.

Asserting the FLT# input unconditionally aborts the current bus cycle and forces the processor into the FLOAT mode, and is therefore not guaranteed to enter FLOAT in a valid state. After deactivating FLT#, the processor is not guaranteed to exit FLOAT mode in a valid state. This is not a problem as the FLT# pin is meant to be used only during ONCE. After exiting FLOAT, the processor must be reset to return it to a valid state. Reset should be asserted before FLT# is deasserted. This will ensure that the processor will exit float in a valid state.

FLT# has an internal pull-up resistor, and if it is not used it should be unconnected.

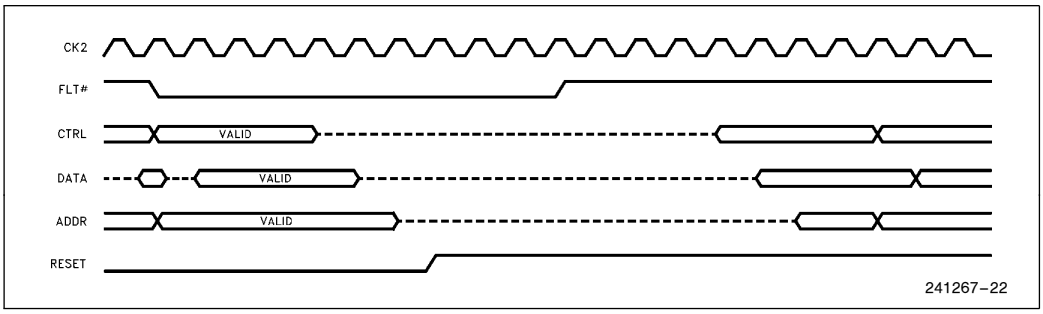


Figure 1-2. Entering and Exiting, FLT#

2.0 MECHANICAL DATA

2.1 Package Dimensions

The Intel386 DX is available in a 132 lead plastic quad flat pack (PQFP) package. Table 2.1 and Figures 2.1–2.5 show the physical dimensions of this package.

Table 2.1. Intel Case Outline Dimensions for 132 Lead Plastic Quad Flat Pack 0.025 Inch Pitch

Symbol	Description	Inch		mm	
		Min	Max	Min	Max
A	Package Height	0.160	0.170	4.06	4.32
A1	Standoff	0.020	0.030	0.51	0.76
D, E	Terminal Dimension	1.075	1.085	27.31	27.56
D1, E1	Package Body	0.947	0.953	24.05	24.21
D2, E2	Bumper Distance	1.097	1.103	27.86	28.02
D3, E3	Lead Dimension	0.800 REF		20.32 REF	
L1	Foot Length	0.020	0.030	0.51	0.76
Issue	IWS Preliminary 1/15/87				

Symbol List

Letter or Symbol	Description of Dimensions
A	Package Height: Distance from Seating Plane to Highest Point of Body
A1	Standoff: Distance from Seating Plane to Base Plane
D/E	Overall Package Dimension: Lead Tip to Lead Tip
D1/E1	Plastic Body Dimension
D2/E2	Bumper Distance
D3/E3	Footprint
L1	Foot Length

NOTES:
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Datum plane H located at the mold parting line and coincident with the bottom of the lead where lead exits plastic body.
3. Datums A B and D to be determined where center leads exit plastic body at datum plane H.
4. Controlling Dimension, Inch.
5. Dimensions D1, D2, E1, and E2 are measured at the mold parting line and do not include mold protrusion. Allowable mold protrusion is 0.18 mm (0.007 in) per side.
6. Pin 1 identifier is located within one of the two zones indicated.

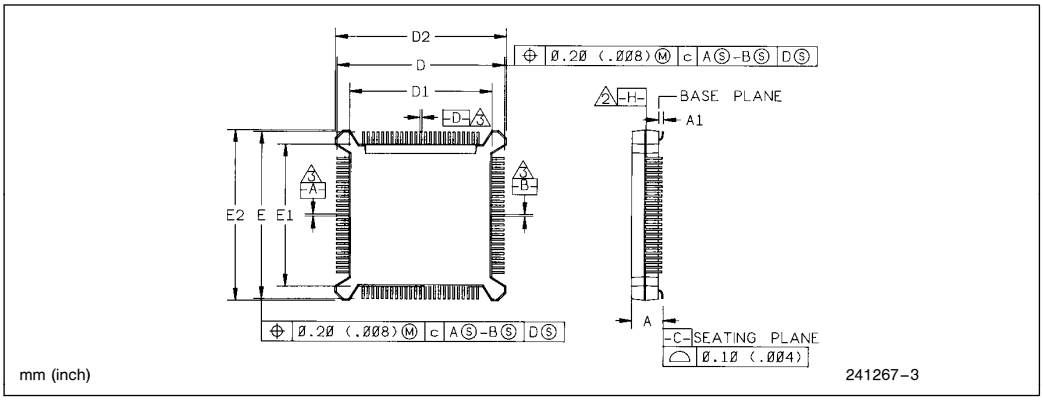


Figure 2.1. Principal Dimensions and Datums

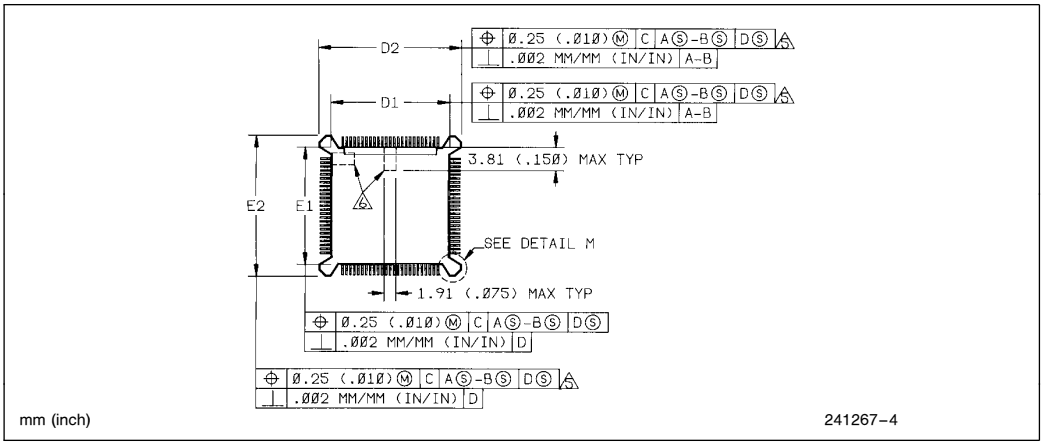


Figure 2.2. Molded Details

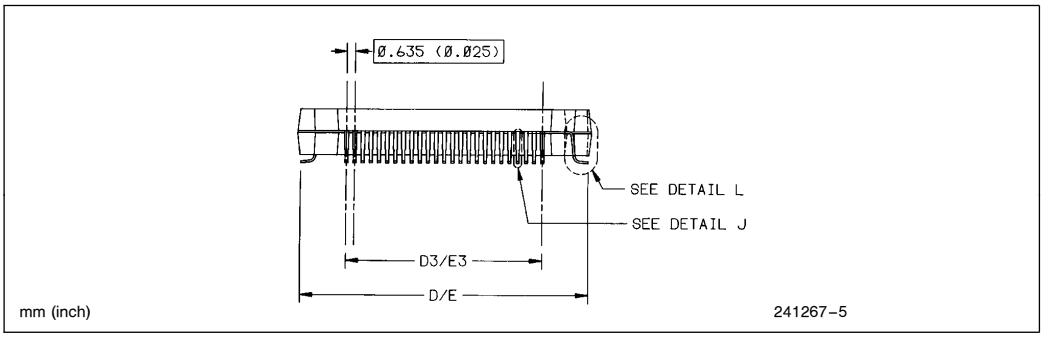


Figure 2.3. Terminal Details

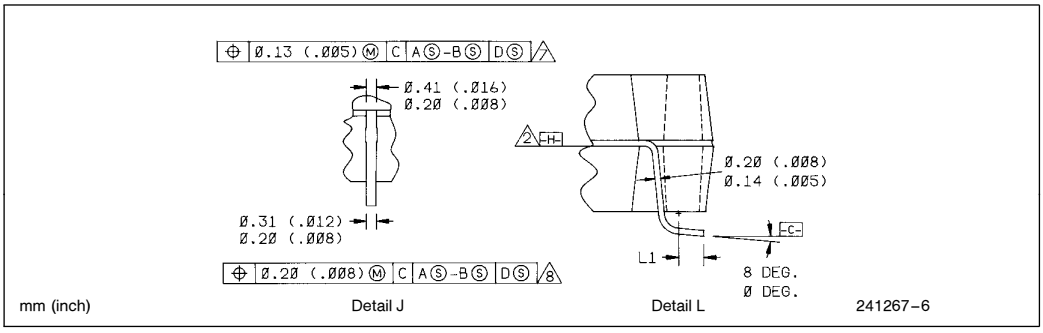


Figure 2.4. Typical Lead

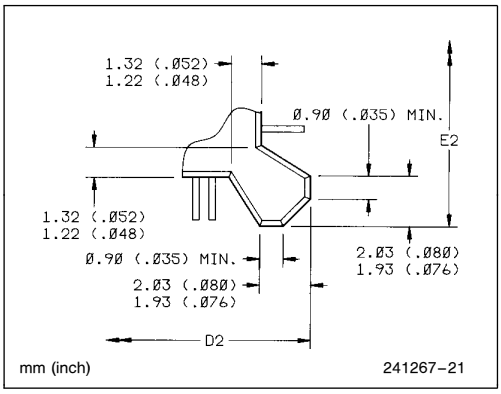


Figure 2.5. Detail M

2.2 Package Thermal Specifications

The Intel386 DX Microprocessor is specified for operation when case temperature is within the range of 0°C–100°C. The case temperature may be measured in any environment, to determine whether the Intel386 DX Microprocessor is within specified operating range. The case temperature should be measured at the center of the top surface.

The ambient temperature is guaranteed as long as T_c is not violated. The ambient temperature can be calculated from the θ_{jc} and θ_{ja} from the following equations:

$$T_j = T_c + P^*\theta_{jc}$$

$$T_a = T_j - P^*\theta_{ja}$$

$$T_c = T_a + P^*[\theta_{ja} - \theta_{jc}]$$

Values for θ_{ja} and θ_{jc} are given in Table 2.2 for the 100 lead fine pitch. θ_{ja} is given at various airflows. Table 2.3 shows the maximum T_a allowable (without exceeding T_c) at various airflows.

Table 2.2. Thermal Resistances (°C/Watt) θ_{jc} and θ_{ja}

Package	θjc	θ_{ja} versus Airflow - ft/min (m/sec)					
		0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
132 Lead PQFP	9.0	31.0	24.5	21.5	19.0	17.0	16.0

Table 2.3. Maximum T_a at various airflows

Package	Frequency	T_A(°C) versus Airflow - ft/min (m/sec)					
		0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
132 Lead PQFP	20 MHz	71	79	83	87	89	90
	25 MHz	65	75	80	84	87	89
	33 MHz	60	72	78	82	85	87

NOTE:
The numbers in Table 2.3 were calculated using worst case I_{CC} at T_C = 100°C with the outputs unloaded.

3.0 D.C./A.C. SPECIFICATIONS

Table 3-1. Maximum Ratings

Parameter	Intel386™ DX 20, 25, 33 MHz Maximum Rating
Storage Temperature	−65°C to +150°C
Case Temperature Under Bias	−65°C to +110°C
Supply Voltage with Respect to V_{SS}	−0.5V to +6.5V
Voltage on Other Pins	−0.5V to V_{CC} + 0.5V

Table 3-1 is a stress rating only, and functional operation at the maximums is not guaranteed. Functional operating conditions are given in **3.1 D.C. Specifications** and **3.2 A.C. Specifications**.

Extended exposure to the Maximum Ratings may affect device reliability. Furthermore, although the Intel386 DX contains protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

3.1 D.C. Specifications

Functional Operating Range: V_{CC} = 5V ±5%; T_{CASE} = 0°C to +100°C

Table 3-2. Intel386™ DX D.C. Characteristics

Symbol	Parameter	Intel386™ DX 20 MHz, 25 MHz, 33 MHz		Unit	Test Conditions
		Min	Max		
V_{IL}	Input Low Voltage	−0.3	0.8	V	(Note 1)
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3	V	
V_{ILC}	CLK2 Input Low Voltage	−0.3	0.8	V	(Note 1)
V_{IHC}	CLK2 Input High Voltage 20 MHz 25 MHz and 33 MHz	 V_{CC} − 0.8 3.7	 V_{CC} + 0.3 V_{CC} + 0.3	 V V	
V_{OL}	Output Low Voltage I_{OL} = 4 mA: A2–A31, D0–D31 I_{OL} = 5 mA: BE0#–BE3#, W/R#, D/C#, M/IO#, LOCK#, ADS#, HLDA	 	 0.45 0.45	 V V	
V_{OH}	Output High Voltage I_{OH} = 1 mA: A2–A31, D0–D31 I_{OH} = 0.9 mA: BE0#–BE3#, W/R#, D/C#, M/IO#, LOCK#, ADS#, HLDA	 2.4 2.4	 	 V V	
I_{LI}	Input Leakage Current (For All Pins except BS16#, PEREQ, BUSY#, and ERROR#)		±15	μA	0V ≤ V_{IN} ≤ V_{CC}
I_{IH}	Input Leakage Current (PEREQ Pin)		200	μA	V_{IH} = 2.4V (Note 2)
I_{IL}	Input Leakage Current (BS16#, BUSY#, and ERROR# Pins)		−400	μA	V_{IL} = 0.45 (Note 3)
I_{LO}	Output Leakage Current		±15	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
I_{CC}	Supply Current CLK2 = 40 MHz: with 20 MHz Intel386™ DX CLK2 = 50 MHz: with 25 MHz Intel386™ DX CLK2 = 66 MHz: with 33 MHz Intel386™ DX	 	(Note 4) 260 320 390	 mA mA mA	 I_{CC} Typ. = 200 mA I_{CC} Typ. = 240 mA I_{CC} Typ. = 300 mA
C_{IN}	Input or I/O Capacitance		10	pF	F_C = 1 MHz
C_{OUT}	Output Capacitance		12	pF	F_C = 1 MHz
C_{CLK}	CLK2 Capacitance		20	pF	F_C = 1 MHz

NOTES:
1. The min value, −0.3, is not 100% tested.
2. PEREQ input has an internal pulldown resistor.
3. BS16#, BUSY# and ERROR# inputs each have an internal pullup resistor.
4. CHMOS IV Technology.

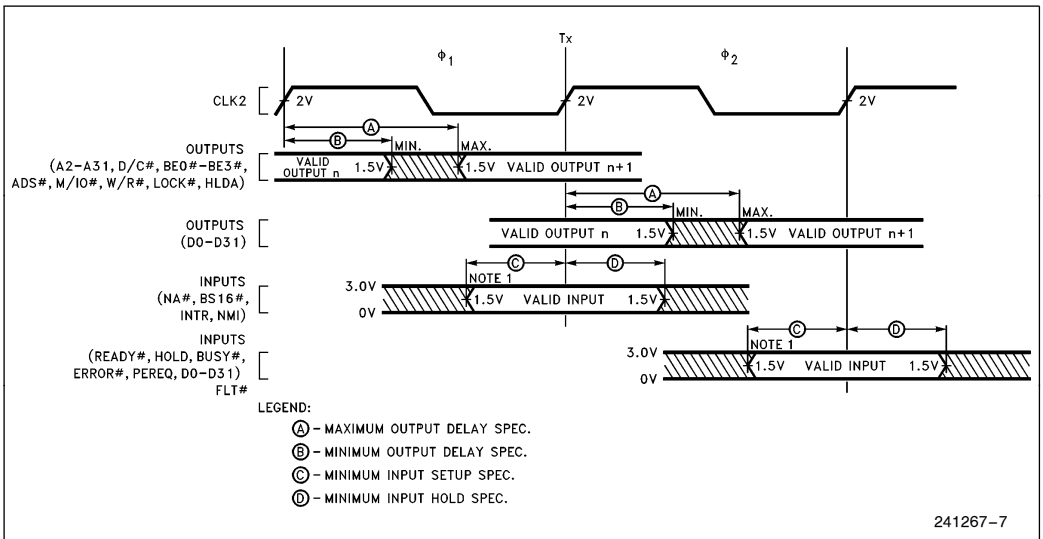
3.2 A.C. SPECIFICATIONS

3.2.1 A.C. Spec Definitions

The A.C. specifications, given in Tables 3-3, 3-4, and 3-5, consist of output delays, input setup requirements and input hold requirements. All A.C. specifications are relative to the CLK2 rising edge crossing the 2.0V level.

A.C. spec measurement is defined by Figure 3-1. Inputs must be driven to the voltage levels indicated by Figure 3-1 when A.C. specifications are measured. Intel386 DX output delays are specified with minimum and maximum limits, measured as shown. The minimum Intel386 DX delay times are hold times provided to external circuitry. Intel386 DX input setup and hold times are specified as minimums, defining the smallest acceptable sampling window. Within the sampling window, a synchronous input signal must be stable for correct Intel386 DX operation.

Outputs NA#, W/R#, D/C#, M/IO#, LOCK#, BE0#–BE3#, A2–A31 and HLDA only change at the beginning of phase one. D0–D31 (write cycles) only change at the beginning of phase two. The READY#, HOLD, BUSY#, ERROR#, PEREQ and D0–D31 (read cycles) inputs are sampled at the beginning of phase one. The NA#, BS16#, INTR and NMI inputs are sampled at the beginning of phase two.



NOTES:
1. Input waveforms have tr ≤ 2.0 ns from 0.8V to 2.0V.
2. See section 9.5.8 for typical output rise time versus load capacitance.

Figure 3-1. Drive Levels and Measurement Points for A.C. Specifications

3.2.2 A.C. SPECIFICATION TABLES

Functional Operating Range: $V_{CC} = 5V \pm 5\%$; $T_{CASE} = 0°C$ to $+100°C$

Table 3-3. 33 MHz Intel386™ DX A.C. Characteristics

Symbol	Parameter	33 MHz Intel386™ DX		Unit	Ref. Fig.	Notes
		Min	Max			
	Operating Frequency	8	33.3	MHz		Half of CLK2 Frequency
t1	CLK2 Period	15.0	62.5	ns	3-3	
t2a	CLK2 High Time	6.25		ns	3-3	at 2V
t2b	CLK2 High Time	4.5		ns	3-3	at 3.7V
t3a	CLK2 Low Time	6.25		ns	3-3	at 2V
t3b	CLK2 Low Time	4.5		ns	3-3	at 0.8V
t4	CLK2 Fall Time		4	ns	3-3	3.7V to 0.8V (Note 3)
t5	CLK2 Rise Time		4	ns	3-3	0.8V to 3.7V (Note 3)
t6	A2–A31 Valid Delay	4	15	ns	3-5	$C_L = 50$ pF
t7	A2–A31 Float Delay	4	20	ns	3-6	(Note 1)
t8	BE0#–BE3#, LOCK# Valid Delay	4	15	ns	3-5	$C_L = 50$ pF
t9	BE0#–BE3#, LOCK# Float Delay	4	20	ns	3-6	(Note 1)
t10	W/R#, M/IO#, D/C#, Valid Delay	4	15	ns	3-5	$C_L = 50$ pF
t10a	ADS# Valid Delay	4	14.5	ns	3-5	$C_L = 50$ pF
t11	W/R#, M/IO#, D/C#, ADS# Float Delay	4	20	ns	3-6	(Note 1)
t12	D0–D31 Write Data Valid Delay	7	24	ns	3-5a	$C_L = 50$ pF, (Note 4)
t12a	D0–D31 Write Data Hold Time	2			3-5b	$C_L = 50$ pF
t13	D0–D31 Float Delay	4	17	ns	3-6	(Note 1)
t14	HLDA Valid Delay	4	20	ns	3-6	$C_L = 50$ pF
t15	NA# Setup Time	5		ns	3-4	
t16	NA# Hold Time	2		ns	3-4	
t17	BS16# Setup Time	5		ns	3-4	
t18	BS16# Hold Time	2		ns	3-4	
t19	READY# Setup Time	7		ns	3-4	
t20	READY# Hold Time	4		ns	3-4	

3.2.2 A.C. SPECIFICATION TABLES (Continued)

Functional Operating Range: $V_{CC} = 5V \pm 5\%$; $T_{CASE} = 0°C$ to $+100°C$

Table 3-3. 33 MHz Intel386™ DX A.C. Characteristics (Continued)

Symbol	Parameter	33 MHz Intel386™ DX		Unit	Ref. Fig.	Notes
		Min	Max			
t21	D0–D31 Read Setup Time	5		ns	3-4	
t22	D0–D31 Read Hold Time	3		ns	3-4	
t23	HOLD Setup Time	11		ns	3-4	
t24	HOLD Hold Time	2		ns	3-4	
t25	RESET Setup Time	5		ns	3-7	
t26	RESET Hold Time	2		ns	3-7	
t27	NMI, INTR Setup Time	5		ns	3-4	(Note 2)
t28	NMI, INTR Hold Time	5		ns	3-4	(Note 2)
t29	PEREQ, ERROR#, FLT#, BUSY# Setup Time	5		ns	3-4	(Note 2)
t30	PEREQ, ERROR#, FLT#, BUSY# Hold Time	4		ns	3-4	(Note 2)

NOTES:

1. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not 100% tested.
2. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.
3. Rise and fall times are not tested.
4. Min. time not 100% tested.

3.2.2 A.C. SPECIFICATION TABLES (Continued)

Functional Operating Range: $V_{CC} = 5V \pm 5\%$; $T_{CASE} = 0°C$ to $+100°C$

Table 3-4. 25 MHz Intel386™ DX A.C. Characteristics

Symbol	Parameter	25 MHz Intel386™ DX		Unit	Ref. Fig.	Notes
		Min	Max			
	Operating Frequency	4	25	MHz		Half of CLK2 Frequency
t1	CLK2 Period	20	125	ns	3-3	
t2a	CLK2 High Time	7		ns	3-3	at 2V
t2b	CLK2 High Time	4		ns	3-3	at 3.7V
t3a	CLK2 Low Time	7		ns	3-3	at 2V
t3b	CLK2 Low Time	5		ns	3-3	at 0.8V
t4	CLK2 Fall Time		7	ns	3-3	3.7V to 0.8V
t5	CLK2 Rise Time		7	ns	3-3	0.8V to 3.7V
t6	A2–A31 Valid Delay	4	21	ns	3-5	$C_L = 50$ pF
t7	A2–A31 Float Delay	4	30	ns	3-6	(Note 1)
t8	BE0#–BE3# Valid Delay	4	24	ns	3-5	$C_L = 50$ pF
t8a	LOCK# Valid Delay	4	21	ns	3-5	$C_L = 50$ pF
t9	BE0#–BE3#, LOCK# Float Delay	4	30	ns	3-6	(Note 1)
t10	W/R#, M/IO#, D/C#, ADS# Valid Delay	4	21	ns	3-5	$C_L = 50$ pF
t11	W/R#, M/IO#, D/C#, ADS# Float Delay	4	30	ns	3-6	(Note 1)
t12	D0–D31 Write Data Valid Delay	7	27	ns	3-5a	$C_L = 50$ pF
t12a	D0–D31 Write Data Hold Time	2			3-5b	$C_L = 50$ pF
t13	D0–D31 Float Delay	4	22	ns	3-6	(Note 1)
t14	HLDA Valid Delay	4	22	ns	3-6	$C_L = 50$ pF
t15	NA# Setup Time	7		ns	3-4	
t16	NA# Hold Time	3		ns	3-4	
t17	BS16# Setup Time	7		ns	3-4	
t18	BS16# Hold Time	3		ns	3-4	
t19	READY# Setup Time	9		ns	3-4	
t20	READY# Hold Time	4		ns	3-4	

3.2.2 A.C. SPECIFICATION TABLES (Continued)

Functional Operating Range: $V_{CC} = 5V \pm 5\%$; $T_{CASE} = 0°C$ to $+100°C$

Table 3-4. 25 MHz Intel386™ DX A.C. Characteristics (Continued)

Symbol	Parameter	25 MHz Intel386™ DX		Unit	Ref. Fig.	Notes
		Min	Max			
t21	D0–D31 Read Setup Time	7		ns	3-4	
t22	D0–D31 Read Hold Time	5		ns	3-4	
t23	HOLD Setup Time	15		ns	3-4	
t24	HOLD Hold Time	3		ns	3-4	
t25	RESET Setup Time	10		ns	3-7	
t26	RESET Hold Time	3		ns	3-7	
t27	NMI, INTR Setup Time	6		ns	3-4	(Note 2)
t28	NMI, INTR Hold Time	6		ns	3-4	(Note 2)
t29	PEREQ, ERROR#, FLT#, BUSY# Setup Time	6		ns	3-4	(Note 2)
t30	PEREQ, ERROR#, FLT#, BUSY# Hold Time	5		ns	3-4	(Notes 2, 3)

NOTES:

1. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not 100% tested.
2. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.
3.

	Symbol	Parameter	Min
$T_C = 0°C$	t30	PEREQ, ERROR#, FLT#, BUSY# Hold Time	4
$T_C = +100°C$	t30	PEREQ, ERROR#, FLT#, BUSY# Hold Time	5

3.2.2 A.C. SPECIFICATION TABLES (Continued)

Functional Operating Range: $V_{CC} = 5V \pm 5\%$; $T_{CASE} = 0°C$ to $+100°C$

Table 3-5. 20 MHz Intel386™ DX A.C. Characteristics

Symbol	Parameter	20 MHz Intel386™ DX		Unit	Ref. Fig.	Notes
		Min	Max			
	Operating Frequency	4	20	MHz		Half of CLK2 Frequency
t_1	CLK2 Period	25	125	ns	3-3	
t_{2a}	CLK2 High Time	8		ns	3-3	at 2V
t_{2b}	CLK2 High Time	5		ns	3-3	at (V_{CC} − 0.8V)
t_{3a}	CLK2 Low Time	8		ns	3-3	at 2V
t_{3b}	CLK2 Low Time	6		ns	3-3	at 0.8V
t_4	CLK2 Fall Time		8	ns	3-3	(V_{CC} − 0.8V) to 0.8V
t_5	CLK2 Rise Time		8	ns	3-3	0.8V to (V_{CC} − 0.8V)
t_6	A2–A31 Valid Delay	4	30	ns	3-5	$C_L = 120$ pF
t_7	A2–A31 Float Delay	4	32	ns	3-6	(Note 1)
t_8	BE0#–BE3#, LOCK# Valid Delay	4	30	ns	3-5	$C_L = 75$ pF
t_9	BE0#–BE3#, LOCK# Float Delay	4	32	ns	3-6	(Note 1)
t_{10}	W/R#, M/IO#, D/C#, ADS# Valid Delay	6	28	ns	3-5	$C_L = 75$ pF
t_{11}	W/R#, M/IO#, D/C#, ADS# Float Delay	6	30	ns	3-6	(Note 1)
t_{12}	D0–D31 Write Data Valid Delay	4	38	ns	3-5c	$C_L = 120$ pF
t_{13}	D0–D31 Float Delay	4	27	ns	3-6	(Note 1)
t_{14}	HLDA Valid Delay	6	28	ns	3-6	$C_L = 75$ pF
t_{15}	NA# Setup Time	9		ns	3-4	
t_{16}	NA# Hold Time	14		ns	3-4	
t_{17}	BS16# Setup Time	13		ns	3-4	
t_{18}	BS16# Hold Time	21		ns	3-4	
t_{19}	READY# Setup Time	12		ns	3-4	
t_{20}	READY# Hold Time	4		ns	3-4	
t_{21}	D0–D31 Read Setup Time	11		ns	3-4	
t_{22}	D0–D31 Read Hold Time	6		ns	3-4	
t_{23}	HOLD Setup Time	17		ns	3-4	
t_{24}	HOLD Hold Time	5		ns	3-4	
t_{25}	RESET Setup Time	12		ns	3-7	

3.2.2 A.C. SPECIFICATION TABLES (Continued)

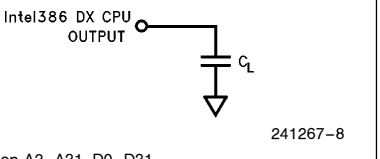
Functional Operating Range: $V_{CC} = 5V \pm 5\%$; $T_{CASE} = 0°C$ to $+100°C$

Table 3-5. 20 MHz Intel386™ DX A.C. Characteristics (Continued)

Symbol	Parameter	20 MHz Intel386™ DX		Unit	Ref. Fig.	Notes
		Min	Max			
t_{26}	RESET Hold Time	4		ns	3-7	
t_{27}	NMI, INTR Setup Time	16		ns	3-4	(Note 2)
t_{28}	NMI, INTR Hold Time	16		ns	3-4	(Note 2)
t_{29}	PEREQ, ERROR#, FLT#, BUSY# Setup Time	14		ns	3-4	(Note 2)
t_{30}	PEREQ, ERROR#, FLT#, BUSY# Hold Time	5		ns	3-4	(Note 2)

NOTES:
1. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not 100% tested.
2. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.

3.2.3 A.C. TEST LOADS



C_L = 120 pF on A2–A31, D0–D31
C_L = 75 pF on BE0#–BE3#, W/R#, M/IO#, D/C#, ADS#, LOCK#, HLDA
C_L includes all parasitic capacitances.

Figure 3-2. A.C. Test Load

3.2.4 A.C. TIMING WAVEFORMS

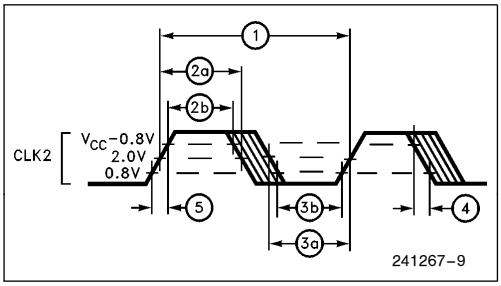


Figure 3-3. CLK2 Timing

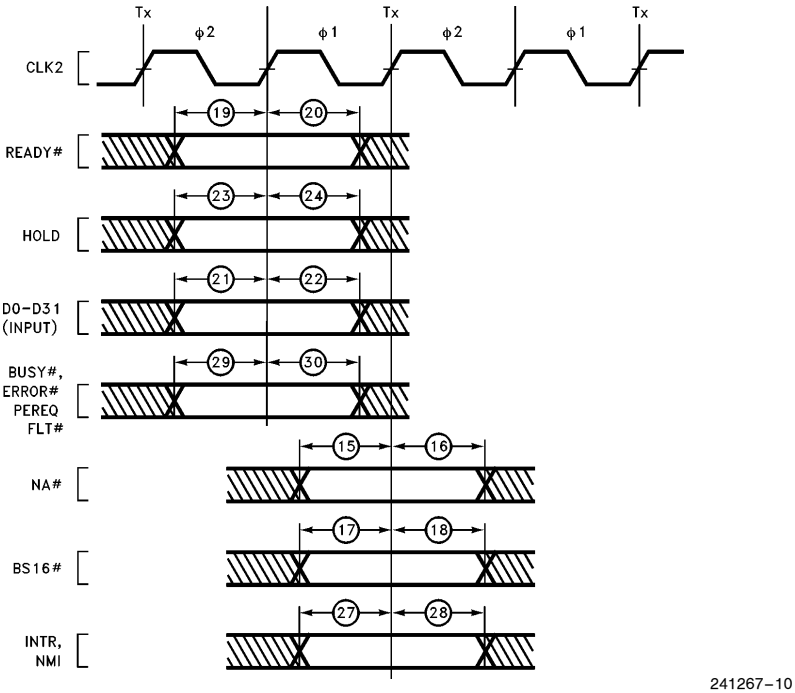


Figure 3-4. Input Setup and Hold Timing

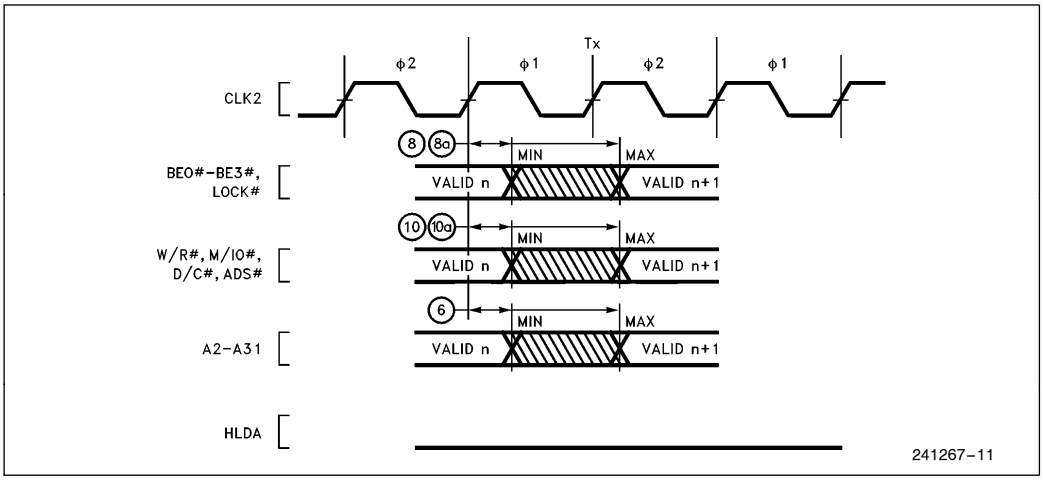


Figure 3-5. Output Valid Delay Timing

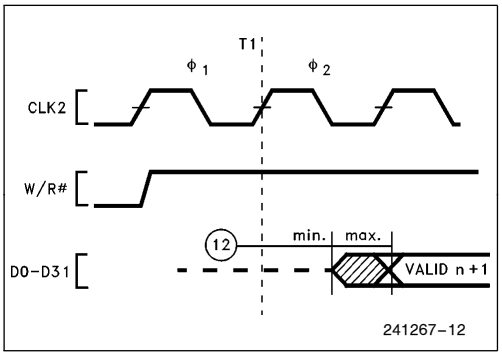


Figure 3-5a. Write Data Valid Delay Timing (25 MHz, 33 MHz)

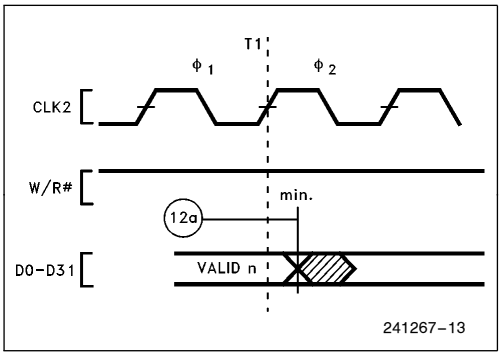


Figure 3-5b. Write Data Hold Timing (25 MHz, 33 MHz)

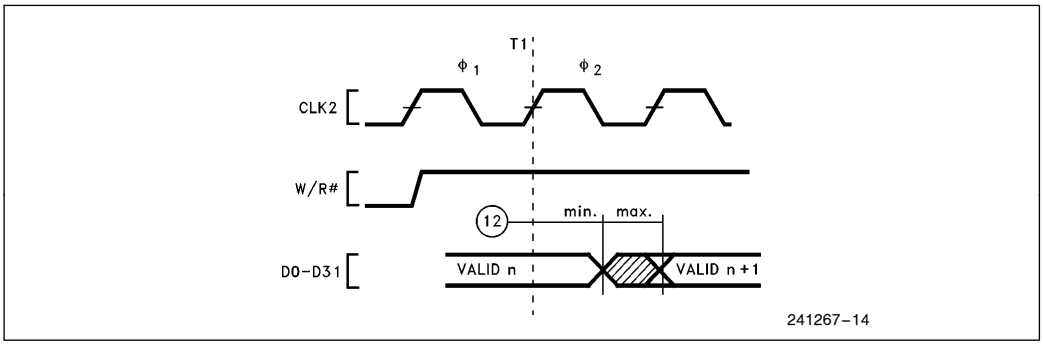
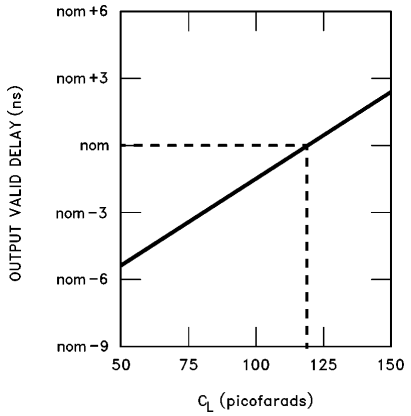


Figure 3-5c. Write Data Valid Delay Timing (20 MHz)

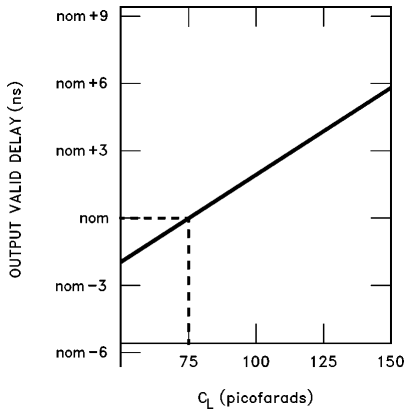
3.2.5 TYPICAL OUTPUT VALID DELAY VERSUS LOAD CAPACITANCE AT MAXIMUM OPERATING TEMPERATURE (C_L = 120 pF)



241267–15

NOTE:
This graph will not be linear outside of the C_L range shown.

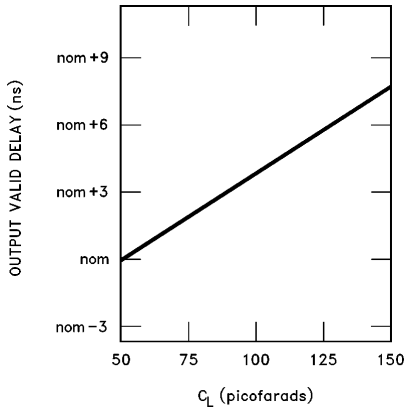
3.2.6 TYPICAL OUTPUT VALID DELAY VERSUS LOAD CAPACITANCE AT MAXIMUM OPERATING TEMPERATURE (C_L = 75 pF)



241267–16

NOTE:
This graph will not be linear outside of the C_L range shown.

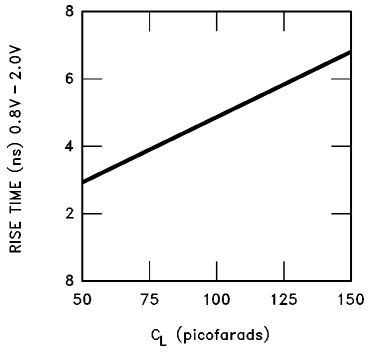
3.2.7 TYPICAL OUTPUT VALID DELAY VERSUS LOAD CAPACITANCE AT MAXIMUM OPERATING TEMPERATURE (C_L = 50 pF)



241267-17

NOTE:
This graph will not be linear outside of the C_L range shown.

3.2.8 TYPICAL OUTPUT RISE TIME VERSUS LOAD CAPACITANCE AT MAXIMUM OPERATING TEMPERATURE



241267-18

NOTE:
This graph will not be linear outside of the C_L range shown.

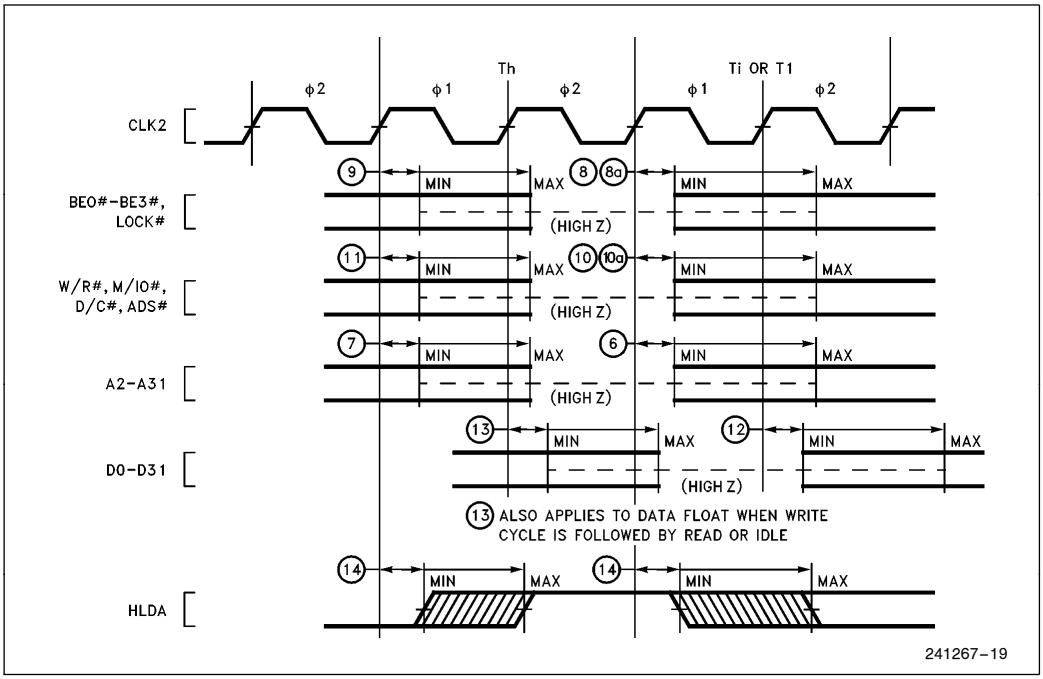
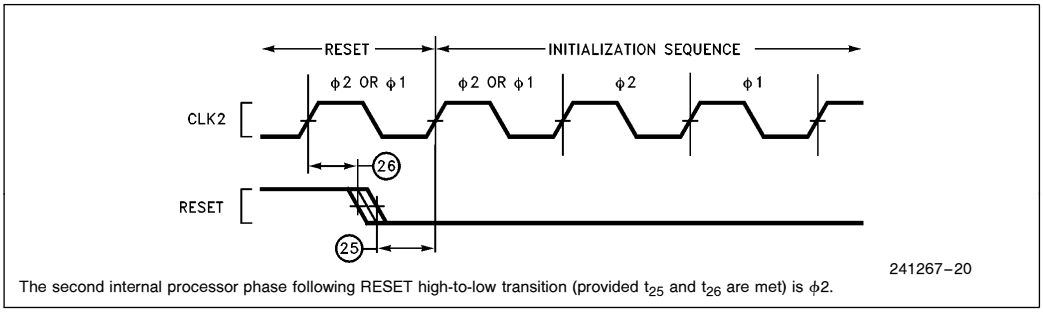


Figure 3-6. Output Float Delay and HLDA Valid Delay Timing



The second internal processor phase following RESET high-to-low transition (provided t_{25} and t_{26} are met) is $\phi 2$.

Figure 3-7. RESET Setup and Hold Timing, and Internal Phase