

8-bit μ P-compatible D/A converter

5018

FEATURES

- 8-bit resolution
- Input latches
- Low-loading data inputs
- On-chip voltage reference
- Output buffer amplifier
- Accurate to $\pm 1/2$ LSB (0.19%)
- Monotonic to 8 bits
- Amplifier and reference both short-circuit protected
- Compatible with 8085, 68000 and many other μ Ps

APPLICATIONS

- Precision 8-bit D/A converters
- A/D converters
- Programmable power supplies
- Test equipment
- Measuring instruments
- Analog-digital multiplication

DESCRIPTION

The 5018 is a complete 8-bit digital-to-analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal) and high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature coefficient.

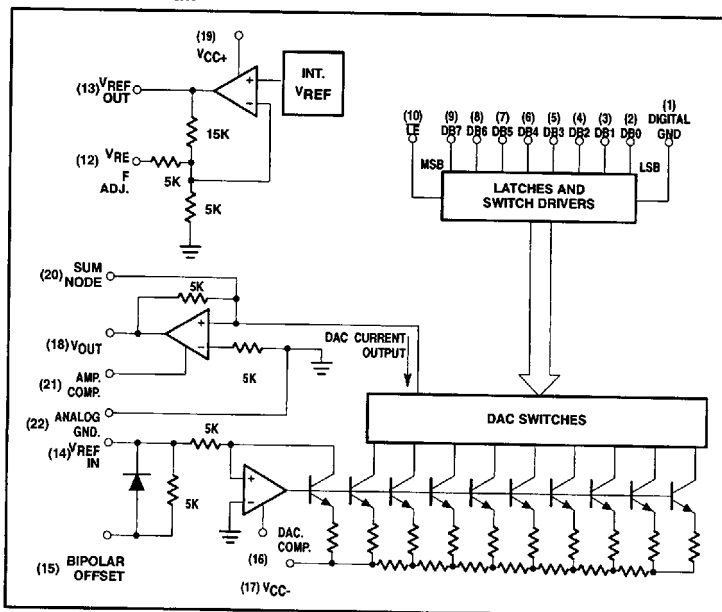
The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

ORDERING INFORMATION

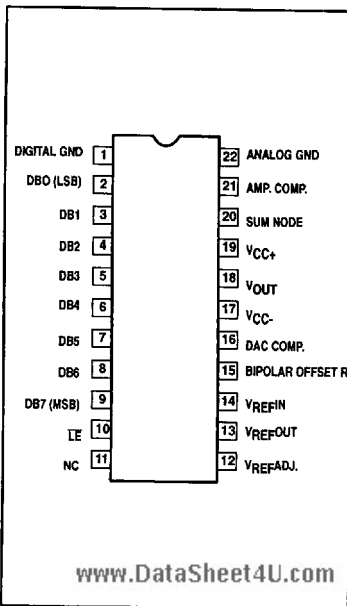
DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
22-Pin Ceramic DIP	5018/BWA	GDIP1-T22

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

BLOCK DIAGRAM



PIN CONFIGURATION



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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING ¹	UNIT
V_{CC+}	Positive supply voltage	18	V
V_{CC-}	Negative supply voltage	-18	V
V_I	Logic input voltage	0 to 18	V
V_{REFIN}	Voltage at V_{REF} input	12	V
V_{REFADJ}	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REFOUT}	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Power dissipation	1000	mW

DC ELECTRICAL CHARACTERISTICS

 $V_{CC+} = +15V$, $V_{CC-} = -15V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS ²	$T_{amb} = +25^{\circ}C$			$T_{amb} = -55^{\circ}C, +125^{\circ}C$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ΔFS	Resolution		8	8	8	8		8	Bits
	Monotonicity		8	8	8	8		8	Bits
	Relative accuracy				± 0.19			± 0.19	%FS
V_{CC+}	Positive supply voltage		+11.4	+15		+11.4	+15		V
V_{CC-}	Negative supply voltage		-11.4	-15		-11.4	-15		V
V_{IH}	Logic "1" input voltage	Pin 1 = GND	2.0		0.8	2.0		0.8	V
V_{IL}	Logic "0" input voltage	Pin 1 = GND							V
I_{IH}	Logic "1" input current	Pin 1 = GND, $2V < V_I < 18V$		0.1	10			10	μA
I_{IL}	Logic "0" input current	Pin 1 = GND, $-5V < V_I < 0.8V$		-2.0	-10			-10	μA
V_{FS}	Full scale output voltage	Unipolar operation $V_{REFIN} = 5.000V$	9.50	9.961	10.50				V
V_{FS}	Full scale output voltage	Bipolar operation $V_{REFIN} = 5.000V$	4.5	4.961	5.5				V
V_{ZS}	Zero scale voltage	Bipolar operation	-5.25	-5.000	-4.75				V
I_{SC}	Output short circuit current	$V_O = 0V$		15	40				mA
$PSR^{+}(out)$	Output power supply rejection (+)	$V_{CC-} = -15V$, $13.5V \leq V_{CC+} \leq 16.5V$, external $V_{REFIN} = 5.000V$		0.001	0.01			0.01	%FS/ %VS
$PSR^{-}(out)$	Output power supply rejection (-)	$V_{CC+} = -15V$, $-13.5V \leq V_{CC-} \leq -16.5V$, external $V_{REFIN} = 5.000V$		0.001	0.01			0.01	%FS/ %VS
TC_{FS}	Full scale temperature coefficient	$V_{REFIN} = 5.000V$					20		ppm/ $^{\circ}C$
TC_{ZS}	Zero scale temperature coefficient						5		ppm/ $^{\circ}C$
I_{REF}	Reference output current ⁹	$V_{REFOUT} = 0V$		15	3				mA
I_{REFSC}	Reference short circuit current				30				mA
$PSR^{+}(REF)$	Reference power supply rejection (+)	$V_{CC-} = -15V$, $13.5V \leq V_{CC+} \leq 16.5V$, $I_{REF} = 1.0mA$		0.003	0.01			0.01	%FR/%VS
$PSR^{-}(REF)$	Reference power supply rejection (-)	$V_{CC+} = -15V$, $-13.5V \leq V_{CC-} \leq -16.5V$, $I_{REF} = 1.0mA$		0.003	0.01			0.01	%FR/%VS
V_{REF}	Reference voltage	$I_{REF} = 1.0mA$	4.9	5.0	5.25				V

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DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS ²	T _{amb} = +25°C			T _{amb} = -55°C, +125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$\Delta Y_{REF}/\Delta T$	Reference voltage temperature coefficient	I _{REF} = 1.0mA					60		ppm/°C
Z _{IN}	DAC V _{REF} IN input impedance	I _{REF} = 1.0mA	4.15	5.0	5.85				k Ω
I _{CC+}	Positive supply current	V _{CC+} = 15V		7	14			14	mA
I _{CC-}	Negative supply current	V _{CC-} = -15V		-10	-15			-15	mA
P _D	Power dissipation	I _{REF} = 1.0mA, V _{CC} = $\pm$ 15V		255	435			435	mW

AC ELECTRICAL CHARACTERISTICS

V_{CC+} = +15V, V_{CC-} = -15V, unless otherwise specified.

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS www.DataSheet4U.com	T _{amb} = +25°C			T _{amb} = 55°C, +125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t _{SLH}	Setting time ⁴	$\pm 1/2$ LSB	Input	All bits low-to-high ³		1.8					μ s
t _{SHL}	Setting time ⁵	$\pm 1/2$ LSB	Input	All bits high-to-low		2.3					μ s
t _{PLH}	Propagation delay ⁴	Output	Input	All bits switched low-to-high		300					ns
t _{PHL}	Propagation delay ⁵	Output	Input	All bits switched high-to-low		150					ns
t _{PLSB}	Propagation delay ^{4, 5}	Output	Input	1 LSB change ^{3, 4}		150					ns
t _{PLH}	Propagation delay ⁶	Output	$\overline{LE}$	Low-to-High transition		300					ns
t _{PHL}	Propagation delay ⁷	Output	$\overline{LE}$	High-to-Low transition		150					ns
t _S	Setup time ^{3, 8}	$\overline{LE}$	Input		100						ns
t _H	Hold time ^{3, 8}	Input	$\overline{LE}$		50						ns
t _{PW}	Latch enable pulse width ^{3, 8}				150						ns

NOTES:

- Operation beyond limits in the table may impair the useful life of the device.
- Refer to Figure 1.
- Refer to Figure 2.
- See Figure 5.
- See Figure 6.
- See Figure 7.
- See Figure 8.
- See Figure 9.
- For reference currents > 3mA, use of an external buffer is required.

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TEST CONFIGURATIONS AND WAVEFORM DEFINITIONS

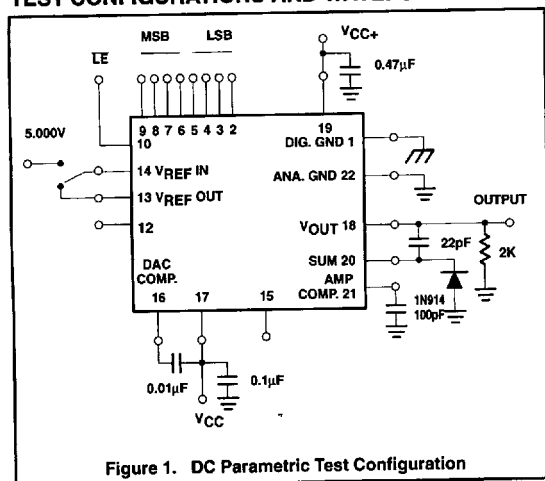


Figure 1. DC Parametric Test Configuration

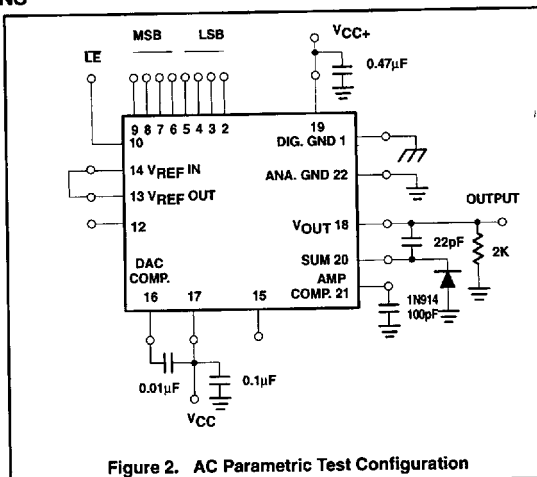


Figure 2. AC Parametric Test Configuration

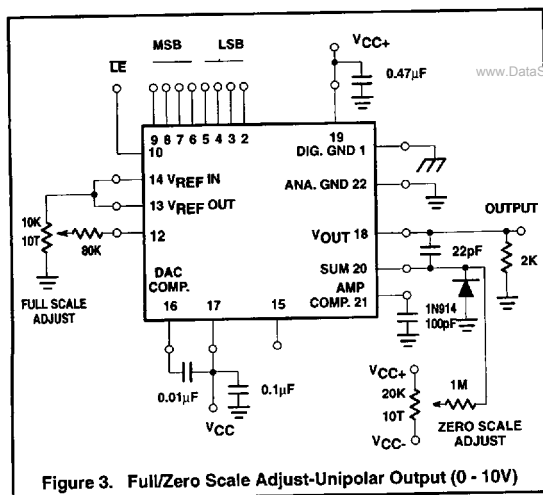


Figure 3. Full/Zero Scale Adjust-Unipolar Output (0 - 10V)

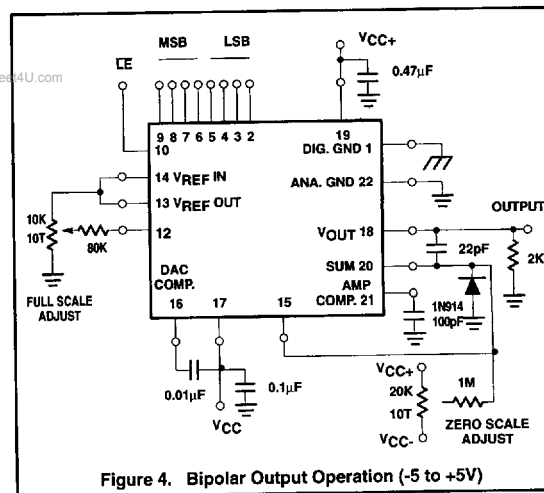


Figure 4. Bipolar Output Operation (-5 to +5V)

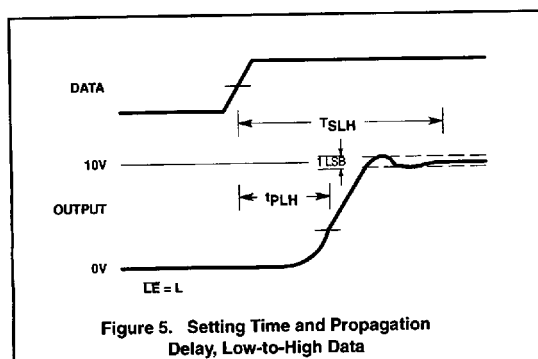


Figure 5. Setting Time and Propagation Delay, Low-to-High Data

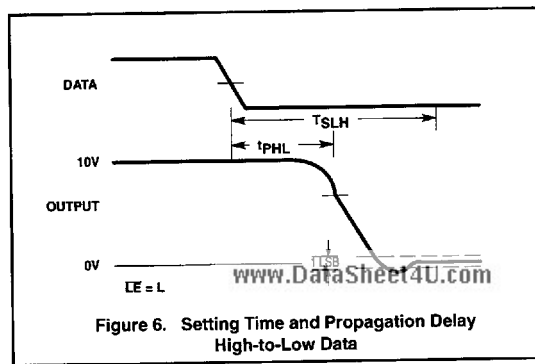


Figure 6. Setting Time and Propagation Delay, High-to-Low Data

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TEST WAVEFORM DEFINITIONS

