DYMEC

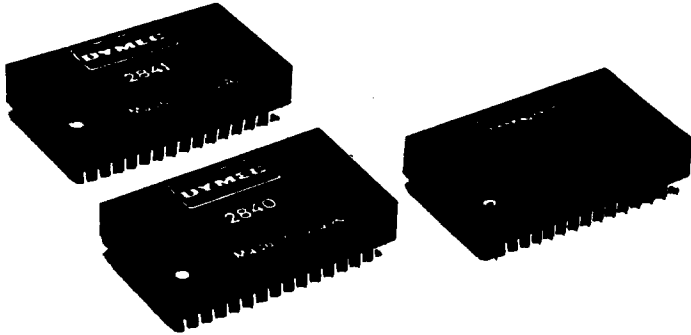## 20 BIT A/D CONVERTER SERIES

2840 20 Bits at 100 mSec
2841 20 Bits at 500 mSec
2842 20 Bits at 1 Sec

Description

Models 2840, 2841& 2842 are complete, integrating A/D converters performing 20 Bit Conversions in 100 Milliseconds, 500 Milliseconds and 1 Second respectively. This Series uses the charged-balanced asynchronous V/F converter with internal counter/timer architecture for ultra-precise repeatability of wide dynamic range, slowly varying signals.

With an input range of 10 µV to 10V, this series provides A/D conversion with a Dynamic Range of 1,000,000:1 (120db) without the complications and errors associated with gain ranging or logarithmic schemes.

Their unique architecture allows for integration of the input signal, thus improving common mode and normal mode rejection and for continuous sampling of the input signal, avoiding the annoying dead time associated with most integrating converters. The 2840, 2841,2842 Series achieves remarkable repeatability of 0.3 ppm at up to 100 samples per second depending on Mode, Speed & Resolution chosen (see respective applications criteria)

Commands to the converter and data from the converter are accomplished via an 8 bit microprocessor compatible bus. The unit can be used in continuous sample or triggered mode, where a data ready flag alerts the µP that the conversion is complete.

Features

20 Bit Integrating A/D

Programmable Conversion Time

Continuous sampling

<10µV Sensitivity

Repeatability to 0.3ppm

Microprocessor Compatible

Applications

Analytical Instrumentation

Automatic Test Equipment

Clinical Chemistry

Data Acquisition Systems

Elemental Analysis

Magnetometers

Medical Instrumentation

Seismology

Thickness & Weighing Systems

ANALOG INPUT

Input Range
-10μV to -10V

Overrange
5%

Configuration
Single-ended

Impedance
6 KΩ

Offset Voltage
±10mV trimmable to zero

Overvoltage Protection
±Vs without damage

TRANSFER CHARACTERISTICS

V/F Full Scale
2840   10MHz
2841   5 MHz
2842   2 MHz

Gain Error
±1%, Trimmable to zero

Differential NonLinearity
2840   0.1 ppm
2841   0.2 ppm
2842   0.5 ppm

Integral Non-Linearity
2840   ±0.05% FS ±0.05% of input
2841   ±0.02% FS ±0.02% of input
2842   ±0.01% FS ±0.01% of input

Fullscale Step Response
2840   5μSec plus 2 cycles of new frequency
2841   10μSec plus 2 cycles of new frequency
2842   20μSec plus 2 cycles of new frequency

Overload Receiving
2840   12 cycles of new frequency
2841   10 cycles of new frequency
2842   8 cycles of new frequency

Noise (3 Sigma)
(10V Input, 1 SPS, 3 minutes)
2840   5μV
2841   4μV
2842   3μV

STABILITY

Gain-Tempco
60ppm FS/°C typical
100ppm FS/°C maximum

Gain - P.S. Sensitivity
200ppm/1% changes in P.S.

Offset-Tempco
10μV/°C typical
30μV/°C maximum

Offset - P.S. Sensitivity
10μV/1% change in P.S.

Warm-up Time
≤ 2 minutes to specified acc'y

Digital Inputs
R/W   50nSec min.
A0,A1,A2   10nSec min.
E Setup   10nSec min.
E Hold   10nSec min.
D0-D7 Setup 10nSec min.
D0-D7 Hold   10nSec min.

Levels
All levels TTL compatible

ENVIRONMENTAL & MECHANICAL

Power Supply
+15V ±3% @ 3mA
-15V ±3% @ 10mA
+5V ±5V @ 200m

Temperature Range
Operating   0° to +70°C
Storage   -25°C to 100°C

THEORY OF OPERATION

The 2840, 2841, 2842 Series uses a charged balanced asynchronuous V/F converter with internal counter timer architecture as shown in Figure 1. The full scale range of the V/F is 10MHz for the 2840, 5MHz for the 2841 and 2MHz for the 2842. The input signal is tracked by the V/F producing a pulse frequency linearly proportional to its full scale, ie:

$$\frac{Vin}{V_{FS}} = \frac{Fout}{F_{FS}}$$

This frequency is accumulated by the counter/timer for the full conversion time of the A/D and presented at the output as a binary word up to 24 bits wide. The continuous tracking and accumulation of pulses performs an inherently montonic integrating function.

Once the pulse accumulation is complete, the count is instantaneously transferred to the output stage, ready to be accessed by the μP. In the continuous sample mode, the counter/timer instantaneously begins to accumulate counts for the next measurement. In the external trigger mode, the counter/timer awaits a trigger command before beginning the next accumulation of pulses. In both cases the V/F continues to generate a pulse frequency proportionately tracking the input signal. There is no dead time on these converters so the integration period and the conversion times are the same and the terms are used interchangeably.
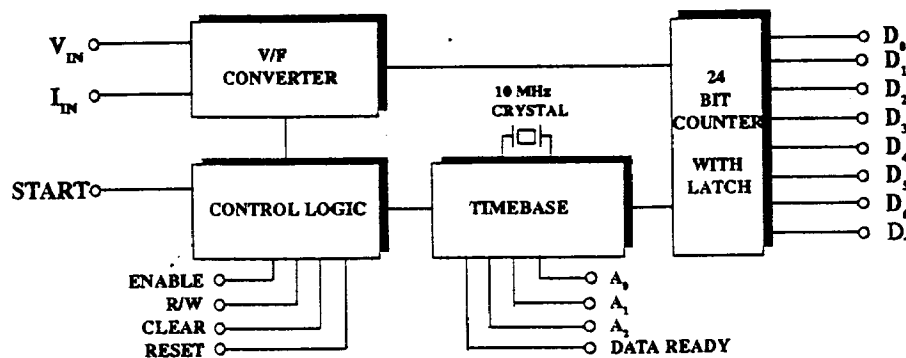

FIGURE 1 - Block Diagram

SENSITIVITY VS SPEED

The sensitivity of the 2840, 2841, 2842 Series is directly proportional to the amount of time the converter is allowed to integrate the input signal.

$$\text{Sensitivity} = \frac{V_{FS} \cdot T_C}{F_{FS}}$$

Where

V_{FS} = Full Scale Voltage
F_{FS} = Full Scale Frequency of the V/F
T_C = Conversion Time.

For example: If the 2840, (with it's 10MHz V/F) integrates the input signal for 1/10th of a second, it will accumulate 1,000,000 pulses. If the fullscale input voltage is 10V, each pulse counted will represent 10μV. Thus, the sensitivity of the 2840 at 10 samples per second is 10μV.

Model / Conversion Time	2840 10MHz	2841 5MHz	2842 2MHz
100 SPS	100μV (16 Bits)	200μV (15Bits)	500μV (14 Bits)
10 SPS	10μV (20 Bits)	20μV (19 Bits)	50μV (18 Bits)
1 SPS	1μV (23 Bits)	2μV (22 Bits)	5μV (21 Bits)

TABLE I - Sensitivity and Resolution With 0-10V F.S

CHOOSING A CONVERSION TIME

The architecture of the 2840, 2841, 2842 Series allows the designer to choose the conversion time of the A/D converter, for the sensitivity, for Conversion Time or a Combination of both criteria.

    a- **For Sensitivity** -- Often sensitivity, that is, the minimum change in input voltage detectable by the converter will be the overriding criteria.

    In that case, calculate the percent of full scale represented by the sensitivity. The inverse of that number represents the full scale count needed.

$$S = (V_{FS}/F_{FS}) \cdot T$$

For Example $10\mu V$ on $10V_{FS}$ =1ppm   or   1mV on 10V = 0.01%

                     $1/1\text{ppm} = 10^6$ counts $1/0.01\% = 10^4$ counts

    Next determine the amount of time required for the V/F to generate that count full scale. That will be your conversion time:

Model	10^6 Counts		10^4 Counts
2840 (10MHz)	0.1 Sec	or	.001 Sec
2841 (5MHz)	0.2 Sec		.002 Sec
2842 (2MHz)	0.5 Sec		.005 Sec

    b - **For Conversion Time** $T = $ Sensitivity $\cdot (F_{FS}/V_{FS})$

Example: At 100MSec integrating (conversion) time

Model	Count	Resolution	Sensitivity
2840 (10MHz)	10^6 counts FS	~ 20 Bits	$10\mu V$
2841 (5MHz)	5×10^5 counts FS	~ 19 Bits	$20\mu V$
2842 (2MHz)	2×10^5 counts FS	~ 18 Bits	$50\mu V$

    c - **Combination** -- In multiplexed systems different sensitivity/speed combinations may be required for each channel. This is easily accomplished with the 2840, 2841, 2842 Series by a simple program command setting the conversion time.

    With the very wide dynamic range of the 2841, 2841, 2842 Series the entire input range can be sampled at high speed and low resolution until the desired level is detected. Then the integration time can be extended for higher sensitivity measurements.

    Where several instruments share one analog front end design - combination of speed and sensitivity can be programmed into 2840, 2841, 2842 Series "on the fly."

    Sometimes the conversion time dominates the design decision. This is true when trying to reject periodic normal mode noise- such as 50/60 Hz line pick up. Then the conversion time should be set at an integer multiple of the period of the noise (ie 20mS or 40mS or 60 mS for 50Hz rejection). 100mS integration is common as it rejects both 50 & 60Hz pickup, Once the conversion time is chosen, the resolution and sensitivity can be calculated.
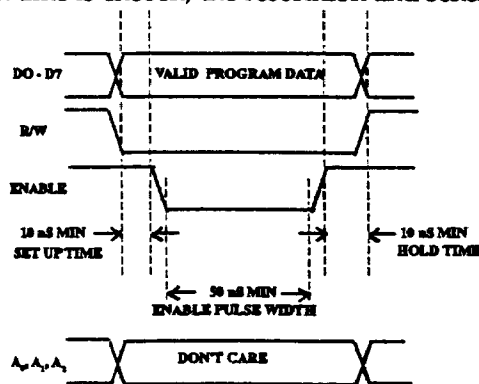

FIGURE 2   Write Commanding

PROGRAMMING CONVERSION TIME

Conversion time is programmed by writing an 8 bit word to the A/D converter. R/W should be placed in a logic 0. Program data are loaded on lines D0-D7 and the Enable command is strobed low per Figure 2.
Note setup and hold time of 10nSec minimum before and after Enable and the 50nSec minimum Enable pulse width.

The programmed conversion time (T_C) is related to an external clock (F_{Clk}) by the following formula.
Clock frequencies up to 50MHz are acceptable

$$T_C = \frac{1}{F_{Clk}} \times B \times 10^N \qquad \text{For a 10MHz Crystal } T_C = \frac{1}{10^7} \times B \times 10^N$$

STEP 1 - Select desired conversion (integration) time.
STEP 2 - Multiply time base by F_{Clk}. The answer is $B \times 10^N$
STEP 3 - Choose B as large as possible within 1-16 range. Determine appropriate N.
STEP 4 - Assemble program byte (with MSB = 1) selecting N & B from Table II.

Word	MSB D7		D6	D5	D4		D3	D2	D1	LSB D0
Function	MSB		N2	N1	N0		B3	B2	B1	B0
Code	M-1	N =	N2	N1	N0	B =	B3	B2	B1	B0
	0	0	0	0	0	1	1	1	1	1
		1	0	0	1	2	1	1	1	0
		2	0	1	0	3	1	1	0	1
		3	0	1	1	4	1	1	0	0
		4	1	0	0	5	1	0	1	1
		5	1	0	1	6	1	0	1	0
		6	1	1	0	7	1	0	0	1
		7	1	1	1	8	1	0	0	0
						9	0	1	1	1
						10	0	1	1	0
						11	0	1	0	1
						12	0	1	0	0
						13	0	0	1	1
						14	0	0	1	0
						15	0	0	0	1
						16	0	0	0	0

TABLE II - Compiling the Conversion Time Byte

Example 1

1) For T_C = 100 mSec and F_{Clk} = 10MHz

2) $T_C \times F_{Clk} = B \times 10^N$
   100mSec $\times 10 \times 10^6 = 10 \times 10^5$

3) Choose N=5   B=10

4) Code

	MSB	N	B
	0	101	0110

Example 2

1) For T_C = 1 mSec and F_{Clk}=10MHz

2) $T_C \times F_{Clk} = B \times 10N$
   1mSec $\times 10 \times 10^6 = 10 \times 10^3$

3) Choose   N = 3   B = 10

4) Code

	MSB	N	B
	0	011	0110

5

READING THE DATA

The 2840, 2841, 2842 Series is capable of up to 24 bit measurements. These are read out on the 8 Bit bus in three bytes. There are also overflow and programming bytes. The bytes are addressed at pins A_0, A_1, A_2 per TABLE III via the timing commands in FIGURE 3.

To read data, set the R/W line to the logical "1" (high) state, and the A0, A1, A2 control lines to the appropriate states for the data byte desired. The order in which these signals are applied isn't important, as long as they are present and static for at least 10 nS before the Enable (E) line is activated, and for a minimum of 10nS after Enable (E) is removed. The Enable line performs the actual read operation, it is a negative pulse, at least 50nS wide. Valid data is present on the output bus 30nS maximum after the leading edge of Enable; the data bus returns to a high impedance state 25nS maximum after the trailing edge of the Enable pulse.

A0	A1	A2	COMMAND	BYTE
0	0	0	READ	LOWER
1	0	0	READ	MIDDLE
0	1	0	READ	UPPER
1	1	0	READ	OVERFLOW
1	0	1	READ	PROG BYTE

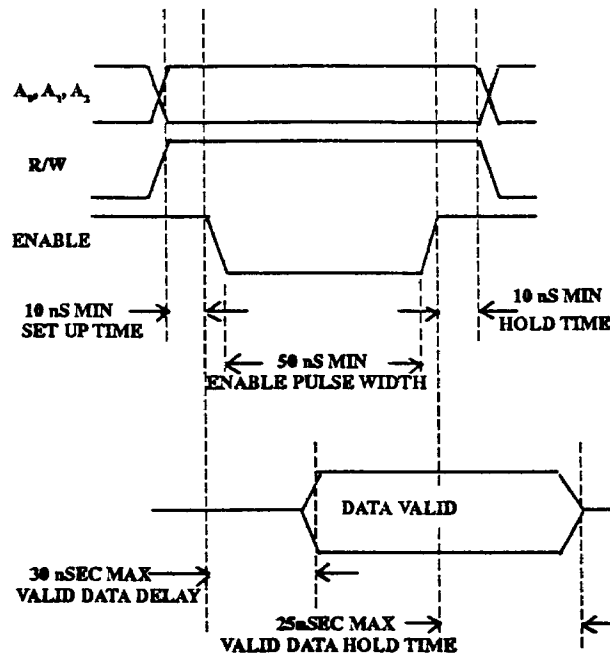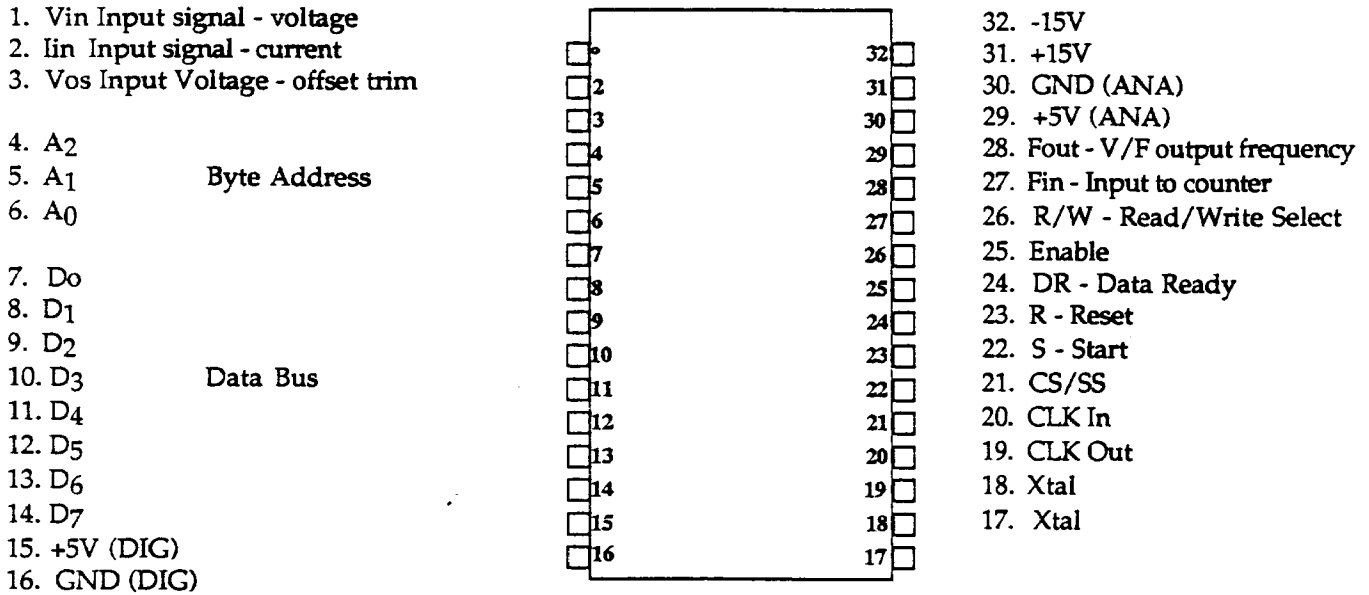TABLE III - Addressing the data bytes

FIGURE 3 - Read Command Timing

OVERFLOW AND PROGRAMMING READBACK BYTES

If the 24 Bit counter overflows, the overflow bit (D_0) on the Overflow Byte (A=110) will be in a high state. The data bits will roll over to zero and continue to count. Thus, using the overflow bit, it is possible to use the 2840, 2841, 2842 Series as a 25 bit converter. See table III and Figure 4 for commands and timing.

At anytime the A/D can be interrogated as to it's programmed status by reading the Program Readback Byte (A=101). This will read back the conversion time program byte.

PIN DESCRIPTION

1. Vin Input signal - voltage		32. -15V
2. Iin Input signal - current		31. +15V
3. Vos Input Voltage - offset trim		30. GND (ANA)
		29. +5V (ANA)
4. A2		28. Fout - V/F output frequency
5. A1 Byte Address		27. Fin - Input to counter
6. A0		26. R/W - Read/Write Select
		25. Enable
7. D0		24. DR - Data Ready
8. D1		23. R - Reset
9. D2		22. S - Start
10. D3 Data Bus		21. CS/SS
11. D4		20. CLK In
12. D5		19. CLK Out
13. D6		18. Xtal
14. D7		17. Xtal
15. +5V (DIG)		
16. GND (DIG)		

All digital signals are TTL compatible

NOTES:

DR- Data Ready - generates a logical "1" that indicates that data has been latched and is ready to read. On Reset (pin 23) Data Ready becomes active high and remains high until a READ operation is performed or conversion is completed.

R - Reset - when logical "0" is applied to pin 23 all operations are stopped and all counters and latches are reset to zero. A minimum pulse width of 100nS at logical 0 is required.

S - Start and CS/SS - Continuous sample /Syncronous Start - when CS/SS is low. The converter will continuously convert the input. When CS/SS is High, the converter will wait for a START command before beginning the next conversion. The START command is positive edge - triggered.
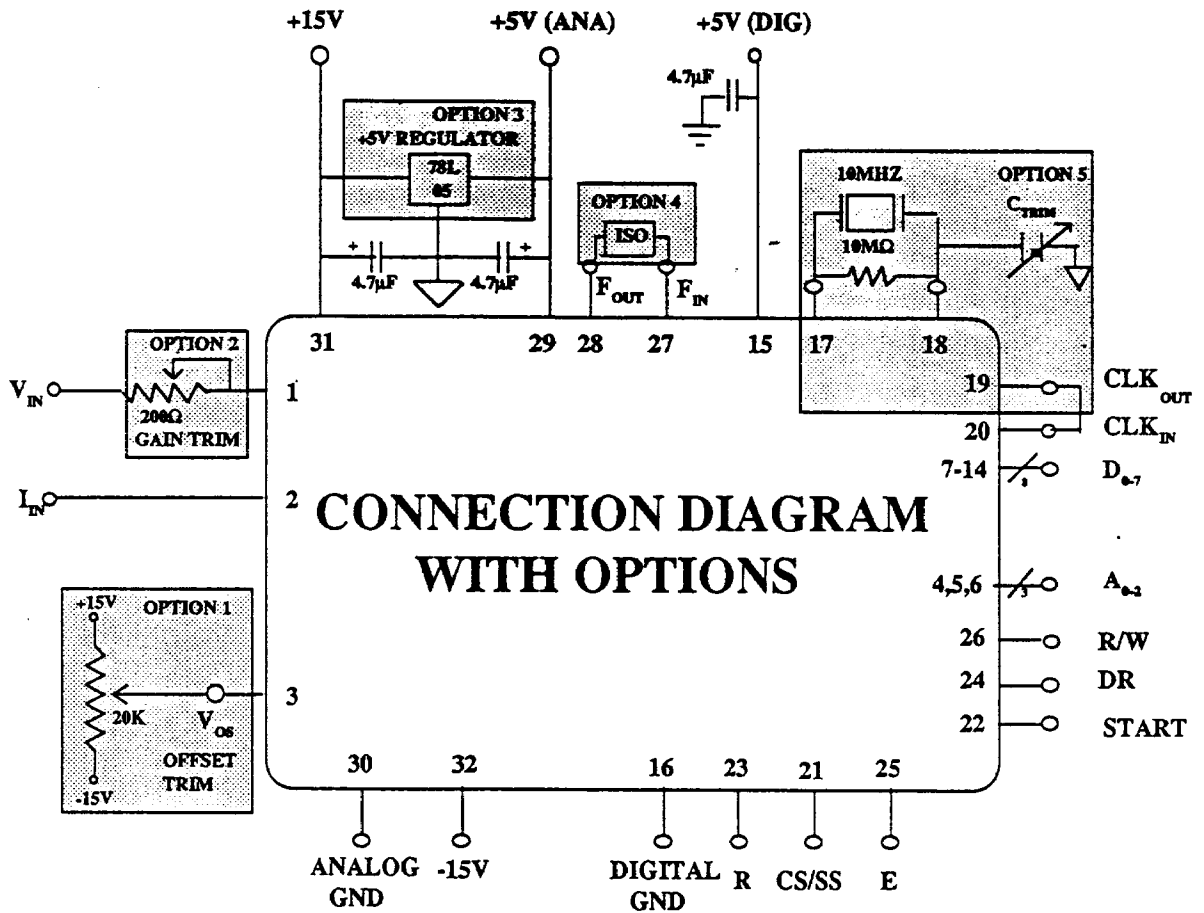
+5V (DIG) and +5V (VFC) may be supplied from the same +5V supply (see option #3 on last page).

Fout and Fin should be tied together for normal operation.
Fout can be used as a test point to check the output of the V/F. An optical isolator or isolation transformer may be inserted between Fout and Fin to totally isolate the analog, and digital sections of the converter. See option #4 on last page.

CLK IN Receives system clock up to 50MHz. CLK in should be tied to CLKout if Crystal Oscillator Clock Circuit is used. See Option #5 on last page.
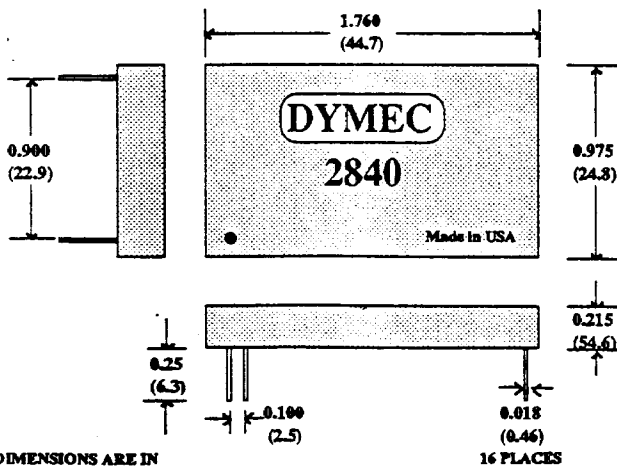
Xtal No connection if clock is supplied by System to pin 20 (CLKin). For self generated Crystal Clock See Option #5 on last page

+15V +5V (ANA) +5V (DIG)

OPTION 3
+5V REGULATOR
78L05

4.7µF

OPTION 4
ISO
F_{OUT} F_{IN}

10MHZ OPTION 5
C_{TRIM}
10MΩ

+ 4.7µF 4.7µF +

OPTION 2
V_{IN} 200Ω GAIN TRIM

OPTION 1
+15V
20K V_{OS}
OFFSET TRIM
-15V

31 29 28 27 15 17 18

1

2 **CONNECTION DIAGRAM WITH OPTIONS**

3

19 CLK_{OUT}
20 CLK_{IN}
7-14 D_{0-7}
4,5,6 A_{0-2}
26 R/W
24 DR
22 START

I_{IN}

30 32 16 23 21 25

ANALOG GND -15V DIGITAL GND R CS/SS E

OPTIONS

1- Offset voltage may be trimmed to zero using a 20KΩ potentionmeter with drift less than 100ppm.

2- Fullscale output can be trimmed to zero error using a 200Ω potentionmeter with drift less than 100ppm.

3- +5V (ANA) may be regulated for optimal performance using a National 78L05 (typical) +5V Regulator.

4- An optical isolator or isolation transformer may be inserted between F_{out} & F_{in} to isolate the analog and digital of the A/D, if dictated by System requirements.

5- Clock frequency may come from a system clock, up to 50MHz maximum, applied to CLK_{IN} (pin 20). Alternately an oscillator clock can be generated using a crystal (10MHz typical). C Trim may then be added to trim the crystal to the exact frequency desired. C Trim values between 2 & 25pf are typical.

DYMEC
2840
Made in USA

1.760 (44.7)
0.900 (22.9)
0.975 (24.8)
0.215 (54.6)
0.25 (6.3)
0.100 (2.5)
0.018 (0.46)
16 PLACES

DIMENSIONS ARE IN INCHES (MILLIMETERS)

ORDERING INFORMATION

2840 20 Bits @ 100MSec

2841 20 Bits @ 200MSec

2842 20 Bits @ 1 Sec

DYMEC

017771 X X

AUG 2 0 1990